

MOSFET - Power, Single N-Channel, DUAL COOL[®]

40 V, 0.78 mΩ, 310 A

Product Preview

NTMFSC0D8N04XM

Features

- Advanced Dual-Sided Cooling Package
- Latest 40 V Power MOSFET Technology for Motor Drive Applications
- Extreme Lower On-Resistance to Minimize Conduction Losses
- Lower Gate Charge to Minimize Gate Driving and Switching Losses
- Soft Body Diode Reverse Recovery
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

Typical Applications

- Motor Drive
- ORing FET
- Battery Protection

MAXIMUM RATINGS (T_J = 25°C, Unless otherwise specified)

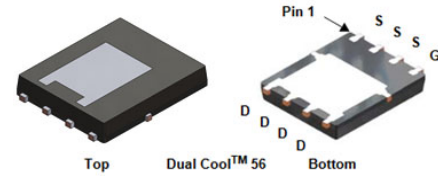
Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	40	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Note 2)	Steady State	T _C = 25°C	I _D	310	A
			P _D	135	W
Continuous Drain Current R _{θJA} (Note 1, 2)	Steady State	T _A = 25°C	I _D	52	A
			P _D	3.8	W
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		I _{DM}	TBD	A
Pulsed Source Current (Body Diode)	T _A = 25°C, t _p = 10 μs		I _{SM}	TBD	A
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode) R _{θJC}			I _S	112	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = TBD A)			E _{AS}	TBD	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T _L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

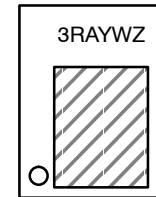
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V _{SSS}	R _{SS(ON)} MAX	I _D MAX
40 V	0.78 mΩ @ 10 V	310 A



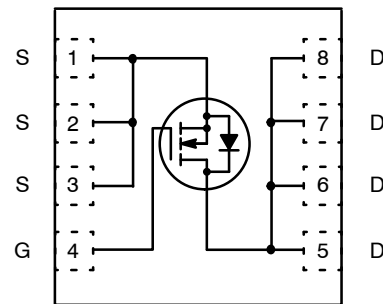
DFN8 5x6
CASE 506EG

MARKING DIAGRAM



- 3R = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- Z = Assembly Lot Code

N-Channel MOSFET



ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction-to-Case (Bottom) – Steady State (Note 3)	1.11	°C/W
$R_{\theta JC}$	Junction-to-Case (Top) – Steady State (Note 3)	1.71	
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Notes 1 and 3)	39	

3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain – to – Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V
Drain – to – Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	$I_D = 1\text{ mA}, \text{ref to } 25^\circ\text{C}$		14.9		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		100	
Gate – to – Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 180\ \mu\text{A}$	2.5		3.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	$I_D = 180\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$		-7.2		mV/°C
Drain – to – Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		0.63	0.78	m Ω
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		TBD		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$		5044		pF	
Output Capacitance	C_{OSS}			3228			
Reverse Transfer Capacitance	C_{RSS}			85			
Output Charge	Q_{OSS}	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$		116		nC	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}, I_D = 50\text{ A}$		72.1			
Threshold Gate Charge	$Q_{G(TH)}$			13.6			
Gate-to-Source Charge	Q_{GS}			20.6			
Gate-to-Drain Charge	Q_{GD}			13.3			
Plateau Voltage	V_{GP}			4.48			V

SWITCHING CHARACTERISTICS (Note 4)

Turn – On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}, I_D = 50\text{ A}, R_G = 2.5\ \Omega$		25.1		ns
Rise Time	t_r			8.1		
Turn – Off Delay Time	$t_{d(OFF)}$			39.1		
Fall Time	t_f			6.3		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		0.80	1.2	V
			$T_J = 125^\circ\text{C}$		0.66		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}, V_{DS} = 20\text{ V}$			65.8		ns
Reverse Recovery Charge	Q_{RR}				139		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures.

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ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSC0D8N04XMTWG	3R	DFN8 5x6 (Pb-Free/Halogen Free)	3000 / Tape & Reel

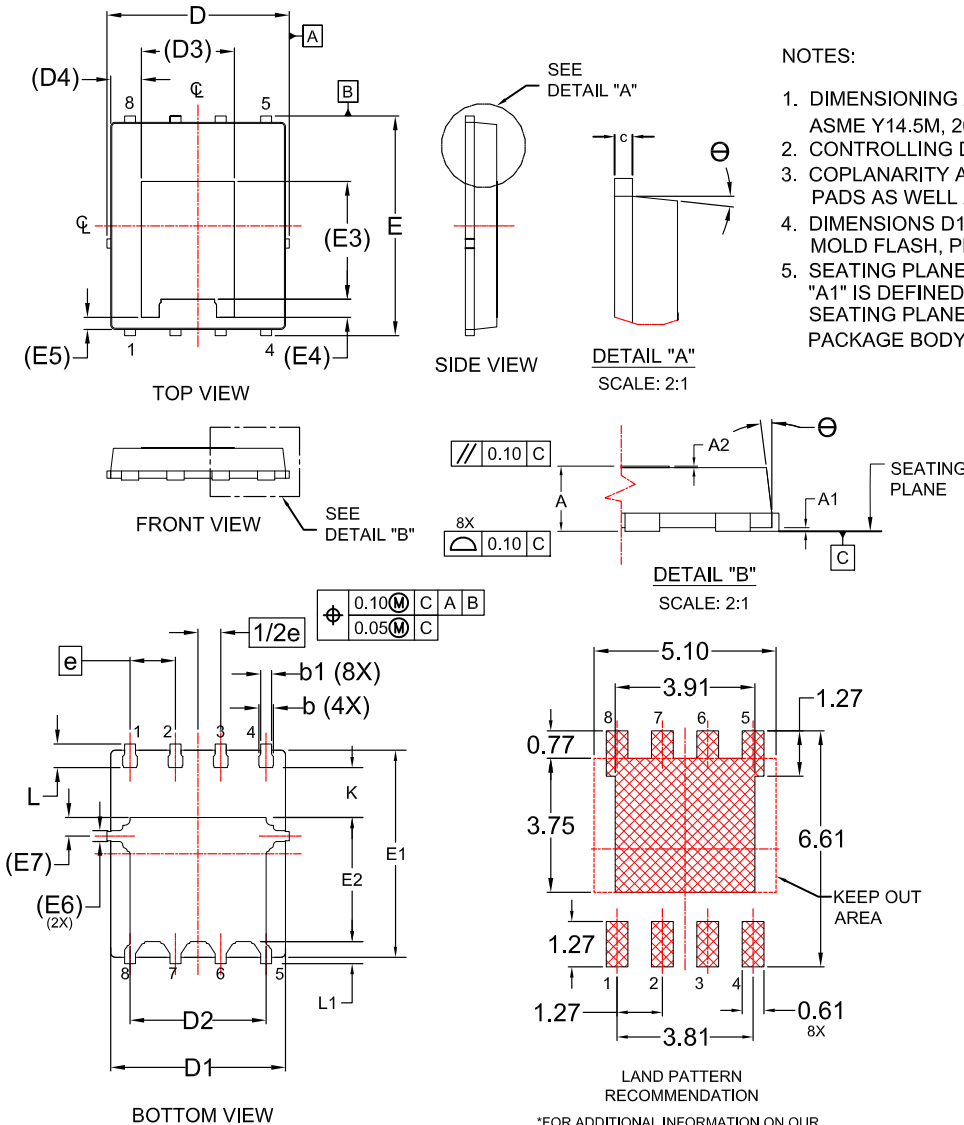
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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NTMFSC0D8N04XM

PACKAGE DIMENSIONS

DFN8 5.1x6.15, 1.27P, DUAL COOL
CASE 506EG
ISSUE D



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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