

MOSFET - Power, Single, N-Channel, STD Gate, DUAL COOL[®], DFN8 5x6

60 V, 1.5 mΩ, 238 A

Preliminary Document NTMFSCHT1D5N06C

Features

- Advanced Dual-Side Cool Package with Enhanced Heat-Dissipation Molding Compound
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_g to Minimize Gate Driving Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Supply Unit (PSU)
- DC/DC Intermediated Bus Converter
- Control FET in High Switching Frequency Application
- Synchronous Rectifier
- ORing FET

MAXIMUM RATINGS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless otherwise specified)

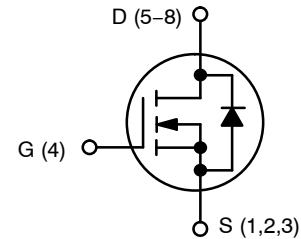
Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	60	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Notes 1, 2)	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	238	A
	$T_C = 100\text{ }^{\circ}\text{C}$		168	
Power Dissipation (Notes 1, 2)	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	166	W
Pulsed Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$, $t_p = 100\text{ }\mu\text{s}$	I_{DM}	676	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^{\circ}\text{C}$
Source-Drain Current (Body Diode)	$T_C = 25\text{ }^{\circ}\text{C}$	I_S	TBD	A
Single Pulse Avalanche Energy ($I_{pk} = \text{TBD A}$) (Note 3)		E_{AS}	TBD	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

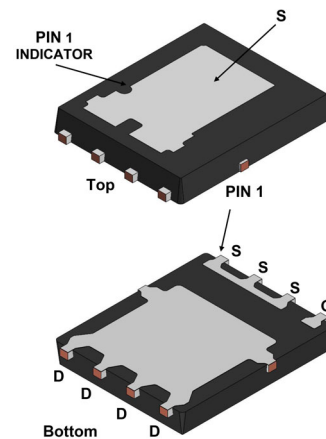
- The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
- Actual continuous current will be limited by thermal & electromechanical application board design.
- E_{AS} of TBD mJ is based on started $T_J = 25\text{ }^{\circ}\text{C}$, $I_{AS} = \text{TBD A}$, $V_{DD} = 48\text{ V}$, $V_{GS} = 10\text{ V}$, 100% avalanche tested.

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}^*$	$I_D \text{ MAX}$
60 V	1.5 mΩ @ $V_{GS} = 10\text{ V}$	238 A

* Target Value.

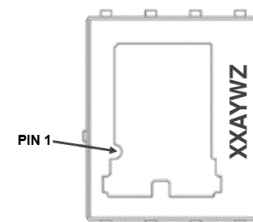


N-CHANNEL MOSFET



**DFN8
CASE 506EA**

MARKING DIAGRAM



XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 3 of this data sheet.

This Preliminary document is for informational purposes only. onsemi may update or withdraw it without notice. Content and referenced products are under development and subject to change.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	0.9	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JCT}$	1.4	
Thermal Resistance, Junction-to-Ambient (Note 4)	$R_{\theta JA}$	39	

4. Actual continuous current will be limited by thermal & electromechanical application board design.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25°C		25		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, T_J = 25^\circ\text{C}$			10	μA
		$V_{DS} = 60\text{ V}, T_J = 125^\circ\text{C}$			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 25^\circ\text{C}$		1.2	1.5	m Ω
		$V_{GS} = 6\text{ V}, I_D = 30\text{ A}, T_J = 25^\circ\text{C}$		TBD	TBD	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.0		4.0	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$		-7		mV/°C
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 30\text{ A}$		161		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance (Note 5)	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}, f = 1\text{ MHz}$		4860	7290	pF
Output Capacitance (Note 5)	C_{OSS}			2800	4200	
Reverse Transfer Capacitance (Note 5)	C_{RSS}			40	80	
Output Charge	Q_{OSS}	$V_{GS} = 6\text{ V}, V_{DD} = 30\text{ V}, I_D = 30\text{ A}$ $V_{GS} = 10\text{ V}, V_{DD} = 30\text{ V}, I_D = 30\text{ A}$		128		nC
Total Gate Charge (Note 5)	$Q_{G(TOT)}$			TBD	TBD	
Threshold Gate Charge	$Q_{G(TH)}$			65	98	
Gate-to-Source Charge	Q_{GS}			13		
Gate-to-Drain Charge	Q_{GD}			22		
Gate-to-Drain Charge	Q_{GD}			11		
Gate Plateau Voltage	V_{GP}			4.6		V
Gate Resistance (Note 5)	R_G	$f = 1\text{ MHz}$		2	3.4	Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 30\text{ V},$ $I_D = 30\text{ A}, R_G = 2.5\text{ }\Omega$		26		ns
Rise Time	t_r			8		
Turn-Off Delay Time	$t_{d(OFF)}$			50		
Fall Time	t_f			9		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 30\text{ A}, T_J = 25^\circ\text{C}$		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 30\text{ A}, T_J = 125^\circ\text{C}$		0.7		

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ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $I_S = 30\text{ A}$, $V_{DD} = 30\text{ V}$, $T_J = 25\text{ }^{\circ}\text{C}$		82		ns
Charge Time	t_a			41		
Discharge Time	t_b			41		
Reverse Recovery Charge	Q_{RR}			139		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Defined by design, not subject to production test.

ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSCHT1D5N06CTWG	TBD	DFN8 4.9x5.8 (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary document release.	11/7/2025

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