

MOSFET – Power, Single N-Channel, STD Gate, DUAL COOL[®], DFN8 5x6

80 V, 3 mΩ, 135 A

Preliminary Document NTMFSCHT3D0N08X

Features

- Advanced Dual-Side Cool Package with Enhanced Heat-Dissipation Molding Compound
- Low Q_{RR} , Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_g to Minimize Gate Driving Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Supply Unit (PSU)
- DC/DC Intermediated Bus Converter
- Control FET in High Switching Frequency Application
- Synchronous Rectifier
- ORing FET

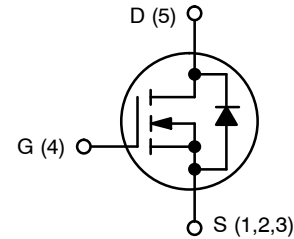
MAXIMUM RATINGS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (Note 1)	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	135	A
	$T_C = 100\text{ }^{\circ}\text{C}$		96	
Power Dissipation (Note 1)	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	119	W
Pulsed Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$, $t_p = 100\text{ }\mu\text{s}$	I_{DM}	543	A
Pulsed Source Current (Body Diode)		I_{SM}	543	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)		I_S	179	A
Single Pulse Avalanche Energy ($I_{PK} = 47\text{ A}$) (Note 3)		E_{AS}	110	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^{\circ}\text{C}$

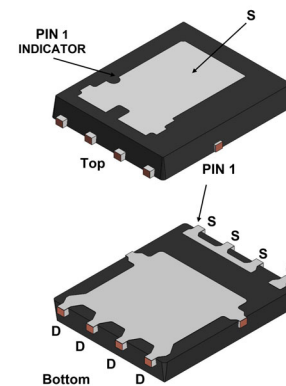
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Actual continuous current will be limited by thermal & electromechanical application board design.
- E_{AS} of 110 mJ is based on started $T_J = 25\text{ }^{\circ}\text{C}$, $I_{AS} = 47\text{ A}$, $V_{DD} = 64\text{ V}$, $V_{GS} = 10\text{ V}$, 100% avalanche tested

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	3 mΩ @ 10 V	135 A

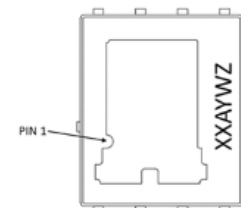


N-CHANNEL MOSFET



DFN8
CASE 506EA

MARKING DIAGRAM



XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 3 of this data sheet.

This Preliminary document is for informational purposes only. onsemi may update or withdraw it without notice. Content and referenced products are under development and subject to change.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	1.3	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JCT}$	1.34	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient (Notes 4 and 5)	$R_{\theta JA}$	39	$^{\circ}\text{C/W}$

4. Surface-mounted on FR4 board using 1 in² pad size, 1 oz. Cu pad.
5. $R_{\theta JA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$. Referenced to 25°C		31.6		$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, T_J = 25^{\circ}\text{C}$			10	μA
		$V_{DS} = 80\text{ V}, T_J = 125^{\circ}\text{C}$			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 31\text{ A}$		2.6	3	$\text{m}\Omega$
		$V_{GS} = 8\text{ V}, I_D = 31\text{ A}$		2.9	3.4	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 153\text{ }\mu\text{A}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 153\text{ }\mu\text{A}$		-7.5		$\text{mV}/^{\circ}\text{C}$
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 31\text{ A}$		97		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance (Note 6)	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$	1340	2680	4020	pF
Output Capacitance (Note 6)	C_{OSS}			780	1170	
Reverse Transfer Capacitance (Note 6)	C_{RSS}			12	24	
Output Charge	Q_{OSS}			56		
Total Gate Charge (Note 6)	$Q_{G(TOT)}$	$V_{GS} = 8\text{ V}, V_{DD} = 40\text{ V}; I_D = 31\text{ A}$		30	45	nC
Total Gate Charge (Note 6)	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DD} = 40\text{ V}; I_D = 31\text{ A}$		38	57	nC
Threshold Gate Charge	$Q_{G(TH)}$			8		
Gate-to-Source Charge	Q_{GS}			13		
Gate-to-Drain Charge (Note 6)	Q_{GD}			6	11	
Gate Plateau Voltage	V_{GP}			4.7		V
Gate Resistance	R_G	$f = 1\text{ MHz}$	0.35	0.7	1.05	Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 40\text{ V},$ $I_D = 31\text{ A}, R_G = 2.5\text{ }\Omega$		23		ns
Rise Time	t_r			7		
Turn-Off Delay Time	$t_{d(OFF)}$			32		
Fall Time	t_f			5		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 31\text{ A}, T_J = 25^{\circ}\text{C}$		0.82	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 31\text{ A}, T_J = 125^{\circ}\text{C}$		0.66		

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI/dt = 1000 A/μs, I _S = 31 A, V _{DD} = 40 V		22		ns
Charge Time	t _a			12		
Discharge Time	t _b			10		
Reverse Recovery Charge	Q _{RR}			144		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Defined by design, not subject to production test.

ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSCHT3D0N08XTWG	TBD	DFN8 4.9x5.8 (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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TYPICAL CHARACTERISTICS

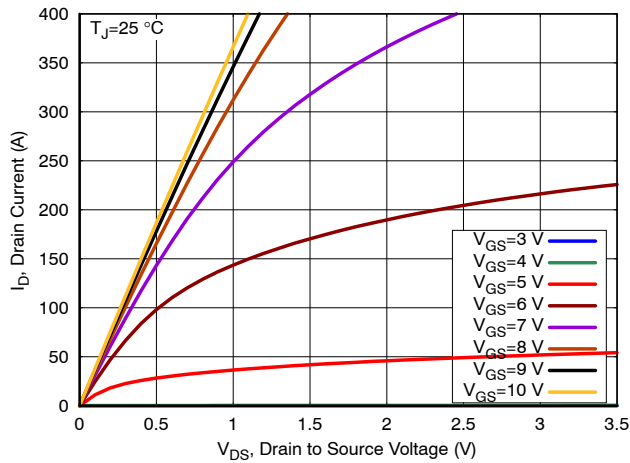


Figure 1. On-Region Characteristics

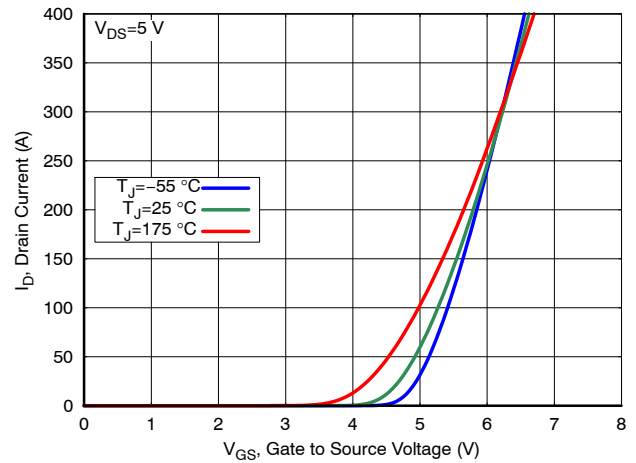


Figure 2. Transfer Characteristics

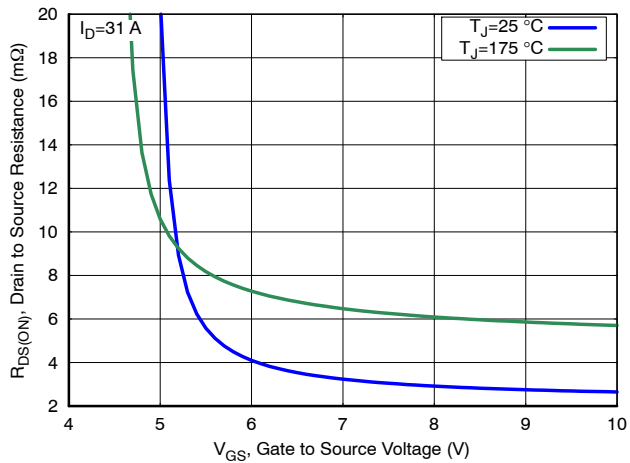


Figure 3. On-Resistance vs. Gate Voltage

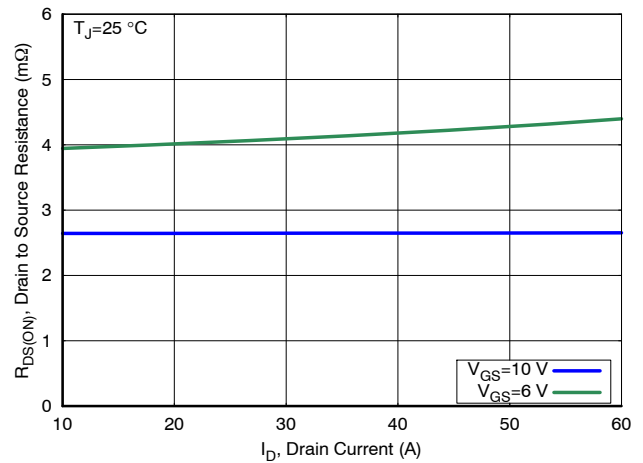


Figure 4. On-Resistance vs. Drain Current

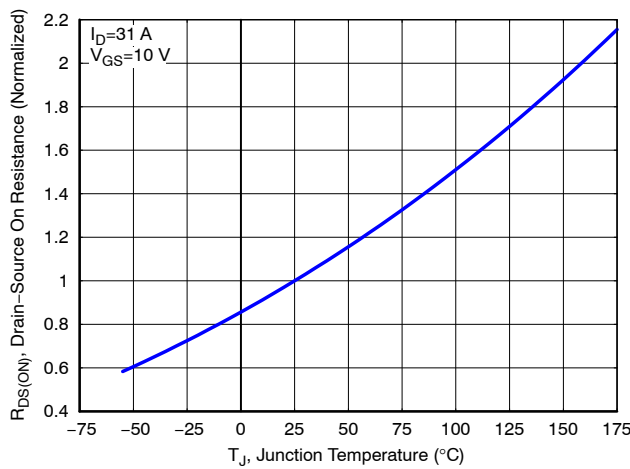


Figure 5. Normalized ON Resistance vs. Junction Temperature

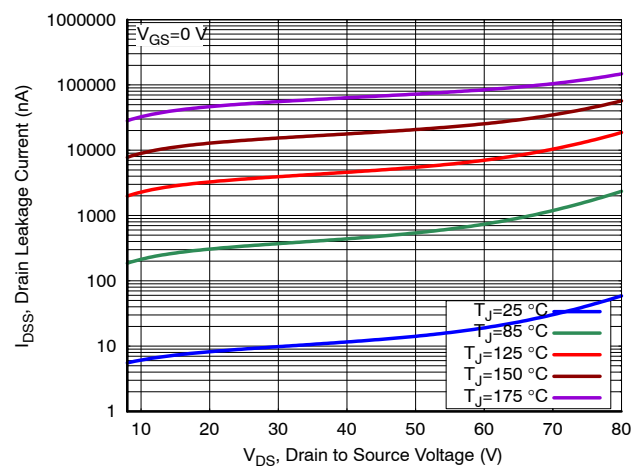


Figure 6. Drain Leakage Current vs. Drain Voltage

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TYPICAL CHARACTERISTICS

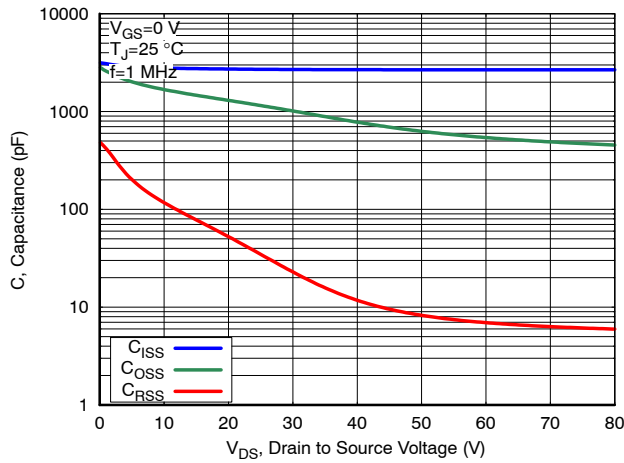


Figure 7. Capacitance Characteristics

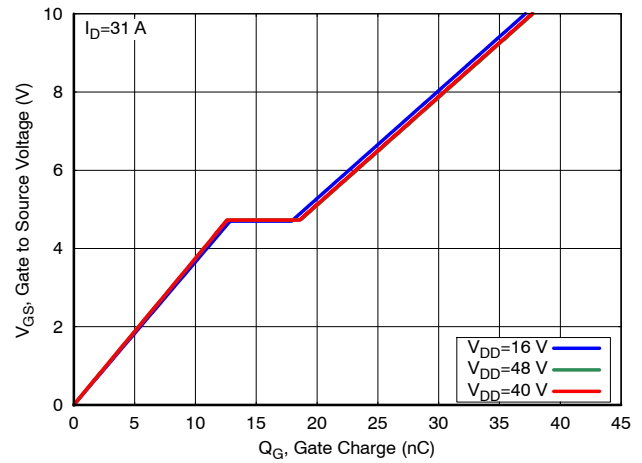


Figure 8. Gate Charge Characteristics

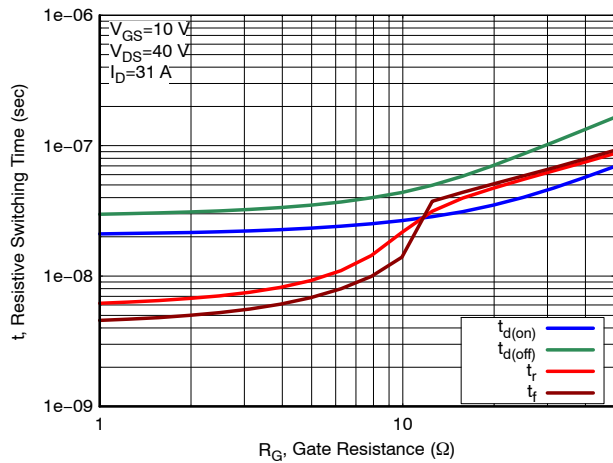


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

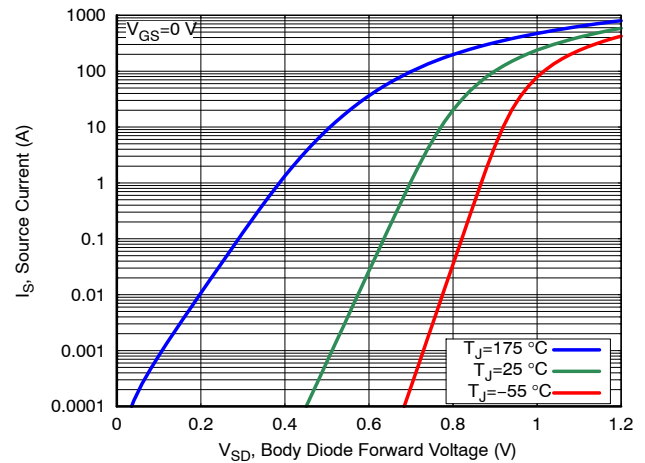


Figure 10. Diode Forward Characteristics

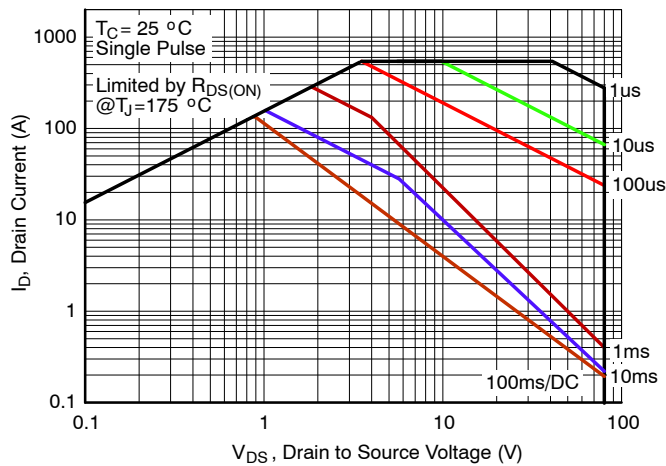


Figure 11. Safe Operating Area (SOA)

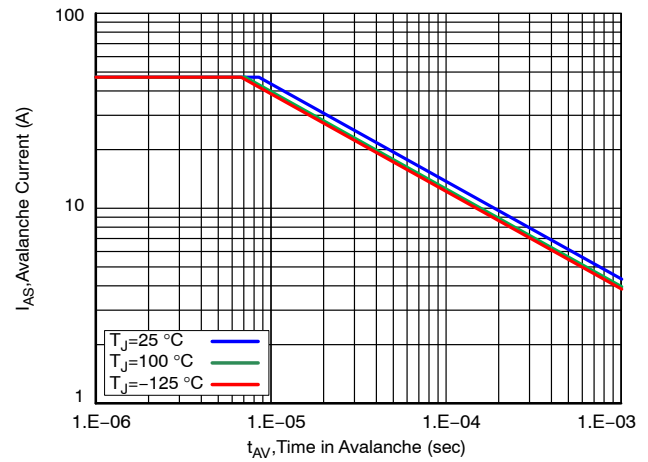


Figure 12. Avalanche Current vs Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

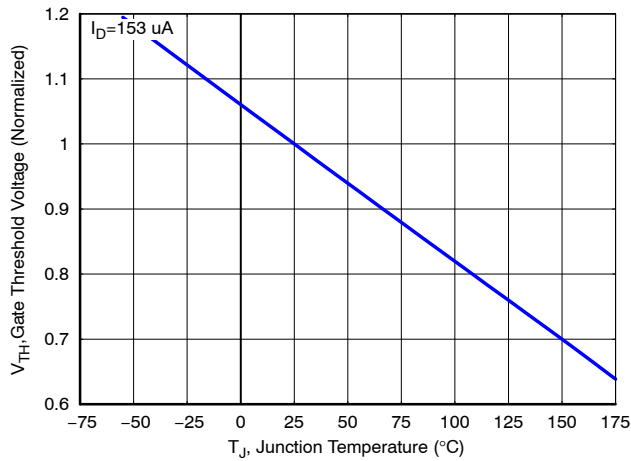


Figure 13. Gate Threshold Voltage vs Junction Temperature

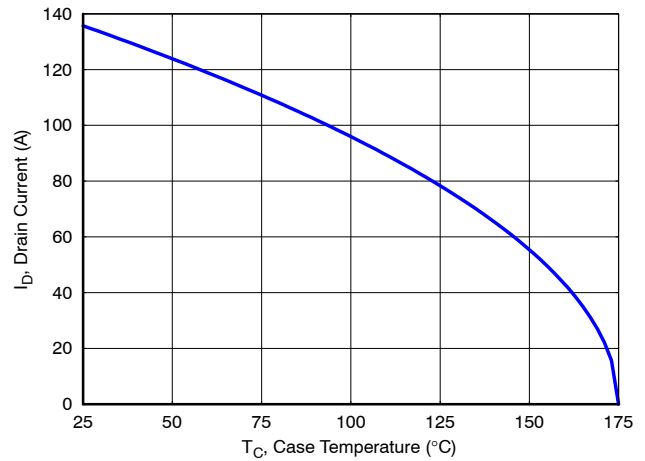


Figure 14. Maximum Current vs. Case Temperature

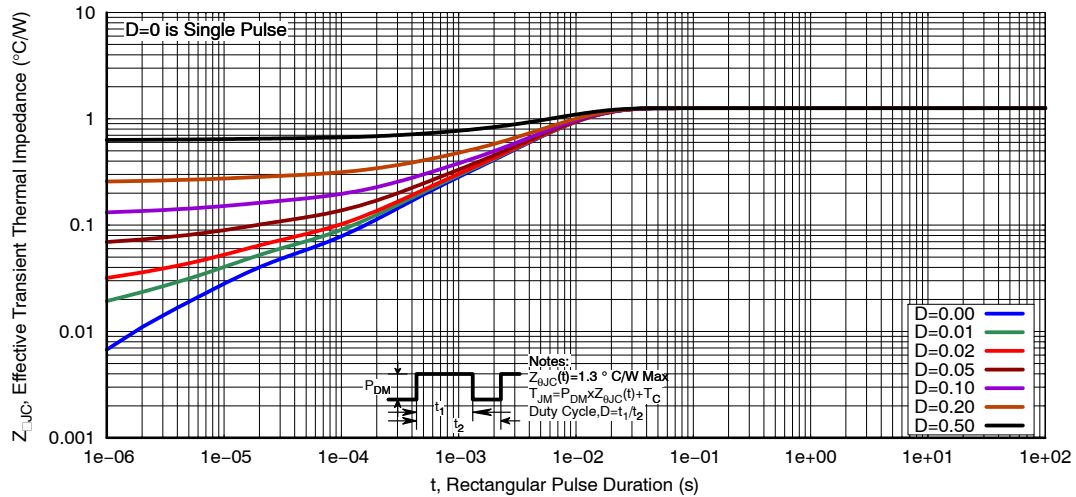


Figure 15. Transient Thermal Response

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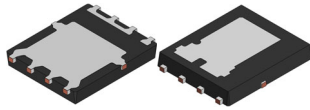
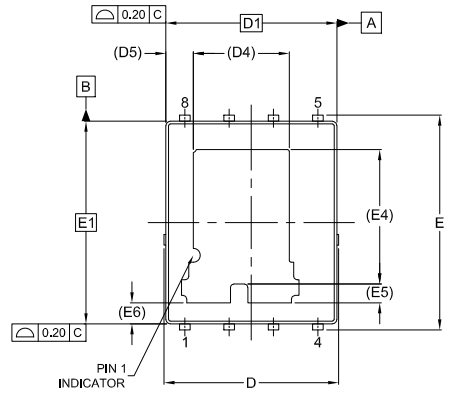
REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary Document release.	4/27/2026
P1	Maximum Ratings, Thermal Characteristics and Electrical Characteristics tables updated, Typical Characteristics figures added.	5/25/2026

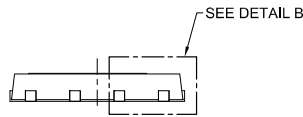
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PACKAGE DIMENSIONS

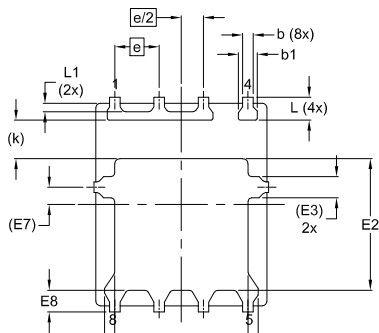
DFN8 4.90x5.80x0.80, 1.27P
CASE 506EA
ISSUE O



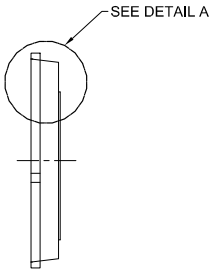
TOP VIEW



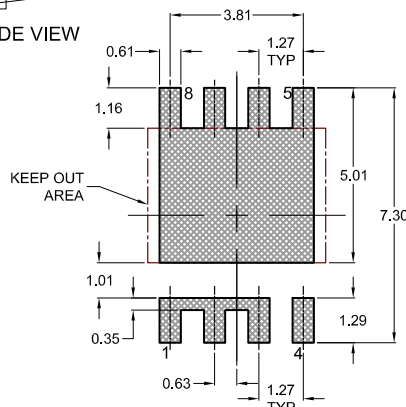
FRONT VIEW



BOTTOM VIEW

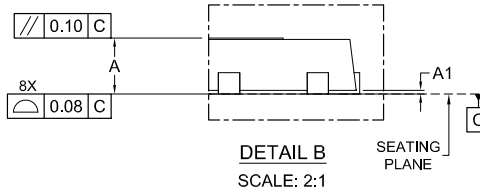


SIDE VIEW



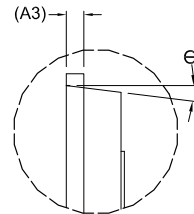
LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ONSEMI SOLDERING
AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D.



DETAIL B
SCALE: 2:1

SEATING
PLANE



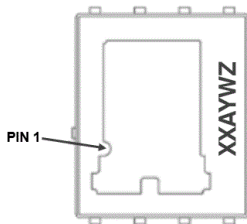
DETAIL A
SCALE: 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.75	0.80	0.85
A1	-	-	0.05
A3	0.25 REF		
b	0.21	0.31	0.41
b1	0.44	0.54	0.64
D	4.90	5.00	5.10
D1	4.90 BSC		
D2	3.72	3.82	3.92
D3	4.30	4.40	4.50
D4	2.75 REF		
D5	0.79 REF		
E	6.05	6.15	6.25
E1	5.80 BSC		
E2	3.67	3.77	3.87
E3	0.60 REF		
E4	3.85 REF		
E5	0.54 REF		
E6	0.60 REF		
E7	0.50 REF		
E8	0.52	0.62	0.72
e	1.27 BSC		
e/2	0.635BSC		
k	1.10 REF		
L	0.56	0.66	0.76
L1	0.15	0.25	0.35
Θ	0°	---	7°

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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