

MOSFET - Power, Single N-Channel, SUPERFET[®], EASY, PQFN88-4L

600 V, 80 mΩ, 40 A NTMT080N60S5

Description

SUPERFET V MOSFET Easy Drive series combines excellent switching performance without sacrificing ease of use and EMI issues for both hard and soft switching topologies. The Power88 package which is an ultraslim SMD package offers excellent switching performance by providing kelvin source configuration and lower parasitic source inductance.

Features

- 650 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 64\text{ m}\Omega$
- 100% Avalanche Tested
- Pb-Free, Halogen Free / BFR Free and are RoHS Compliant

Applications

- Telecom / Server Power Supplies
- EV Charger / UPS / Solar / Industrial Power Supplies

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, Unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	600	V
Gate-to-Source Voltage	V_{GS}	DC	± 30
		AC ($f > 1\text{ Hz}$)	± 30
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	40
		$T_C = 100^\circ\text{C}$	25
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	212
Pulsed Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_{DM}	116
Pulsed Source Current (Body Diode) (Note 1)		I_{SM}	116
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	40	A
Single Pulse Avalanche Energy	$I_L = 5.8\text{ A}$ $R_G = 25\ \Omega$	E_{AS}	287
Avalanche Current		I_{AS}	5.8
Repetitive Avalanche Energy (Note 1)	E_{AR}	2.12	mJ
MOSFET dv/dt	dv/dt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)		50	
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)	T_L	260	$^\circ\text{C}$

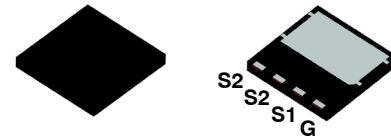
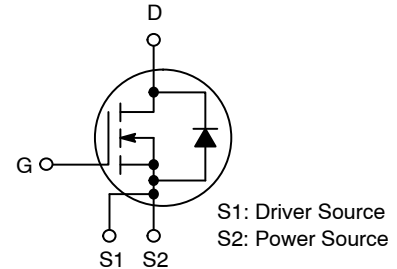
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{SD} \leq 16.5\text{ A}$, $di/dt \leq 200\text{ A/s}$, $V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$.

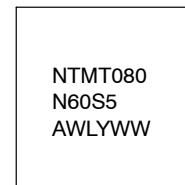
$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
600 V	80 mΩ @ $V_{GS} = 10\text{ V}$	40 A

N-CHANNEL MOSFET



TDFN4 8x8 2P
CASE 520AB

MARKING DIAGRAM



NTMT080N60S5 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping [†]
NTMT080N60S5	TDFN4	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMT080N60S5

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.59	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	45	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	600	-	-	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 10\text{ mA}$, Referenced to 25°C	-	630	-	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_J = 25^\circ\text{C}$	-	-	2	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	±100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 16.5\text{ A}, T_J = 25^\circ\text{C}$	-	64	80	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 3.4\text{ mA}, T_J = 25^\circ\text{C}$	2.4	-	4	V
Forward Trans-conductance	g_{FS}	$V_{DS} = 20\text{ V}, I_D = 16.5\text{ A}$	-	28.8	-	S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 250\text{ kHz}$	-	3029	-	pF
Output Capacitance	C_{OSS}		-	47.1	-	
Time Related Output Capacitance	$C_{OSS(tr)}$	$I_D = \text{Constant}, V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	746	-	
Energy Related Output Capacitance	$C_{OSS(er)}$		$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	83.8	
Total Gate Charge	$Q_{G(tot)}$	$V_{DD} = 400\text{ V}, I_D = 16.5\text{ A}, V_{GS} = 10\text{ V}$	-	56.2	-	nC
Gate-to-Source Charge	Q_{GS}		-	14.8	-	
Gate-to-Drain Charge	Q_{GD}		-	16.3	-	
Gate Resistance	R_G		$f = 1\text{ MHz}$	-	5.66	

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 0/10\text{ V}, V_{DD} = 400\text{ V}, I_D = 16.5\text{ A}, R_G = 4.7\text{ }\Omega$	-	29.4	-	ns
Rise Time	t_r		-	11.4	-	
Turn-Off Delay Time	$t_{d(off)}$		-	88.2	-	
Fall Time	t_f		-	3.62	-	

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_{SD} = 16.5\text{ A}, T_J = 25^\circ\text{C}$	-	-	1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_{SD} = 16.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 400\text{ V}$	-	338	-	ns
Reverse Recovery Charge	Q_{RR}		-	5167	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NTMT080N60S5

TYPICAL CHARACTERISTICS

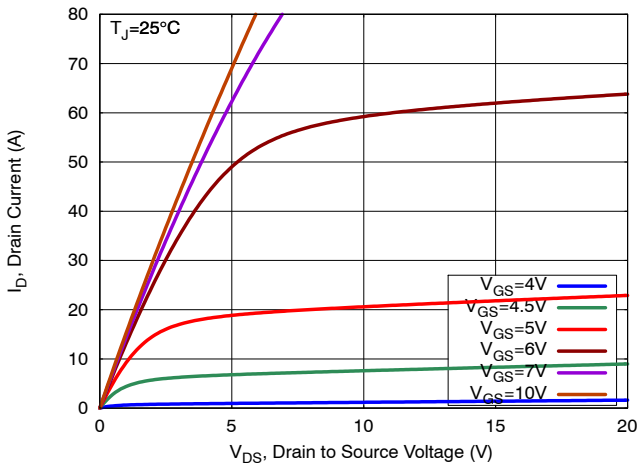


Figure 1. On-Region Characteristics

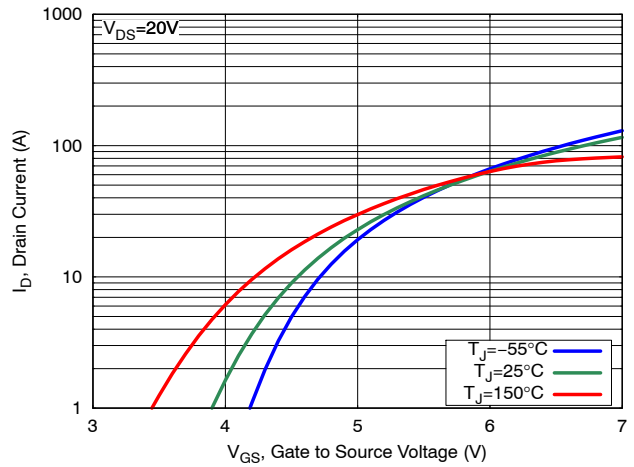


Figure 2. Transfer Characteristics

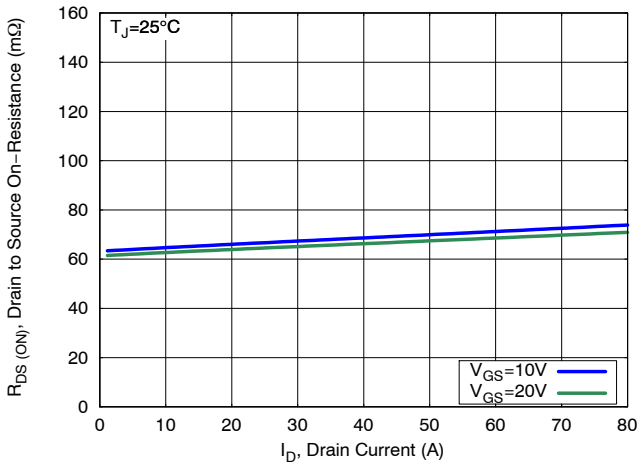


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

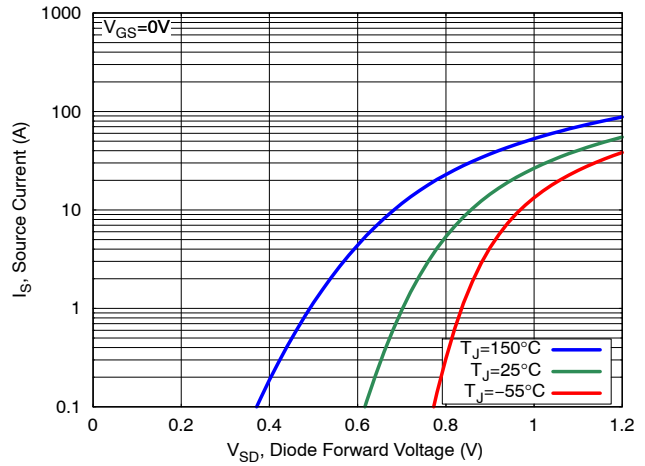


Figure 4. Diode Forward Voltage vs. Source Current

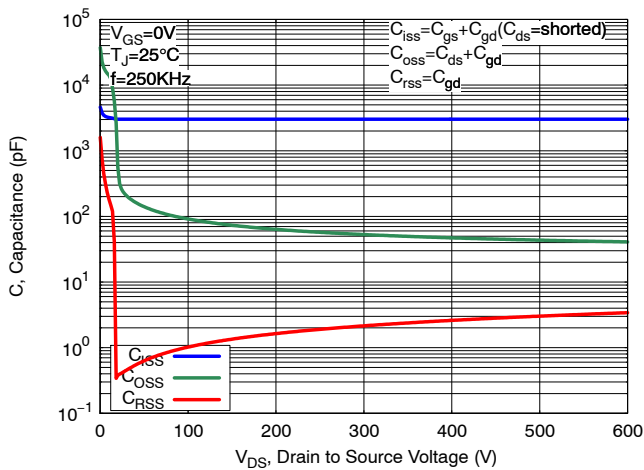


Figure 5. Capacitance Characteristics

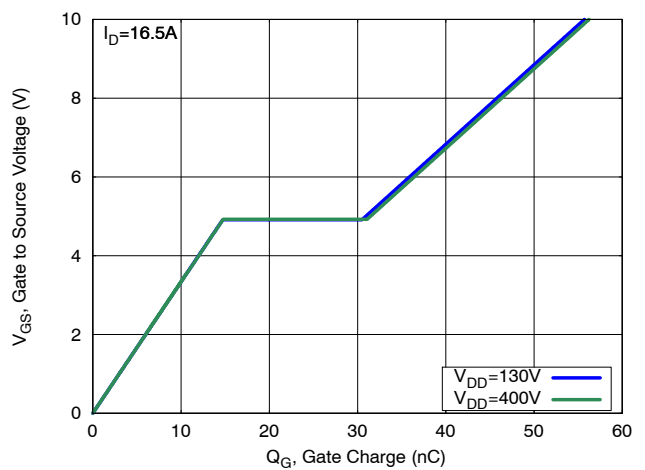


Figure 6. Gate Charge Characteristics

NTMT080N60S5

TYPICAL CHARACTERISTICS

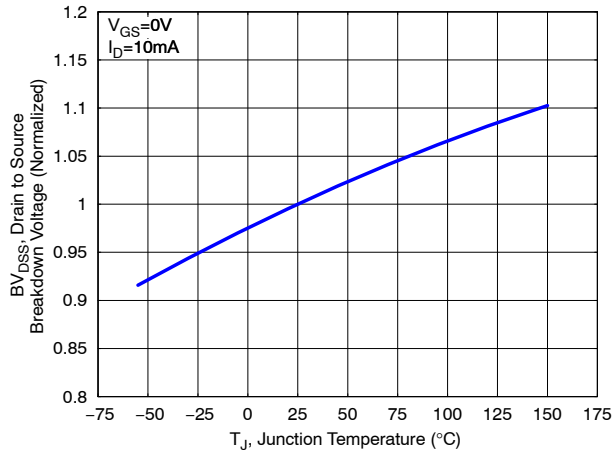


Figure 8. Breakdown Voltage Variation vs. Temperature

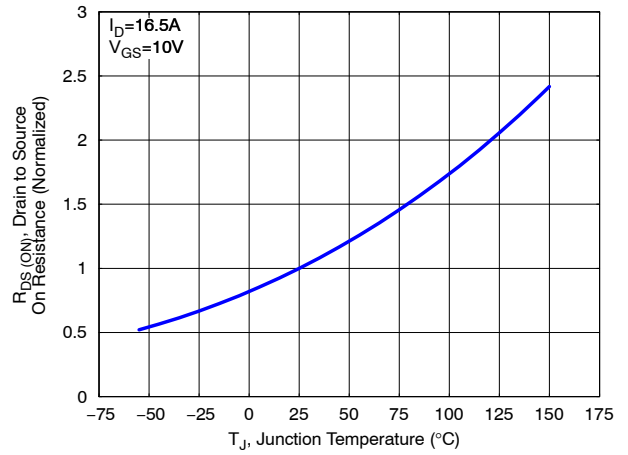


Figure 7. On-Resistance Variation vs. Temperature

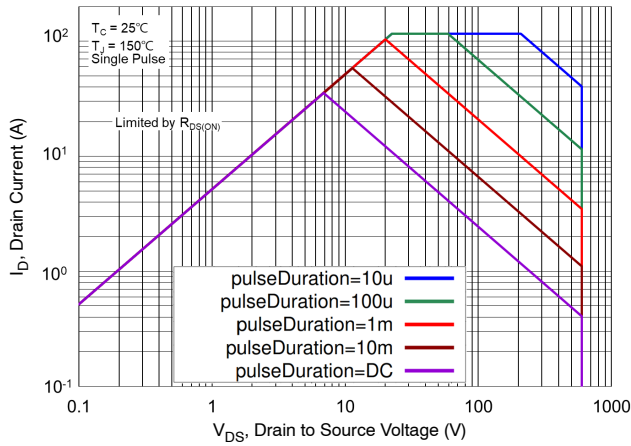


Figure 9. Maximum Safe Operating Area

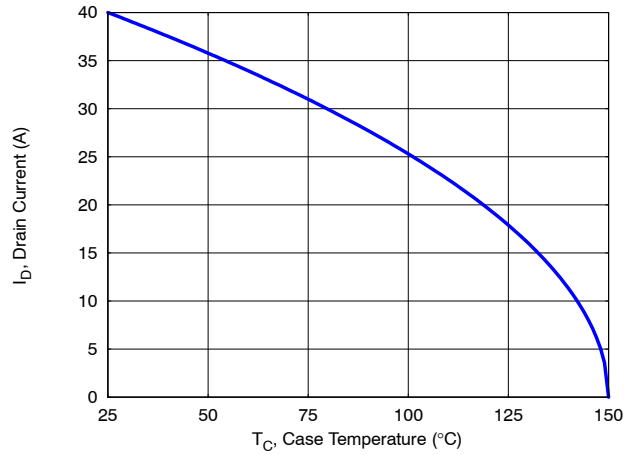


Figure 10. Maximum Drain Current vs. Case Temperature

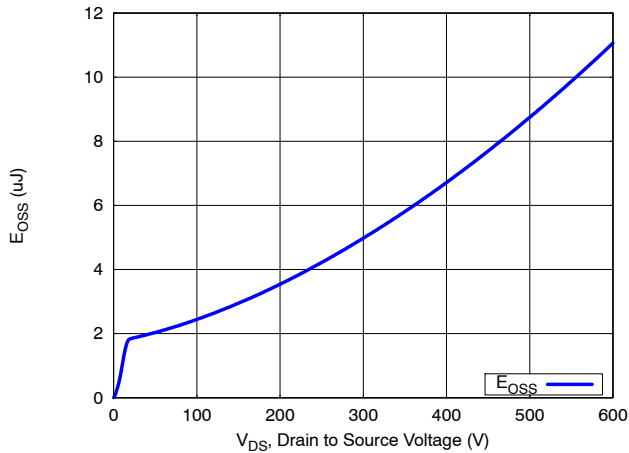


Figure 11. E_{oss} vs. Drain-to-Source Voltage

NTMT080N60S5

TYPICAL CHARACTERISTICS

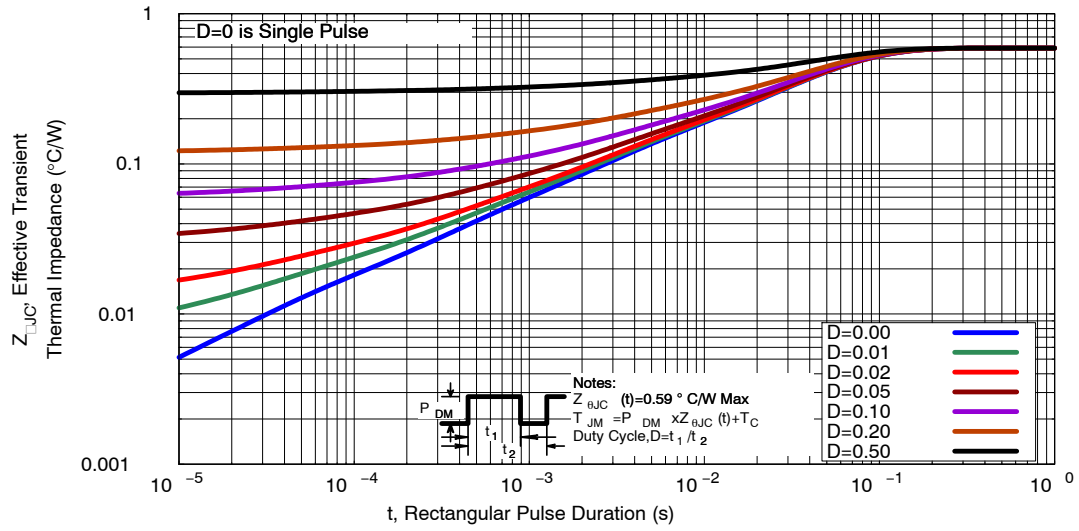
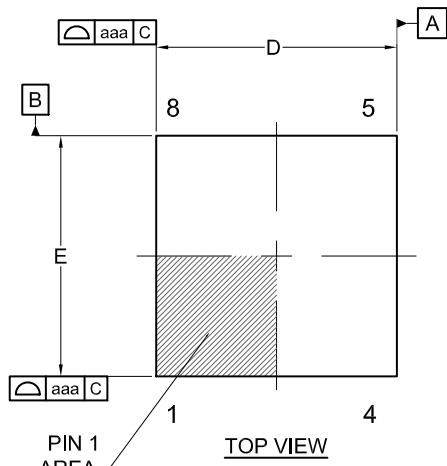


Figure 12. Transient Thermal Impedance

NTMT080N60S5

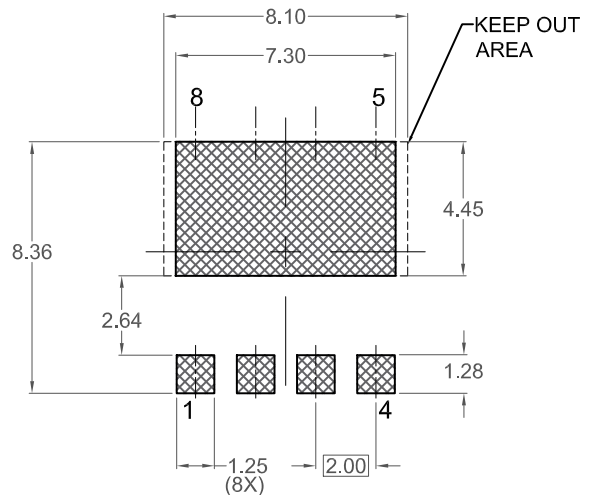
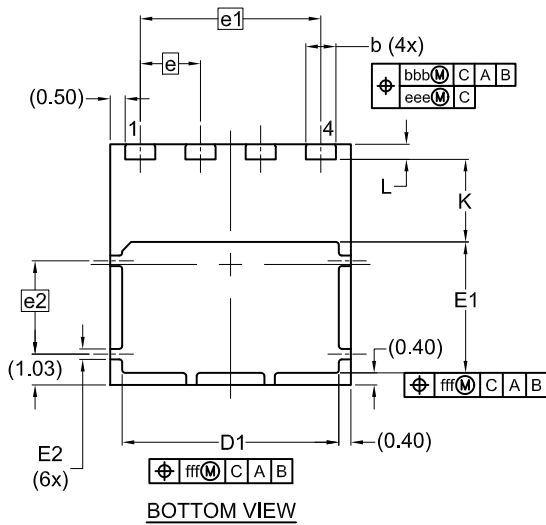
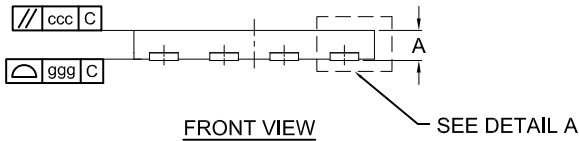
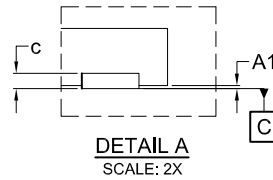
PACKAGE DIMENSIONS

TDFN4 8x8, 2P
CASE 520AB
ISSUE O



- NOTES: UNLESS OTHERWISE SPECIFIED
 A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 D) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.90	1.00	1.10
c	0.10	0.20	0.30
D	7.90	8.00	8.10
D1	7.10	7.20	7.30
E	7.90	8.00	8.10
E1	4.25	4.35	4.45
E2	0.15	0.25	0.35
e	2.00 BSC		
e1	6.00 BSC		
e2	3.10 BSC		
K	(2.75)		
L	0.40	0.50	0.60
aaa	0.10		
bbb	0.10		
ccc	0.05		
eee	0.05		
fff	0.10		
ggg	0.15		



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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