

MOSFET - Power, Single N-Channel, TDFNW8 100 V, 4.2 mΩ, 178 A NTMTSC4D2N10GTXG

Features

- Wide SOA for Linear Mode Operation
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- High Peak UIS Current Capability for Ruggedness
- Small Footprint (8x8 mm) & Top Metal Cooling
- These Devices are Pb-Free, Halogen-Free / BFR-Free and are RoHS Compliant

Typical Applications

- 48 V Hot Swap System, Load Switch, Soft-Start, E-Fuse

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	100	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	I_D	$T_C = 25^\circ\text{C}$	178
		$T_C = 100^\circ\text{C}$	
Power Dissipation $R_{\theta JC}$ (Note 2)	P_D	$T_C = 25^\circ\text{C}$	267
		$T_C = 100^\circ\text{C}$	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	I_D	$T_A = 25^\circ\text{C}$	21
		$T_A = 100^\circ\text{C}$	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	P_D	$T_A = 25^\circ\text{C}$	3.9
		$T_A = 100^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	2558
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to $+175$	$^\circ\text{C}$
Source Current (Body Diode)	I_S	222	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 100 \text{ A}, L = 0.1 \text{ mH}$)	E_{AS}	506	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

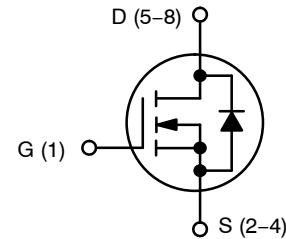
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

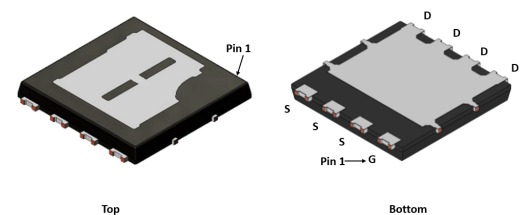
Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	$R_{\theta JC}$	0.56	$^\circ\text{C}/\text{W}$
Junction-to-Top Source - Steady State (Note 2)	$R_{\theta JC}$	0.86	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	38	

1. Surface-mounted on FR4 board using a 1 in², 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	4.2 mΩ @ 10 V	178 A

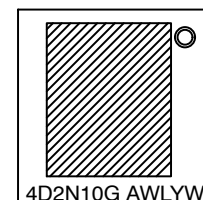


N-CHANNEL MOSFET



TDFNW8
DUAL COOL
CASE 507AS

MARKING DIAGRAM



4D2N10G = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NTMTSC4D2N10GTXG

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = 250 μA, ref to 25°C		84.1		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 80 V	T _J = 25°C		1.0	μA
			T _J = 150°C		100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 450 μA	2.0		4.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = 450 μA, ref to 25°C		-9.24		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 88 A		2.9	4.2	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 88 A		61		S
Gate Resistance	R _G	T _A = 25°C		0.9		Ω

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 50 V		10450		pF
Output Capacitance	C _{OSS}			1050		
Reverse Transfer Capacitance	C _{RSS}			158		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 50 V; I _D = 88 A		159		nC
Threshold Gate Charge	Q _{G(TH)}			27.7		
Gate-to-Source Charge	Q _{GS}			61		
Gate-to-Drain Charge	Q _{GD}			38		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 50 V, I _D = 88 A, R _G = 4.7 Ω		40		ns
Rise Time	t _r			36		
Turn-Off Delay Time	t _{d(OFF)}			76		
Fall Time	t _f			26		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 88 A	T _J = 25°C		0.82	1.2	V
			T _J = 125°C		0.70		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 300 A/μs, I _S = 44 A		46.7			ns
Reverse Recovery Charge	Q _{RR}			224			nC
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 1000 A/μs, I _S = 44 A		46.1			ns
Reverse Recovery Charge	Q _{RR}			595			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

NTMTSC4D2N10GTXG

TYPICAL CHARACTERISTICS

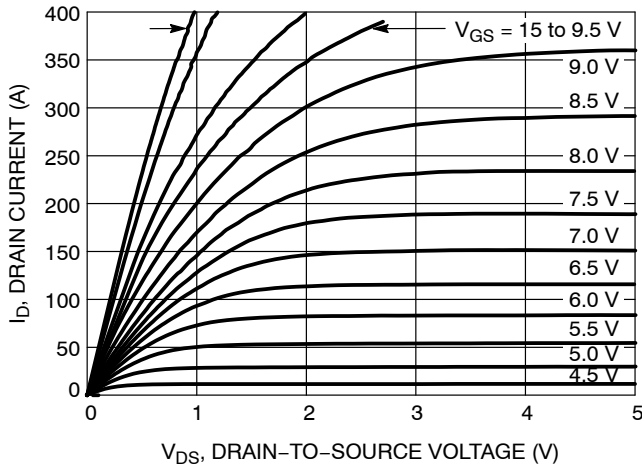


Figure 1. On-Region Characteristics

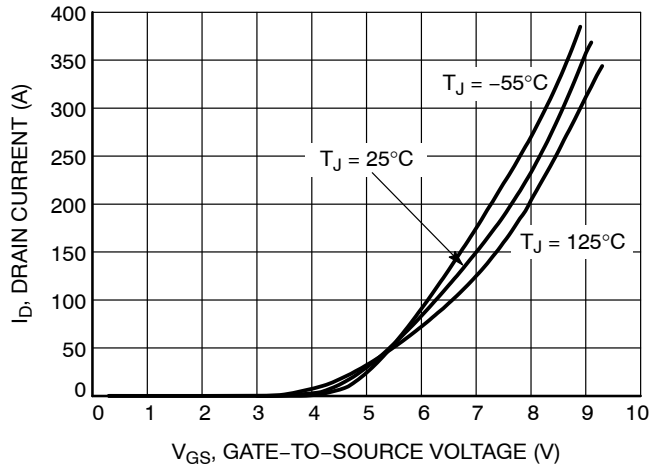


Figure 2. Transfer Characteristics

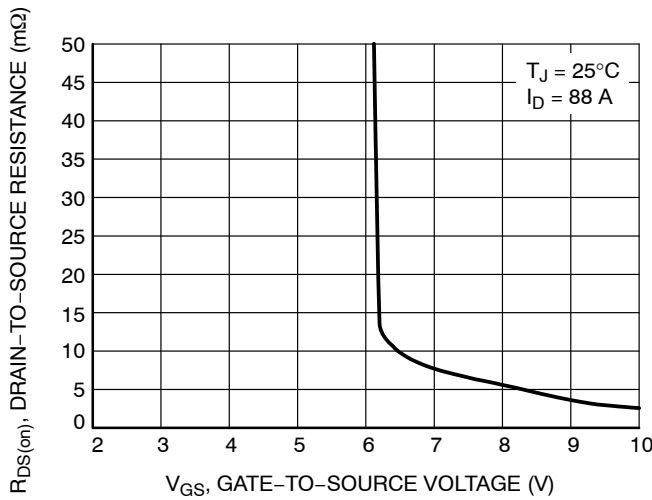


Figure 3. On-Resistance vs. Gate-to-Source Voltage

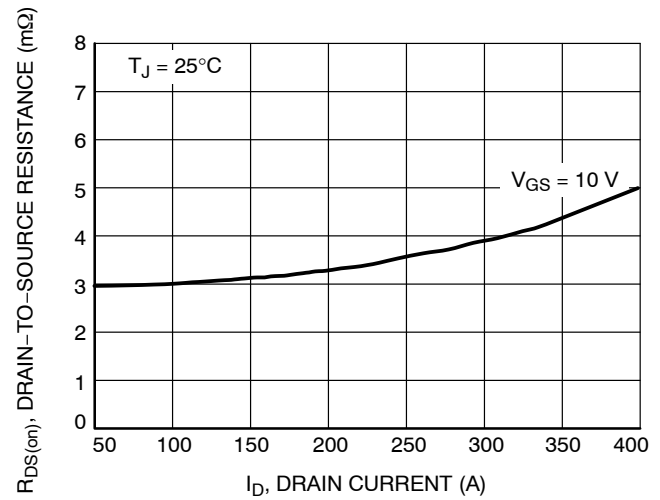


Figure 4. On-Resistance vs. Drain Current

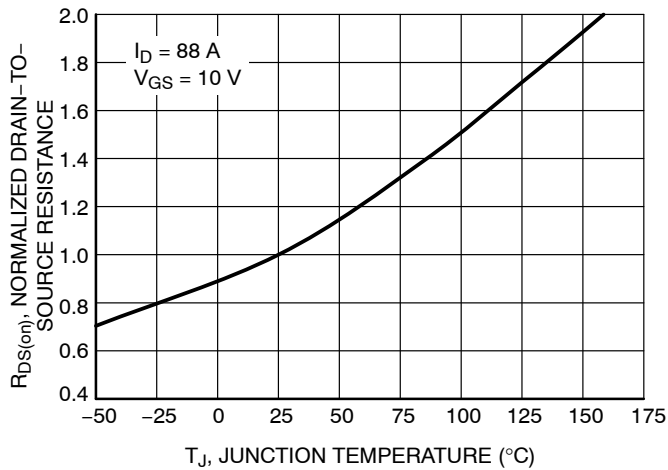


Figure 5. On-Resistance Variation with Temperature

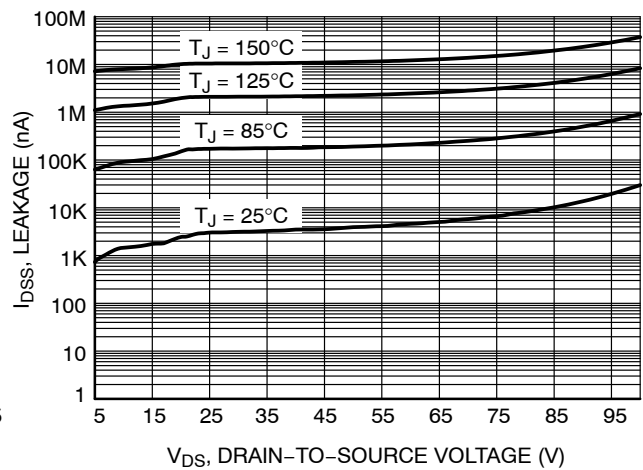


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

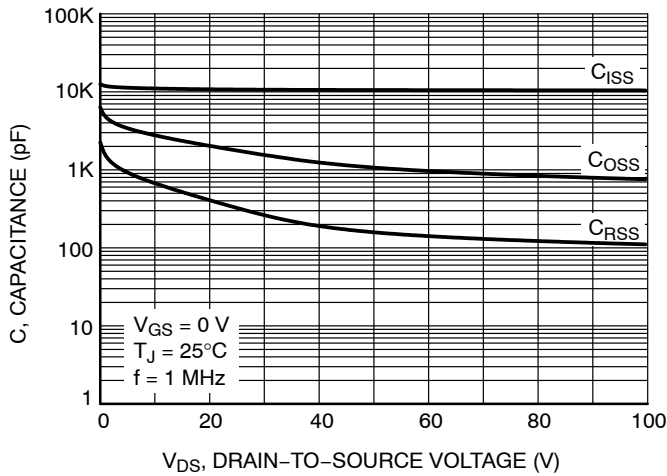


Figure 7. Capacitance Variation

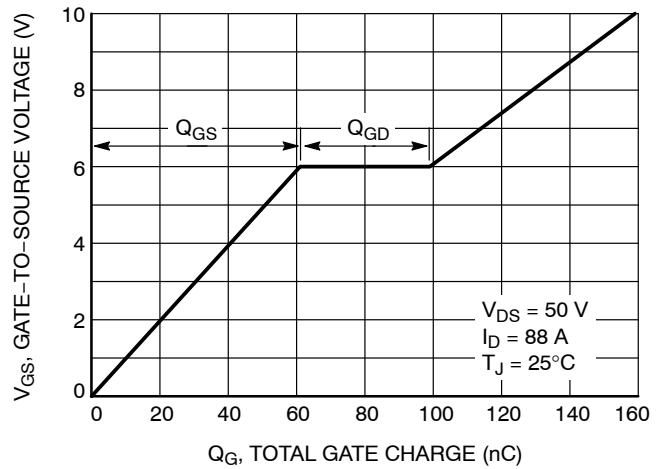


Figure 8. Gate-to-Source Voltage vs. Total Charge

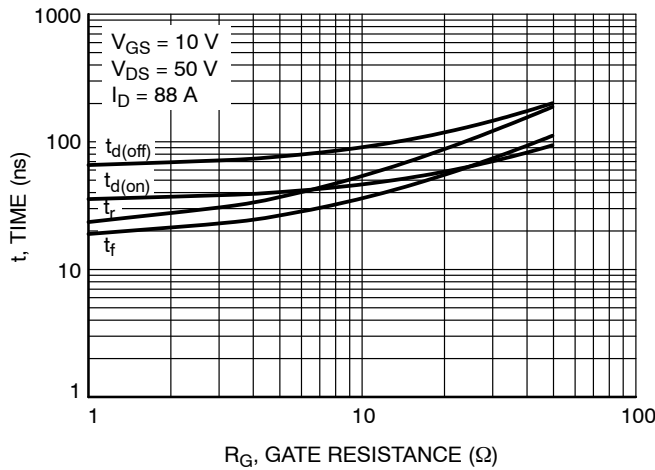


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

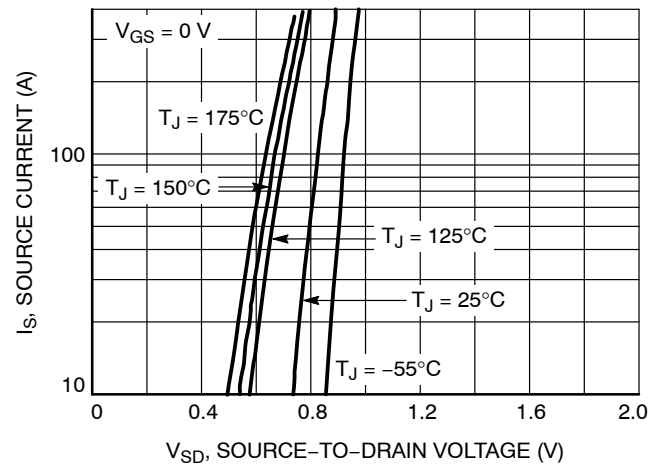


Figure 10. Diode Forward Voltage vs. Current

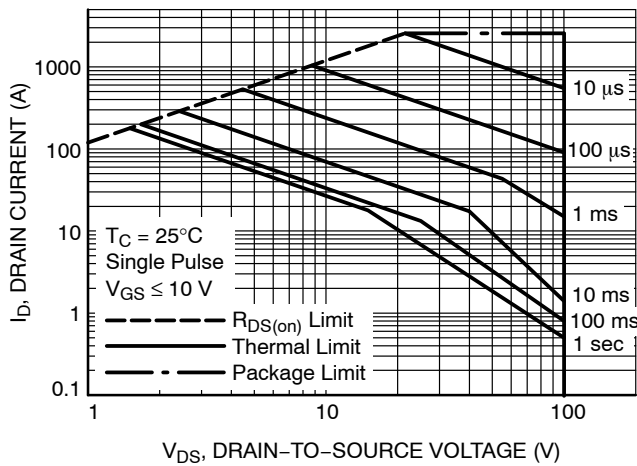


Figure 11. Maximum Rated Forward Biased Safe Operating Area

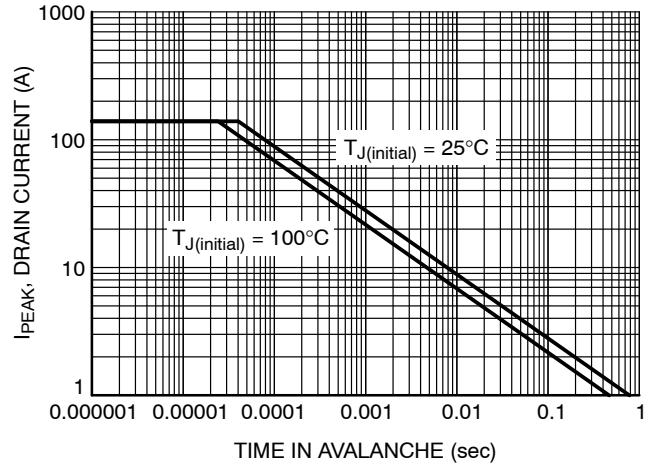


Figure 12. Maximum Drain Current vs. Time in Avalanche

NTMTSC4D2N10GTXG

TYPICAL CHARACTERISTICS

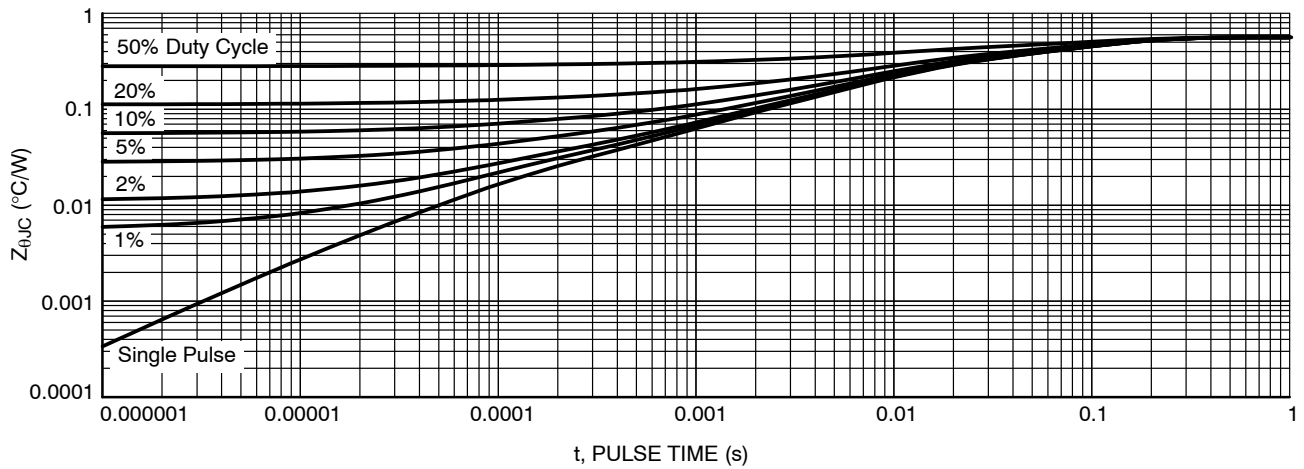
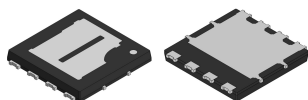


Figure 13. Junction-to-Ambient Transient Thermal Response

DEVICE ORDERING INFORMATION

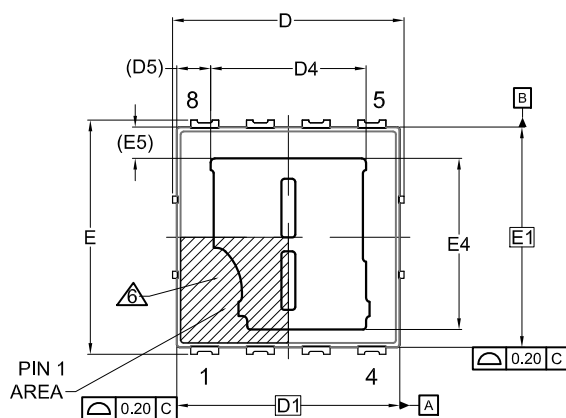
Device	Marking	Package	Shipping [†]
NTMTSC4D2N10GTXG	4D2N10G	TDFNW8 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



TDFNW8 8.30x8.40x0.92, 2.00P
CASE 507AS
ISSUE C

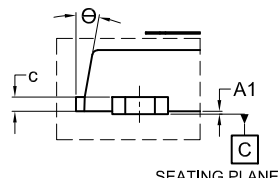
DATE 28 MAY 2024



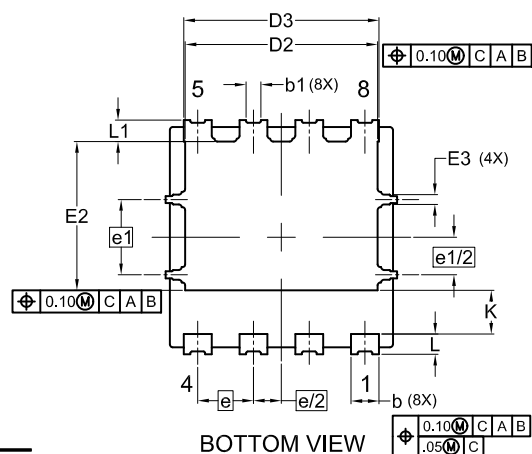
TOP VIEW



SEE DETAIL A FRONT VIEW



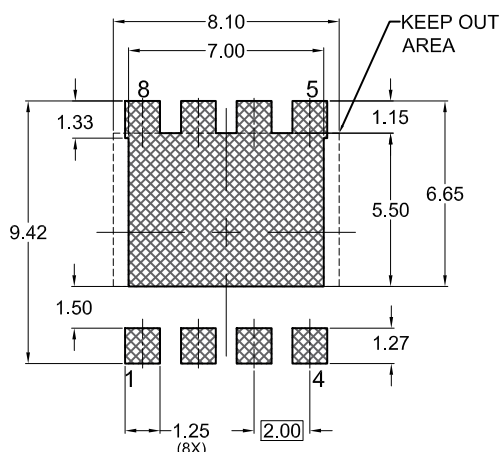
DETAIL A
(SCALE: 2X)



BOTTOM VIEW

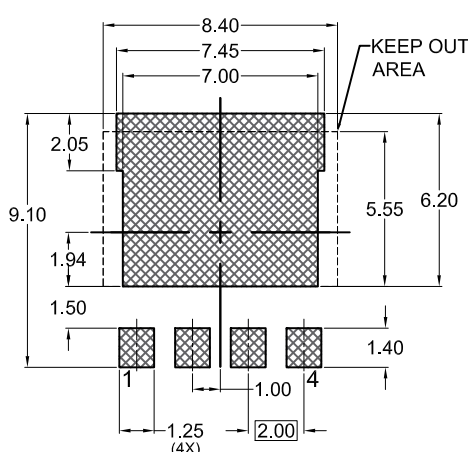
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS.
 "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. SLOT PARTITION IS OPTIONAL.



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL. SOLDERRM/D.



UNIVERSAL LAND PATTERN*

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.82	0.92	1.02
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	8.00 BSC		
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
D4	5.52	5.67	5.82
D5	1.16 REF		
E	8.30	8.40	8.50
E1	7.90 BSC		
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
E4	6.08	6.23	6.38
E5	1.13 REF		
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Ø	0°	—	12°

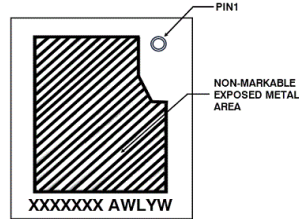
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TDFNW8 8.30x8.40x0.92, 2.00P
CASE 507AS
ISSUE C

DATE 28 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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