# MOSFET - Symmetrical Dual N-Channel

## 80 V, 18 mΩ, 26 A

# NTTFD018N08LC

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 80 V | 18 mΩ @ 10 V | 26 A |
| | 29 mΩ @ 4.5 V | |

### General Description

This device includes two specialized N−Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q2) and synchronous (Q1) have been designed to provide optimal power efficiency.

### Features

Q1: N−Channel

- Max $r_{DS(on)}$ = 18 mΩ at $V_{GS}$ = 10 V, $I_D$ = 7.8 A
- Max $r_{DS(on)}$ = 29 mΩ at $V_{GS}$ = 4.5, $I_D$ = 6.2 A

Q2: N−Channel

- Max $r_{DS(on)}$ = 18 mΩ at $V_{GS}$ = 10 V, $I_D$ = 7.8 A
- Max $r_{DS(on)}$ = 29 mΩ at $V_{GS}$ = 4.5, $I_D$ = 6.2 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- RoHS Compliant

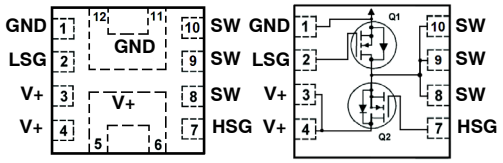
### Typical Applications

- 48 V Input Primary Half Bridge
- Communications
- General Purpose Point of Load

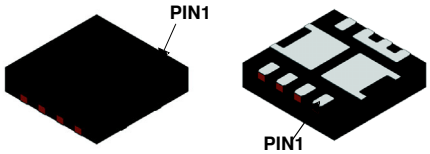
### PIN DESCRIPTION

| Pin | Name | Description |
|---|---|---|
| 1, 11, 12 | GND (LSS) | Low Side Source |
| 2 | LSG | Low Side Gate |
| 3, 4, 5, 6 | V + (HSD) | High Side Drain |
| 7 | HSG | High Side Gate |
| 8, 9, 10 | SW | Switching Node, Low Side Drain |

### ELECTRICAL CONNECTION

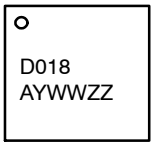



**Dual N-Channel MOSFET**




**Power Clip 33 Symmetric (WQFN12)**
**CASE 510CJ**

### MARKING DIAGRAM




D018 = Specific Device Code
A = Assembly Plant Code
Y = Numeric Year Code
WW = Work Week Code
ZZ = Assembly Lot Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

## ORDERING INFORMATION AND PACKAGE MARKING

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| NTTFD018N08LC | D018 | WQFN12<br>(Pb−Free) | 3000 Units/<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MOSFET MAXIMUM RATINGS ($T_A$ = 25°C, Unless otherwise specified)

| Symbol | Parameter | | | | Q1 | Q2 | Units |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | | 80 | 80 | V |
| $V_{GS}$ | Gate to Source Voltage | | | | ±20 | ±20 | V |
| $I_D$ | Drain Current | −Continuous | $T_C$ = 25°C | (Note 4) | 26 | 26 | A |
| | | −Continuous | $T_C$ = 100°C | (Note 4) | 16 | 16 | |
| | | −Continuous | $T_A$ = 25°C | | 6 (Note 1a) | 6 (Note 1b) | |
| | | −Pulsed | $T_A$ = 25°C | | 349 | 349 | |
| $E_{AS}$ | Single Pulse Avalanche Energy (L = 1 mH, $I_{L(pk)}$ = 8 A) | | | (Note 3) | 32 | 32 | mJ |
| $P_D$ | Power Dissipation for Single Operation | | $T_C$ = 25°C | | 26 | 26 | W |
| | Power Dissipation for Single Operation | | $T_A$ = 25°C | | 1.7 (Note 1a) | 1.7 (Note 1b) | |
| $I_S$ | Source Current (Body Diode) | | | | 21 | 21 | A |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | | −55 to +150 | | °C |
| $T_L$ | Lead Temperature for Soldering Purposes (1/8” from case for 10 s) | | | | 260 | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

| Symbol | Parameter | Q1 | Q2 | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 4.8 | 4.8 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 70 (Note 1a) | 70 (Note 1b) | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 135 (Note 1c) | 135 (Note 1c) | |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Type | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | Q1 | 80 | | | V |
| | | $I_D$ = 250 μA, $V_{GS}$ = 0 V | Q2 | 80 | | | |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | Q1 | | 76.81 | | mV/°C |
| | | $I_D$ = 250 μA, referenced to 25°C | Q2 | | 76.81 | | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 64 V, $V_{GS}$ = 0 V | Q1 | | | 1 | μA |
| | | $V_{DS}$ = 64 V, $V_{GS}$ = 0 V | Q2 | | | 1 | |
| $I_{GSS}$ | Gate to Source Leakage Current, Forward | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | Q1 | | | ±100 | μA |
| | | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | Q2 | | | ±100 | |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Type | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| **ON CHARACTERISTICS** | | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 44 μA | Q1 | 1.0 | 1.5 | 2.5 | V |
| | | $V_{GS}$ = $V_{DS}$, $I_D$ = 44 μA | Q2 | 1.0 | 1.5 | 2.5 | |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 44 μA, referenced to 25°C | Q1 | | –5.71 | | mV/°C |
| | | $I_D$ = 44 μA, referenced to 25°C | Q2 | | –5.71 | | |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 7.8 A | Q1 | | 15 | 18 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 6.2 A | | | 22 | 29 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 7.8 A, $T_J$ = 125°C | | | 25 | | |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 7.8 A | Q2 | | 15 | 18 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 6.2 A | | | 22 | 29 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 7.8 A, $T_J$ = 125°C | | | 25 | | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 7.8 A | Q1 | | 23 | | S |
| | | $V_{DS}$ = 5 V, $I_D$ = 7.8 A | Q2 | | 23 | | |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $C_{ISS}$ | Input Capacitance | Q1: $V_{DS}$ = 40 V, $V_{GS}$ = 0 V, f = 1 Mhz | Q1 | | 856 | | pF |
| | | | Q2 | | 856 | | |
| $C_{OSS}$ | Output Capacitance | Q2: $V_{DS}$ = 40 V, $V_{GS}$ = 0 V, f = 1 MHz | Q1 | | 230 | | pF |
| | | | Q2 | | 230 | | |
| $C_{RSS}$ | Reverse Transfer Capacitance | | Q1 | | 10 | | pF |
| | | | Q2 | | 10 | | |
| $R_G$ | Gate Resistance | $T_A$ = 25°C | Q1 | | 0.5 | | Ω |
| | | | Q2 | | 0.5 | | |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| $td_{(ON)}$ | Turn – On Delay Time | Q1: $V_{DD}$ = 40 V, $V_{GS}$ = 4.5 V, $I_D$ = 6.2 A, $R_{GEN}$ = 6 Ω | Q1 | | 9.4 | | ns |
| | | | Q2 | | 9.4 | | |
| $t_r$ | Rise Time | Q2: $V_{DD}$ = 40 V, $V_{GS}$ = 4.5 V, $I_D$ = 6.2 A, $R_{GEN}$ = 6 Ω | Q1 | | 5.8 | | ns |
| | | | Q2 | | 5.8 | | |
| $t_{D(OFF)}$ | Turn – Off Delay Time | | Q1 | | 14.6 | | ns |
| | | | Q2 | | 14.6 | | |
| $t_f$ | Fall Time | | Q1 | | 5.5 | | ns |
| | | | Q2 | | 5.5 | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0V to 10 V | Q1 | | 12.4 | | nC |
| | | | Q2 | | 12.4 | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0V to 4.5 V | Q1 | | 6.0 | | nC |
| | | | Q2 | | 6.0 | | |
| $Q_{gs}$ | Gate to Source Gate Charge | Q1: $V_{DD}$ = 40 V, $I_D$ = 6.2 A | Q1 | | 1.94 | | nC |
| | | Q2: $V_{DD}$ = 40 V, $I_D$ = 6.2 A | Q2 | | 1.94 | | |
| $Q_{gd}$ | Gate to Drain ”Miller” Charge | | Q1 | | 1.71 | | nC |
| | | | Q2 | | 1.71 | | |

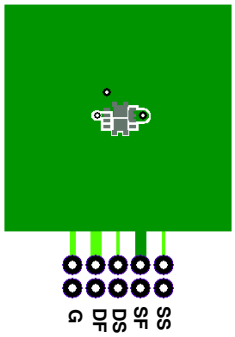
**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Type | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 7.8 A (Note 2) | Q1 | | 0.82 | 1.5 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 7.8 A (Note 2) | Q2 | | 0.82 | 1.5 | |
| $t_{rr}$ | Reverse Recovery Time | Q1: $I_F$ = 7.8 A, di/dt = 300 A/μs | Q1 | | 13.3 | | ns |
| | | | Q2 | | 13.3 | | |
| $Q_{rr}$ | Reverse Recovery Charge | Q2: $I_F$ = 7.8 A, di/dt = 300 A/μs | Q1 | | 18.1 | | nC |
| | | | Q2 | | 18.1 | | |
| $t_{rr}$ | Reverse Recovery Time | Q1: $I_F$ = 7.8 A, di/dt = 1000 A/μs | Q1 | | 10.3 | | ns |
| | | | Q2 | | 10.3 | | |
| $Q_{rr}$ | Reverse Recovery Charge | Q2: $I_F$ = 7.8 A, di/dt = 1000 A/μs | Q1 | | 51 | | nC |
| | | | Q2 | | 51 | | |

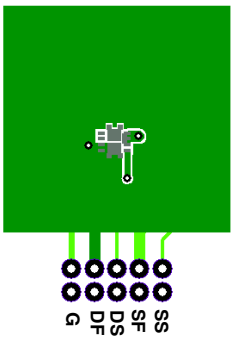
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

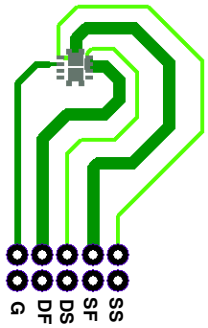
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in$^2$ pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user's board design.



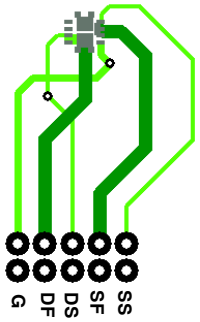

a) 70°C/W when mounted on a 1 in$^2$ pad of 2 oz copper.




b) 70°C/W when mounted on a 1 in$^2$ pad of 2 oz copper.




c) 135°C/W when mounted on a minimum pad of 2 oz copper.




d) 135°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Q1: $E_{AS}$ of 32 mJ is based on starting $T_J$ = 25°C; N−ch: L = 1 mH, $I_{AS}$ = 8 A, $V_{DD}$ = 80 V, $V_{GS}$ = 10 V. 100% test at L = 1 mH, $I_{AS}$ = 8.2 A.
   Q2: $E_{AS}$ of 32 mJ is based on starting $T_J$ = 25°C; N−ch: L = 1 mH, $I_{AS}$ = 8 A, $V_{DD}$ = 80 V, $V_{GS}$ = 10 V. 100% test at L = 1 mH, $I_{AS}$ = 8.2 A.
4. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

## TYPICAL CHARACTERISTICS

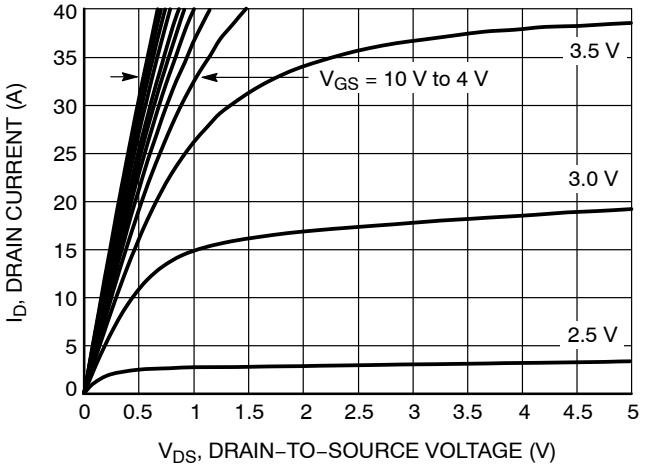



**Figure 1. On−Region Characteristics**

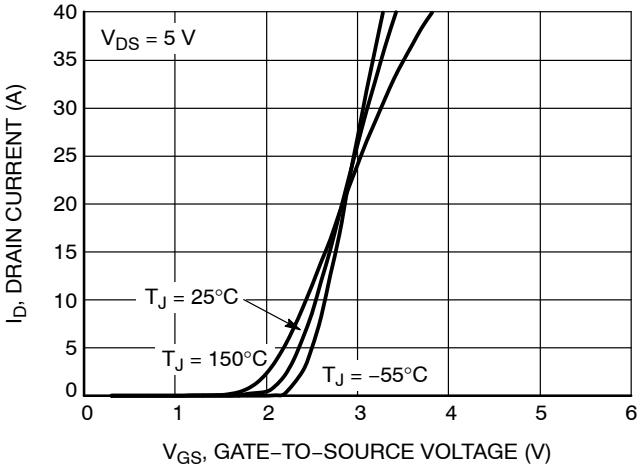



**Figure 2. Transfer Characteristics**

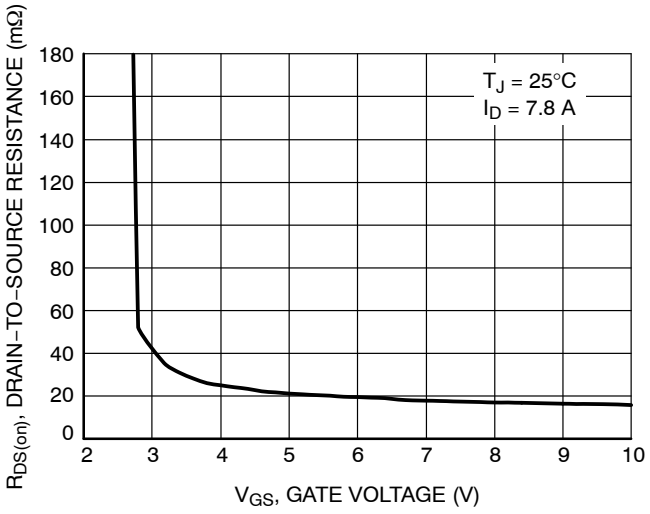



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

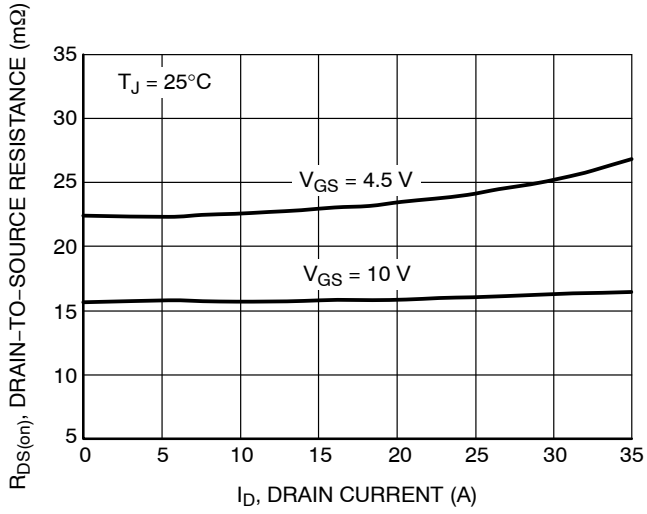



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

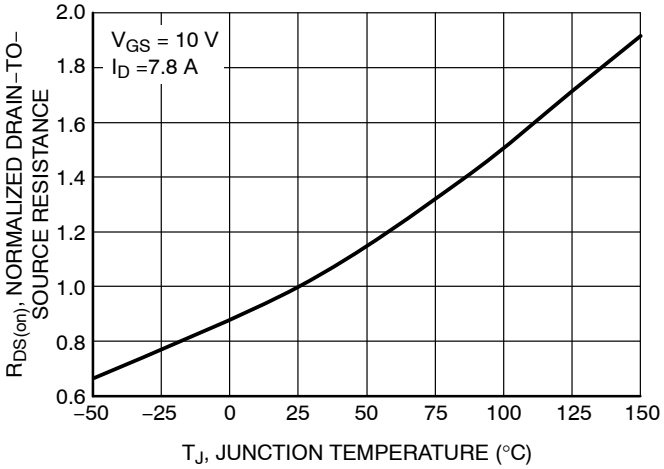



**Figure 5. On−Resistance Variation with Temperature**

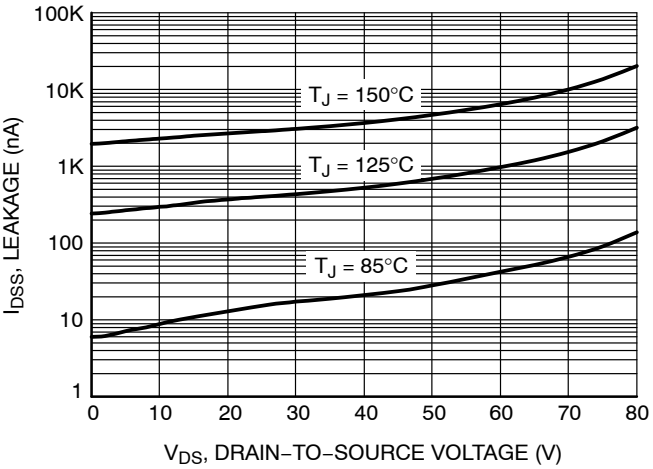



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS

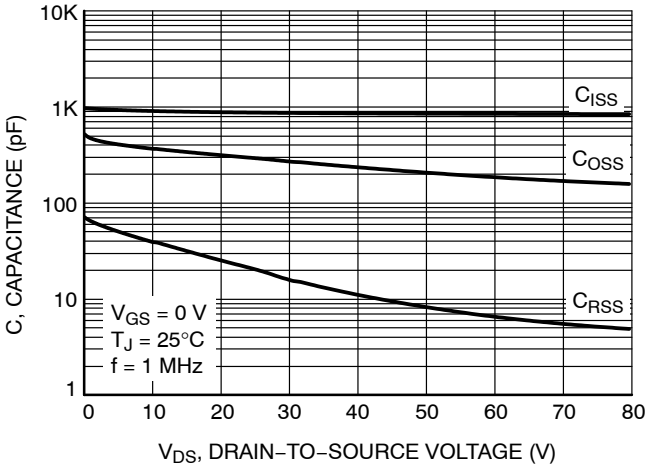



**Figure 7. Capacitance Variation**

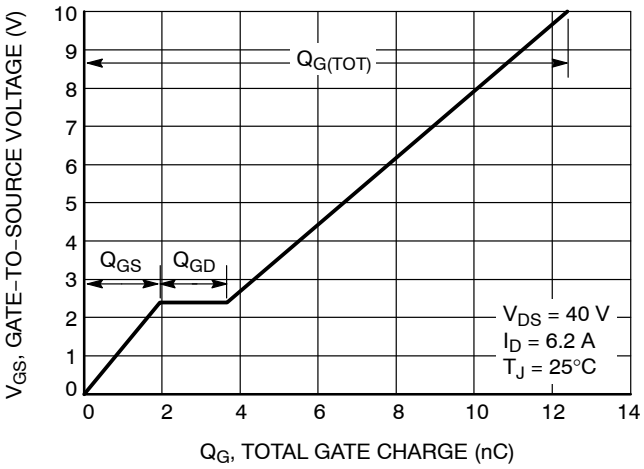



**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

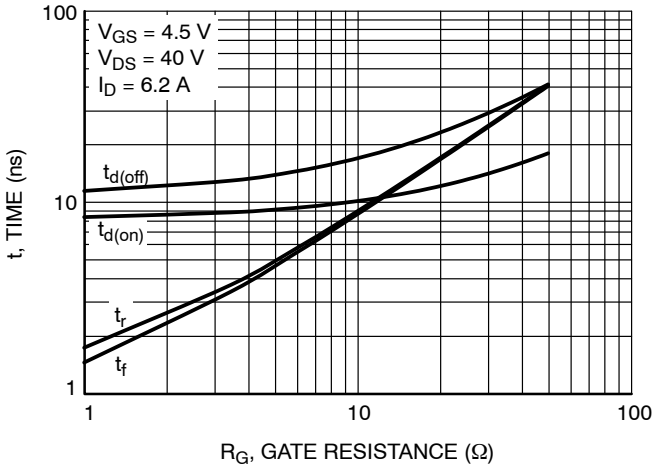



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

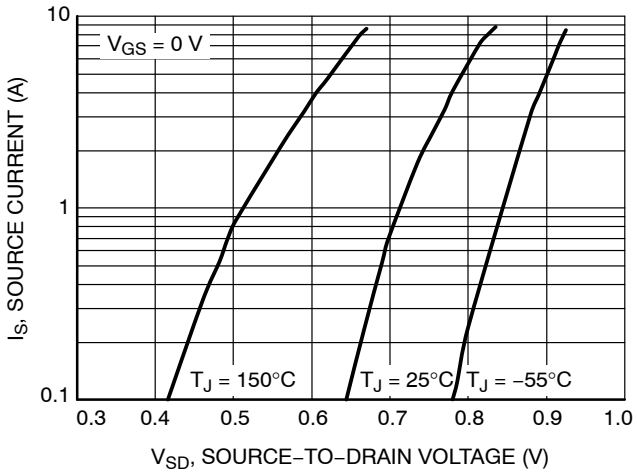



**Figure 10. Diode Forward Voltage vs. Current**

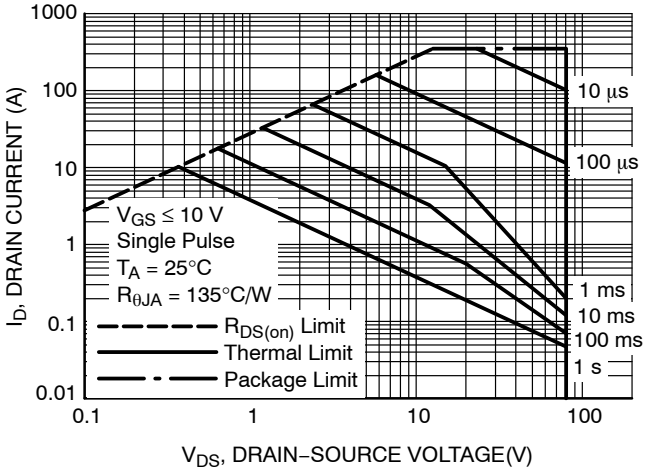



**Figure 11. Safe Operating Area**

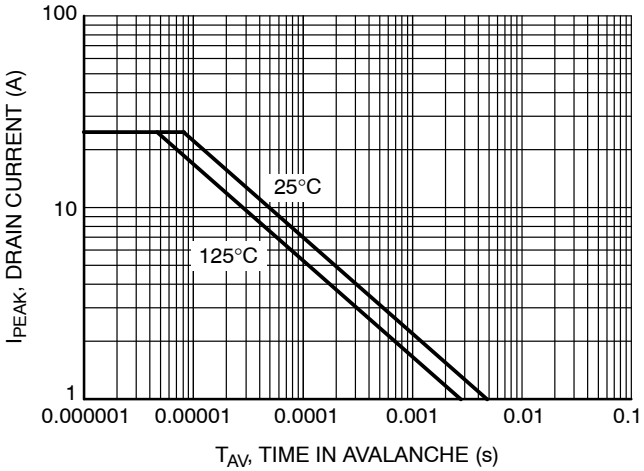



**Figure 12. $I_{PEAK}$ vs. Time in Avalanche**

## TYPICAL CHARACTERISTICS

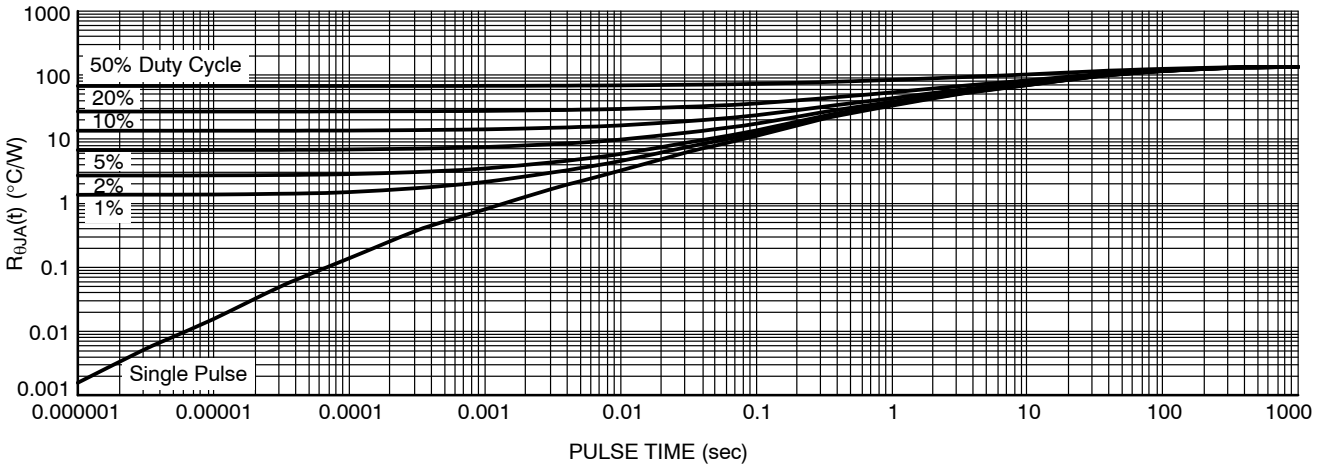



**Figure 13. Thermal Characteristics**

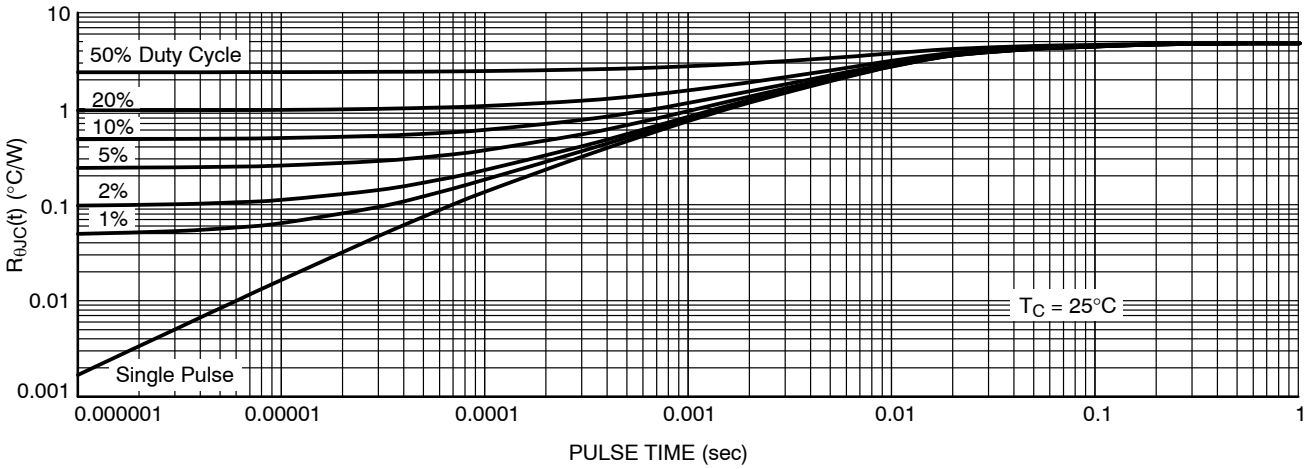
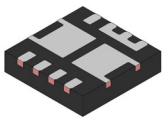


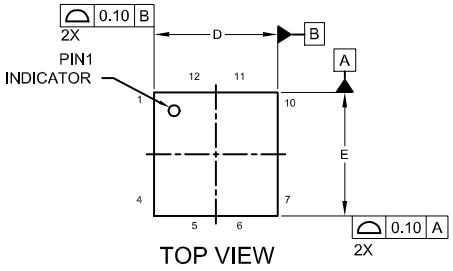

**Figure 14. Thermal Characteristics**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



**WQFN12 3.3X3.3, 0.65P**
CASE 510CJ
ISSUE A

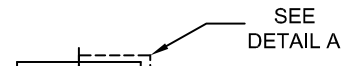
DATE 08 AUG 2022

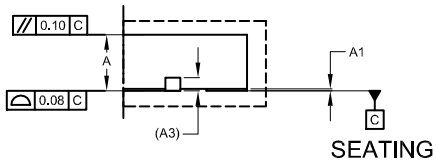



NOTES:

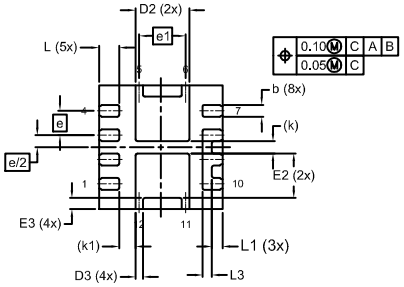
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
5. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

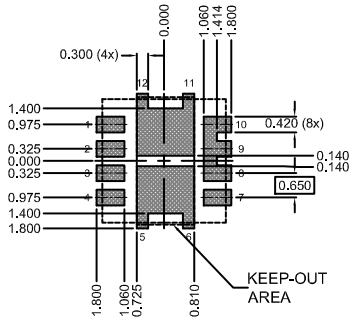
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | -- | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.27 | 0.32 | 0.37 |
| D | 3.20 | 3.30 | 3.40 |
| D2 | 1.34 | 1.44 | 1.54 |
| D3 | 0.10 | 0.20 | 0.30 |
| E | 3.20 | 3.30 | 3.40 |
| E2 | 1.09 | 1.19 | 1.29 |
| E3 | 0.20 | 0.30 | 0.40 |
| e | | 0.65 BSC | |
| e/2 | | 0.325 BSC | |
| e1 | | 1.24 BSC | |
| k | | 0.33 REF | |
| k1 | | 0.43 REF | |
| L | 0.44 | 0.54 | 0.64 |
| L1 | 0.19 | 0.29 | 0.39 |
| L3 | 0.15 | 0.25 | 0.35 |




DETAIL 'A'
SCALE 2:1

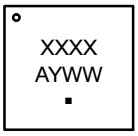



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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|---|---|---|
| DESCRIPTION: | WQFN12 3.3X3.3, 0.65P | PAGE 1 OF 1 |

## ADDITIONAL INFORMATION

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**Technical Library:** www.onsemi.com/design/resources/technical−documentation
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