

MOSFET - Single N-Channel

40 V, 2.1 mΩ, 150 A

NTTFS2D1N04HL

Features

- Max $R_{DS(on)}$ = 2.1 mΩ at $V_{GS} = 10$ V, $I_D = 23$ A
- Max $R_{DS(on)}$ = 3.3 mΩ at $V_{GS} = 4.5$ V, $I_D = 18$ A
- High Performance Technology for Extremely Low $R_{DS(on)}$
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- DC-DC Buck Converters
- Point of Load
- High Efficiency Load Switch and Low Side Switching
- Oring FET

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	40	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	I_D	150	A
Power Dissipation $R_{\theta JC}$ (Note 1)			
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	I_D	24	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			
Pulsed Drain Current	I_{DM}	958	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to $+150$	$^\circ\text{C}$
Source Current (Body Diode)	I_S	69	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{AS} = 29$ A, $L = 0.3$ mH) (Note 3)	E_{AS}	126	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

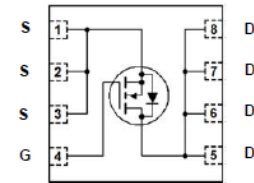
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

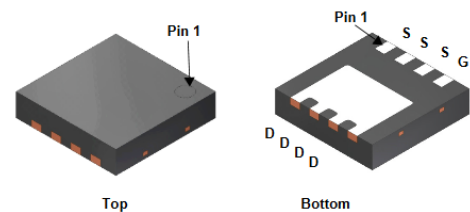
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	1.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	54.8	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using 1 in² pad size, 1 oz. Cu pad.
3. E_{AS} of 126 mJ is based on started $T_J = 25^\circ\text{C}$, $I_{AS} = 29$ A, $V_{DD} = 32$ V, $V_{GS} = 10$ V. 100% test at $I_{AS} = 29$ A.

$V_{(BR)DS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	2.1 mΩ @ 10 V	150 A
	3.3 mΩ @ 4.5 V	

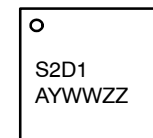


N-CHANNEL MOSFET



WDFN8
3.3X3.3, 0.65P
CASE 483AW

MARKING DIAGRAM



S2D1 = Specific Device Code
A = Assembly Plant Code
Y = Numeric Year Code
WW = Work Week Code
ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS2D1N04HLTWG	PQFN8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTTFS2D1N04HL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		21.80		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, T_J = 25^\circ\text{C}$			10	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, T_J = 125^\circ\text{C}$			100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 120\text{ }\mu\text{A}$	1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 120\text{ }\mu\text{A}$, ref to 25°C		-4.63		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 23\text{ A}$		1.7	2.1	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 18\text{ A}$		2.5	3.3	
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 23\text{ A}$		256		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		1		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$		2745		pF
Output Capacitance	C_{OSS}			645		
Reverse Transfer Capacitance	C_{RSS}			38		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}, I_D = 11.5\text{ A}$		43.6		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 32\text{ V}, I_D = 11.5\text{ A}$		20.7		nC
Gate-to-Source Charge	Q_{GS}			6.1		
Gate-to-Drain Charge	Q_{GD}			6.2		
Plateau Voltage	V_{GP}			2.5		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 32\text{ V}, I_D = 11.5\text{ A}, R_G = 2.5\text{ }\Omega$		17		ns
Rise Time	t_r			12		
Turn-Off Delay Time	$t_{d(OFF)}$			32		
Fall Time	t_f			9		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 23\text{ A}, T_J = 25^\circ\text{C}$		0.79	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 23\text{ A}, T_J = 125^\circ\text{C}$		0.64		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 11.5\text{ A}$		22		ns
Reverse Recovery Charge	Q_{RR}			17		nC
Charge Time	t_a	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 11.5\text{ A}$		22		ns
Discharge Time	t_b			13		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures

5. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

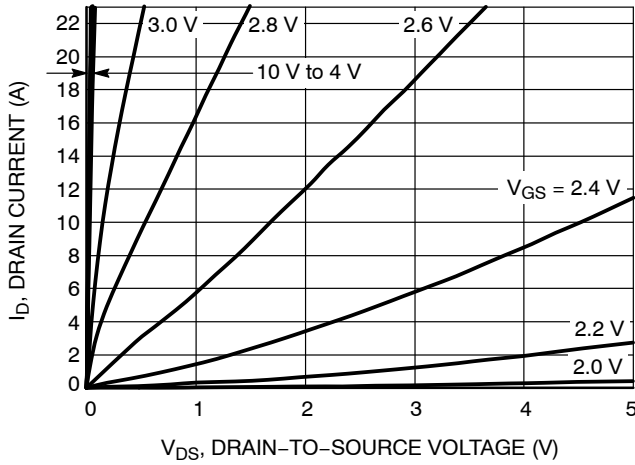


Figure 1. On-Region Characteristics

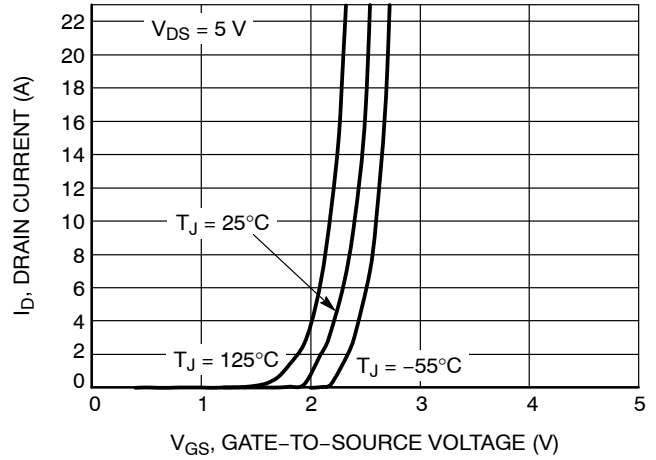


Figure 2. Transfer Characteristics

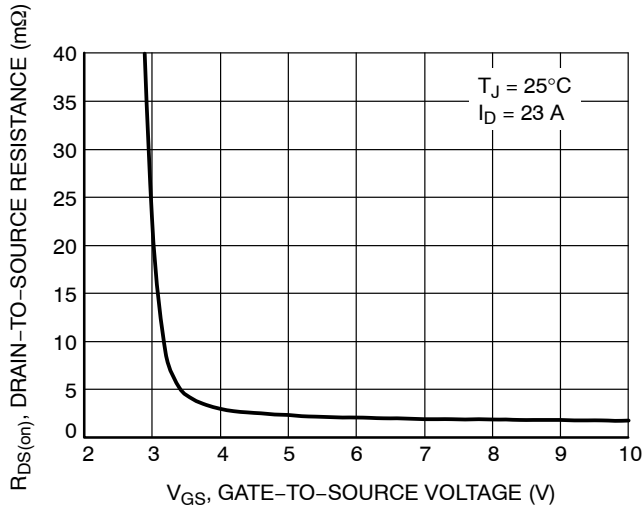


Figure 3. On-Resistance vs. Gate-to-Source Voltage

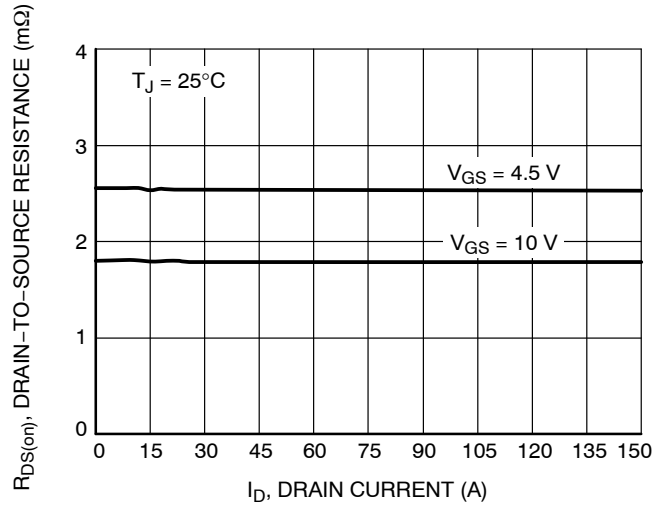


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

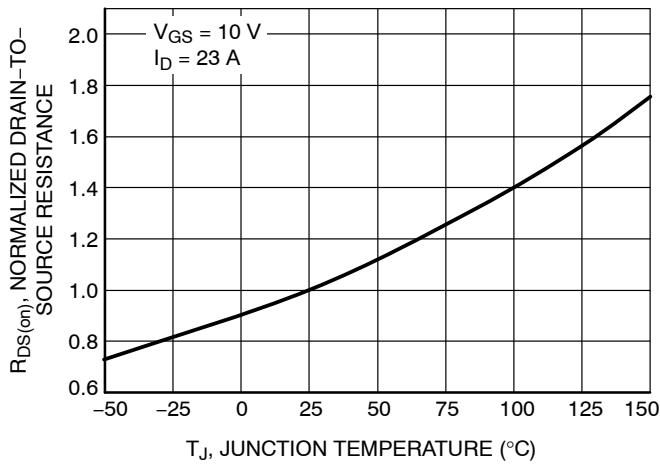


Figure 5. On-Resistance Variation with Temperature

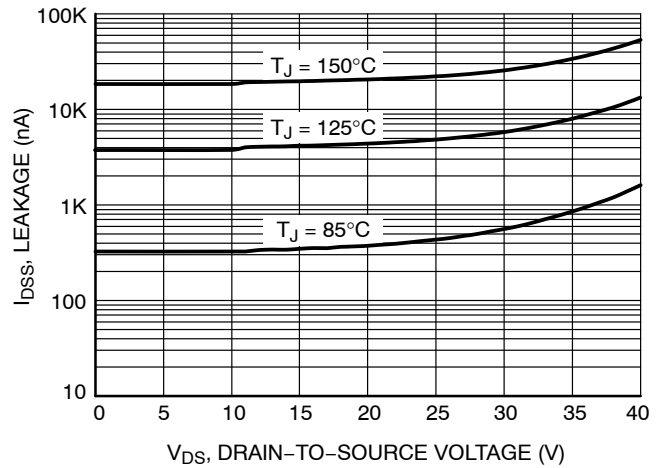


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

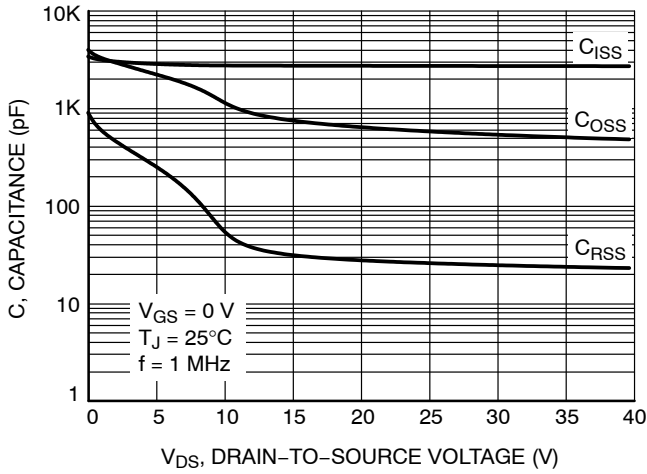


Figure 7. Capacitance Variation

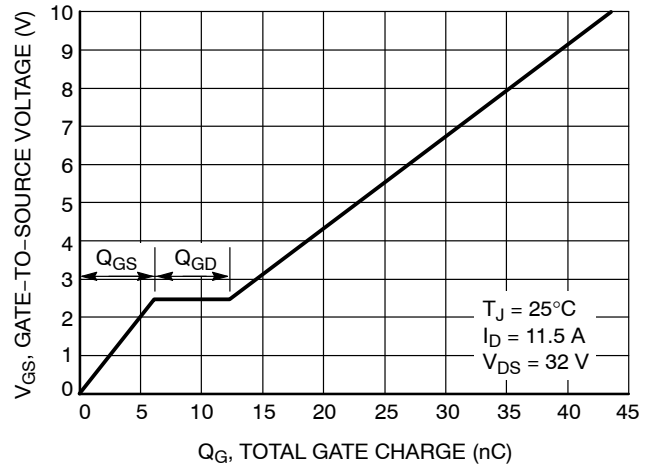


Figure 8. Gate-to-Source Voltage vs. Total Charge

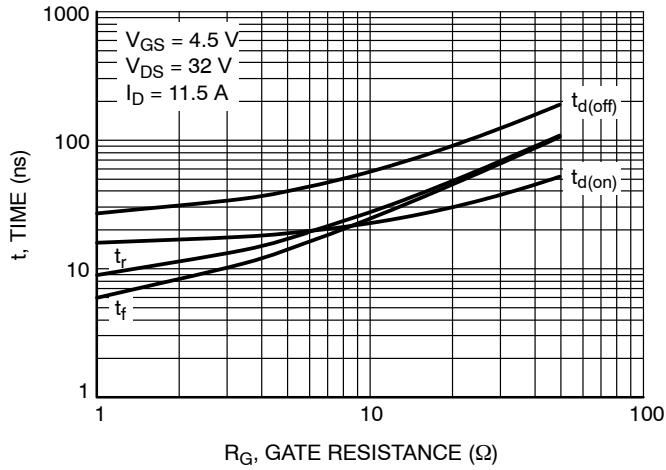


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

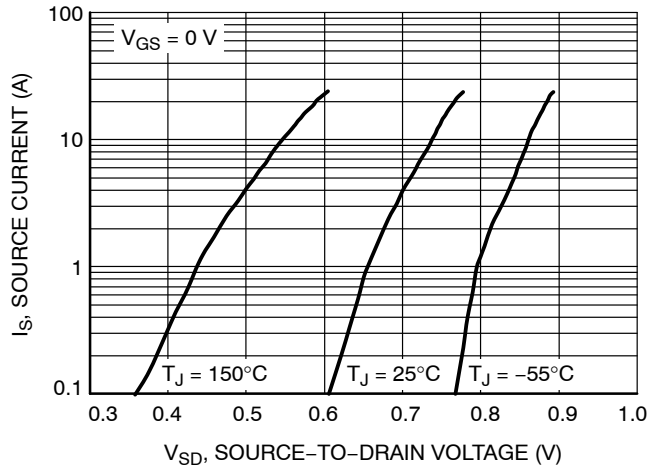


Figure 10. Diode Forward Voltage vs. Current

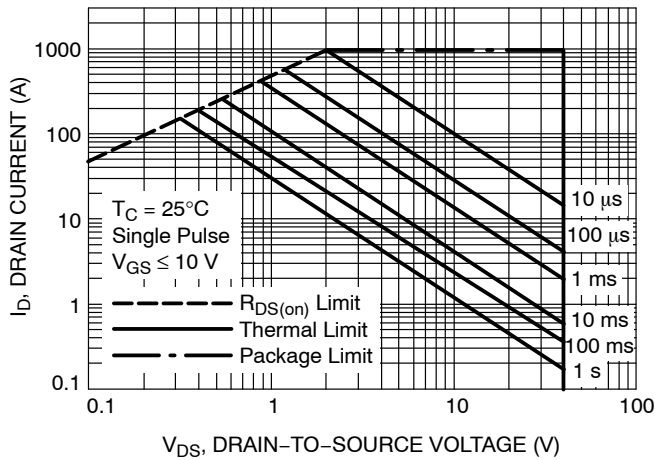


Figure 11. Maximum Rated Forward Biased Safe Operating Area

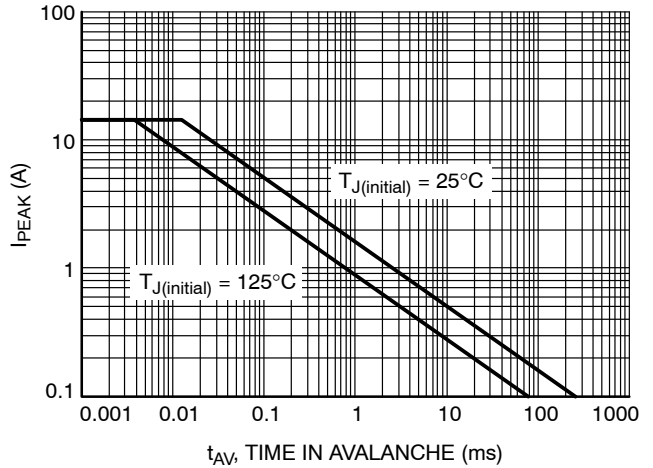


Figure 12. Maximum Drain Current vs. Time in Avalanche

NTTFS2D1N04HL

TYPICAL CHARACTERISTICS

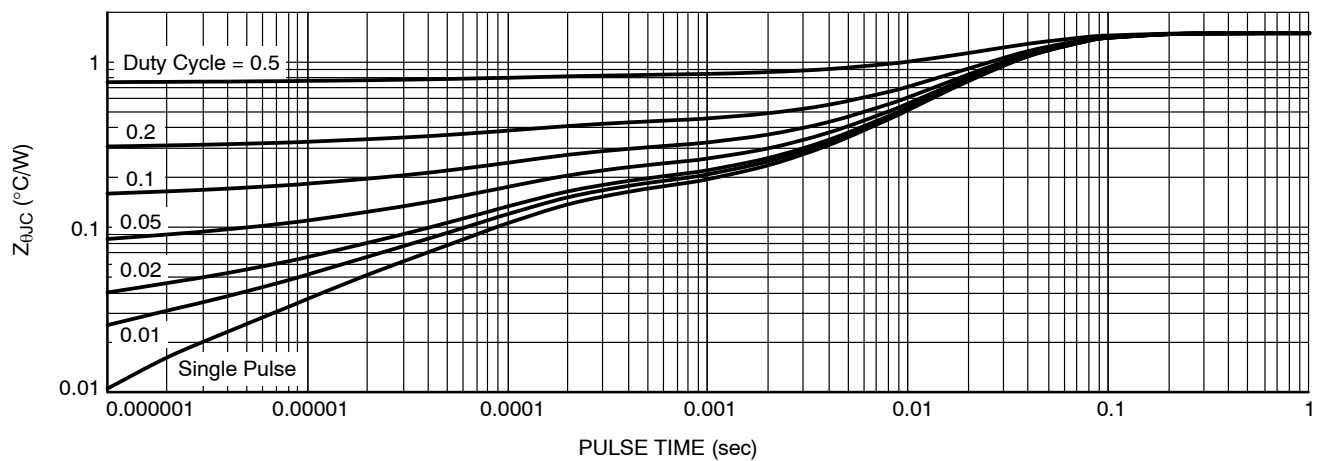
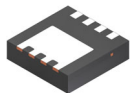


Figure 13. Transient Thermal Impedance

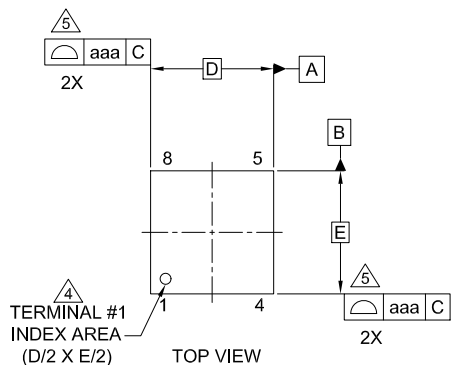


WDFN8 3.30x3.30x0.75, 0.65P

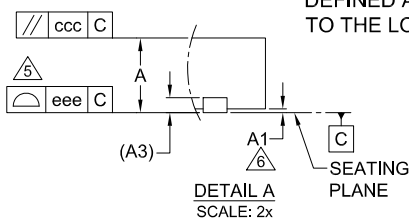
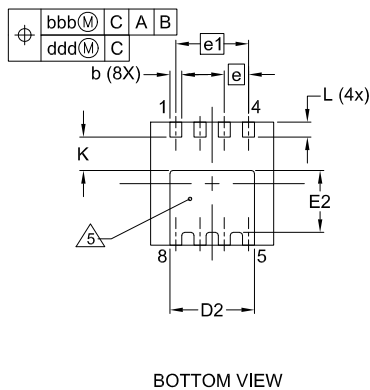
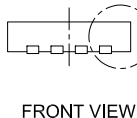
CASE 483AW

ISSUE B

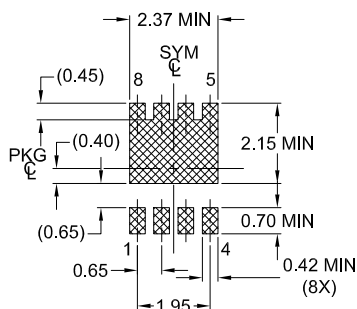
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-SEE DETAIL 'A'



LAND PATTERN RECOMMENDATION



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SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL. SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.30 BSC		
D2	2.17	2.27	2.37
E	3.30 BSC		
E2	1.56	1.66	1.76
e	0.65 BSC		
e1	1.95 BSC		
K	0.90	--	--
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

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