MOSFET - Power, Single N-Channel, Source Down DualCool 33, WDFN9

80 V, 3.6 mΩ, 107 A

NTTFSSCH4D0N08XL

V$_{(BR)DSS}$	R$_{DS(ON)}$ MAX	I$_D$ MAX
80 V	3.6 mΩ @ 10 V	107 A
	5.3 mΩ @ 4.5 V	

Features

- Excellent Thermal Conduction by Advanced Source−Down Center Gate Dual−Cooling Package Technology (3.3x3.3mm)
- Ultra Low R$_{DS(on)}$ to Improve System Efficiency
- Low Q$_G$ and Capacitance to Minimize Driving and Switching Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Switching Frequency DC−DC Conversion
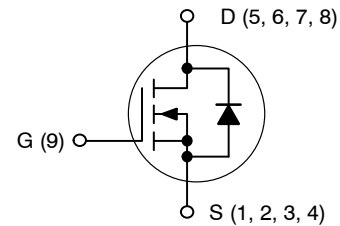- Synchronous Rectifier

N−CHANNEL MOSFET

D (5, 6, 7, 8)
G (9)
S (1, 2, 3, 4)

**WDFN9
CASE 511BX**

MAXIMUM RATINGS (T$_J$ = 25°C unless otherwise noted)

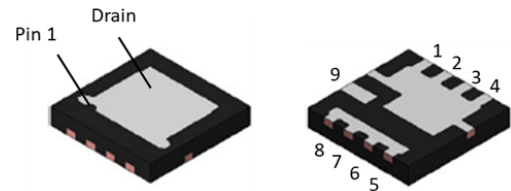| Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V$_{DSS}$	80	V
Gate−to−Source Voltage		V$_{GS}$	±20	V
Continuous Drain Current (Note 1)	T$_C$ = 25°C	I$_D$	107	A
	T$_C$ = 100°C		76	
Power Dissipation (Notes 1, 2)	T$_C$ = 25°C	P$_D$	102	W
Pulsed Drain Current	T$_C$ = 25°C, t$_p$ = 100 μs	I$_{DM}$	419	A
Pulsed Source Current (Body Diode)		I$_{SM}$	419	
Operating Junction and Storage Temperature Range		T$_J$, T$_{stg}$	−55 to +175	°C
Source Current (Body Diode)		I$_S$	155	A
Single Pulse Avalanche Energy (I$_{PK}$ = 40 A)		E$_{AS}$	80	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T$_L$	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 1 in^2 pad size, 1 oz Cu pad.
3. E$_{AS}$ of 80 mJ is based on started T$_J$ = 25°C, I$_{AS}$ = 40 A, V$_{GS}$ = 10 V, 100% avalanche tested.

MARKING DIAGRAM

XXXAYWZZ

PIN 1 INDICATOR

4D0 = Specific Device Code
A = Assembly Location
YW = Assembly Start Week
ZZ = Assembly Lot Number

ORDERING INFORMATION

THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case (Bottom)	$R_{\theta JCB}$	1.5	°C/W
Thermal Resistance, Junction−to−Case (Top)	$R_{\theta JCT}$	1.2	
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	60	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	80			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25°C		32		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25°C			10	μA
		V_{DS} = 80 V, T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 23 A		3.1	3.6	mΩ
		V_{GS} = 4.5 V, I_D = 18 A		3.9	5.3	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 115 μA, T_J = 25°C	1.5		2.1	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 115 μA		−6		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 23 A		156		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}			2520		pF
Output Capacitance	C_{OSS}	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz		630		
Reverse Transfer Capacitance	C_{RSS}			18		
Output Charge	Q_{OSS}			47		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DD} = 40 V; I_D = 23 A		19		
				40		
Threshold Gate Charge	$Q_{G(TH)}$			4.6		
Gate−to−Source Charge	Q_{GS}	V_{GS} = 10 V, V_{DD} = 40 V; I_D = 23 A		8.1		
Gate−to−Drain Charge	Q_{GD}			6.2		
Gate Plateau Voltage	V_{GP}			3.1		V
Gate Resistance	R_G	f = 1 MHz		0.4		Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$			11		ns
Rise Time	t_r	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 40 V, I_D = 23 A, R_G = 2.5 Ω		5		
Turn−Off Delay Time	$t_{d(OFF)}$			28		
Fall Time	t_f			4		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 23 A, T_J = 25°C		0.8		V
		V_{GS} = 0 V, I_S = 23 A, T_J = 125°C		0.7		

NTTFSSCH4D0N08XL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 23 A, dI/dt = 1000 A/μs, V_{DD} = 40 V		19		ns
Charge Time	t_a			11		
Discharge Time	t_b			8		
Reverse Recovery Charge	Q_{RR}			109		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS
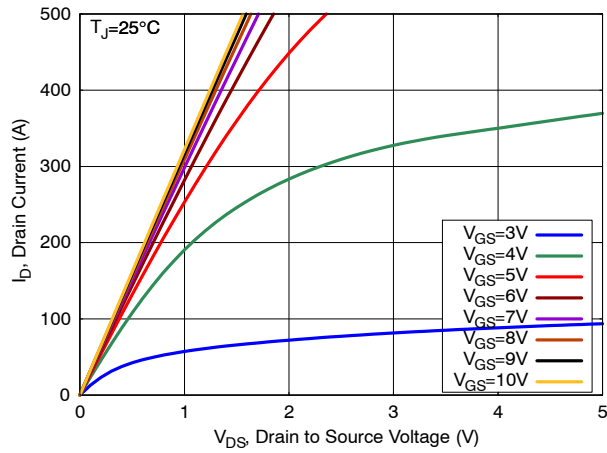
Figure 1. On−Region Characteristics
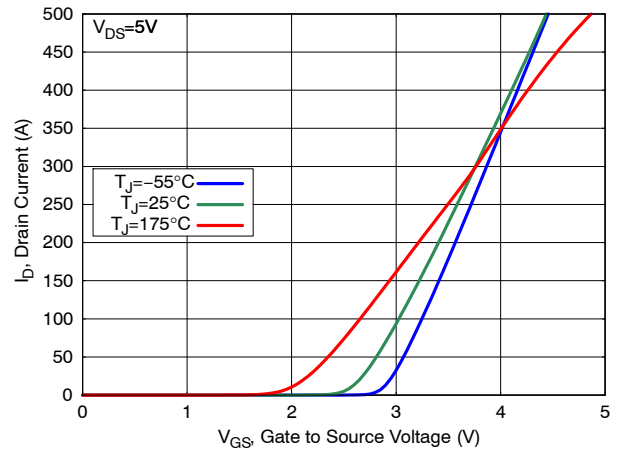
Figure 2. Transfer Characteristics
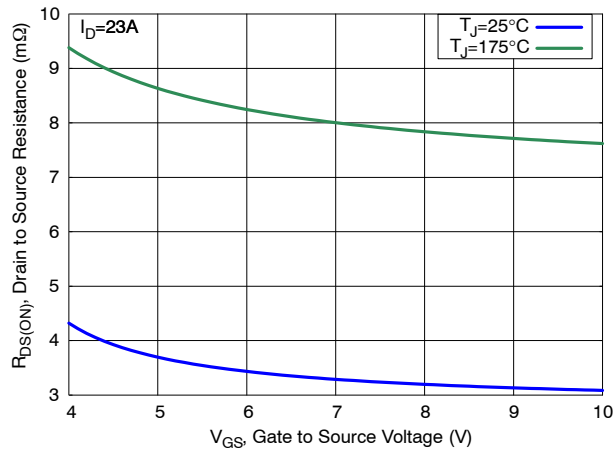
Figure 3. On−Resistance vs. Gate Voltage
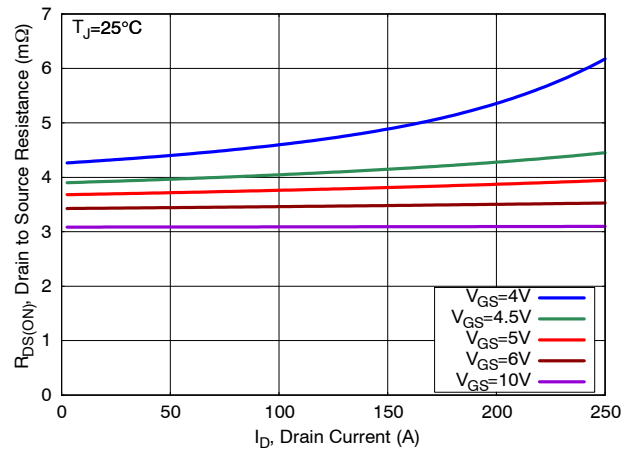
Figure 4. On−Resistance vs. Drain Current
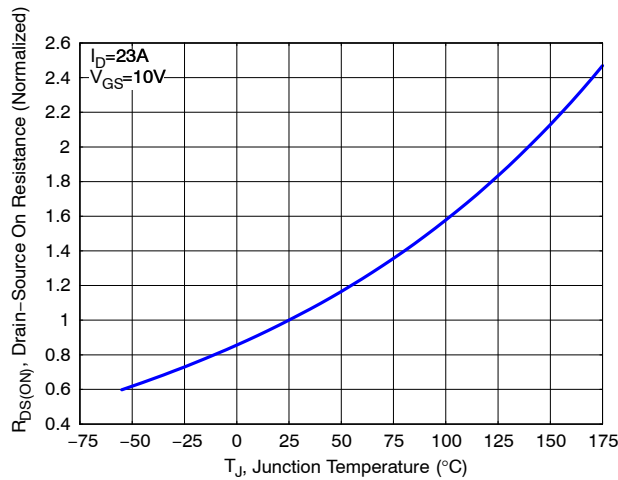
Figure 5. Normalized On−Resistance vs. Junction Temperature
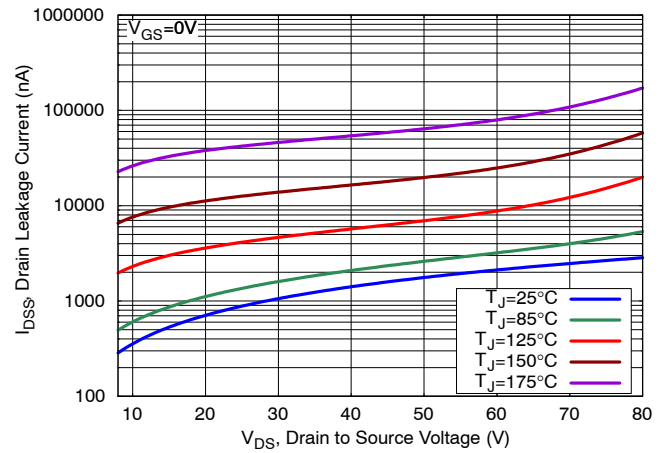
Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS
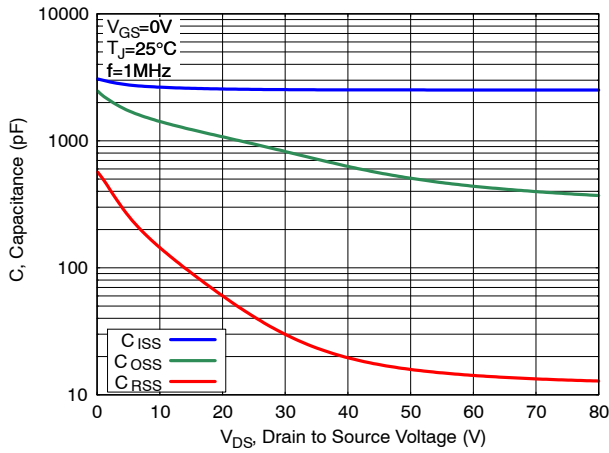
Figure 7. Capacitance Characteristics
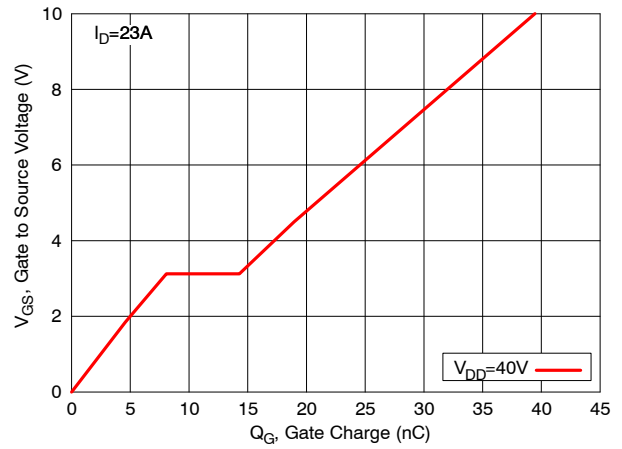
Figure 8. Gate Charge Characteristics
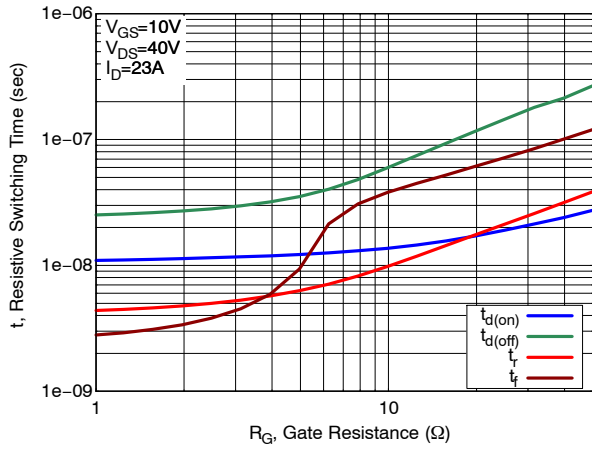
Figure 9. Resistive Switching Time Variation vs. Gate Resistance
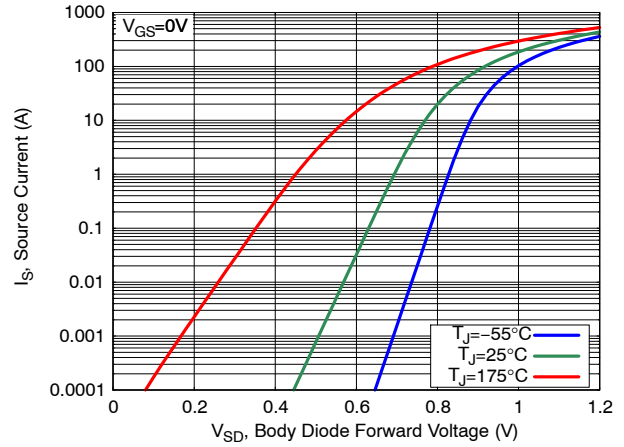
Figure 10. Diode Forward Characteristics
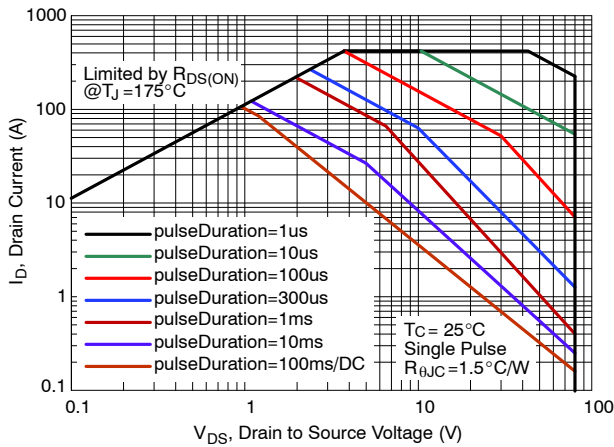
Figure 11. Safe Operating Area (SOA)
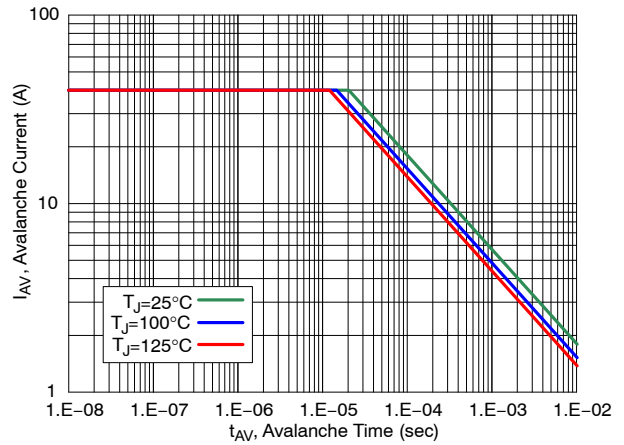
Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS
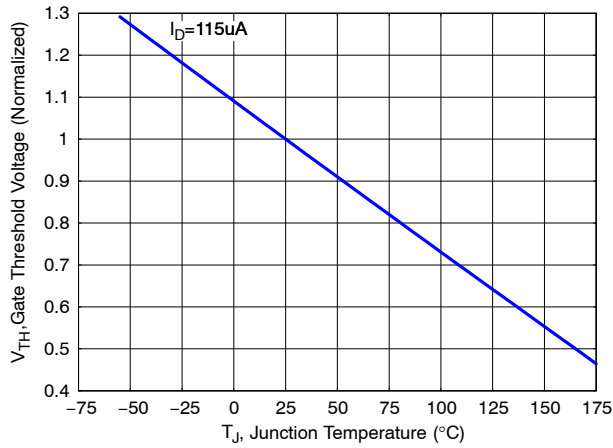
Figure 13. Gate Threshold Voltage vs. Junction Temperature
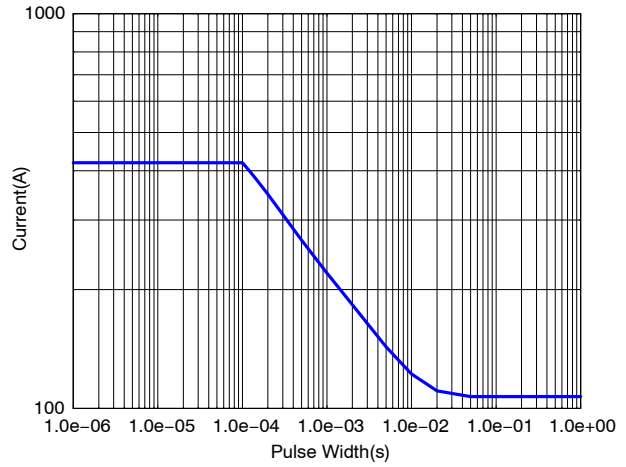
Figure 14. IDM vs. Pulse Width
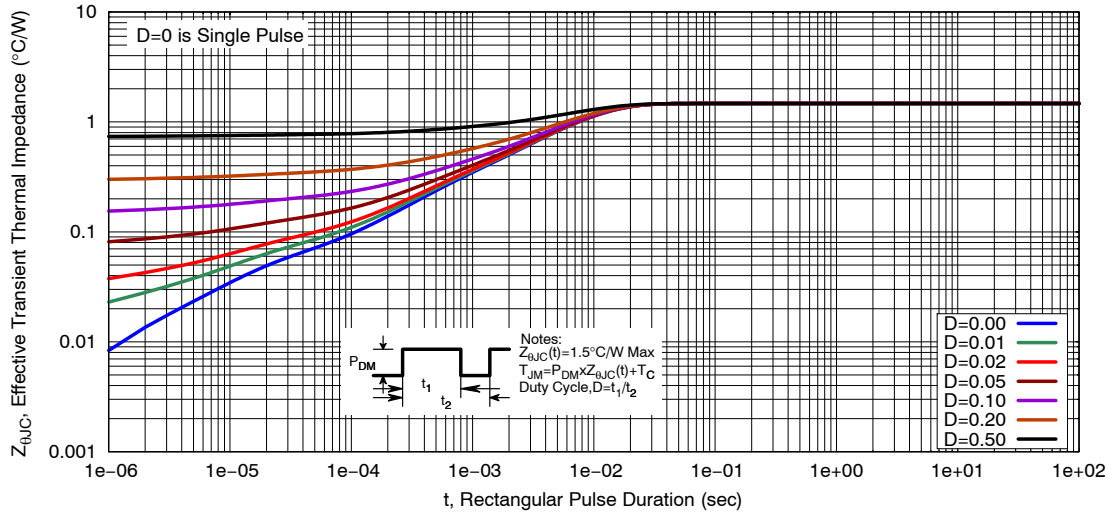
Figure 15. Transient Thermal Response

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTTFSSCH4D0N08XLTWG	4D0	WDFN9 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
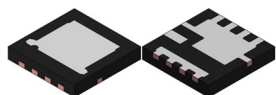
WDFN9 3.30x3.30x0.58, 0.65P
CASE 511BX
ISSUE B

DATE 13 AUG 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1, D2, E1 AND E2 DO NOT INCLUDE MOLD FLASH.
5. SEATING PLANE IS DEFINED BY THE TERMINALS.
   "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

TOP VIEW

FRONT VIEW

SEE DETAIL A

DETAIL A
SCALE: 3:1

SEATING PLANE

BOTTOM VIEW
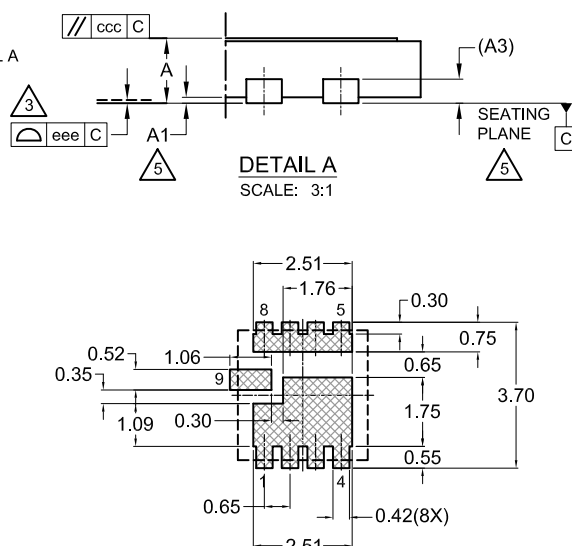
LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

UNIT IN MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.53	0.58	0.63
A1	0.00	-	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
b1	0.37	0.42	0.47
D	3.30 BSC		
D2	2.31	2.41	2.51
D3	1.58	1.68	1.78
D4	0.35	0.45	0.55
D5	0.25	0.35	0.45
D6	2.10	2.20	2.30
D7	2.31	2.41	2.51
D8	0.55 REF		
e	0.65 BSC		
E	3.30 BSC		
E2	0.84	0.94	1.04
E3	0.20	0.25	0.30
E4	1.50	1.60	1.70
E5	0.25	0.35	0.40
E6	0.60 REF		
E7	2.10	2.20	2.30
k	0.75 REF		
k1	0.45 REF		
L	0.73	0.83	0.93
L1	0.10	0.20	0.30
L2	0.35	0.45	0.55
L4	0.40	0.50	0.60
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

GENERIC
MARKING DIAGRAM*

XXXAYWZZ

PIN 1
INDICATOR
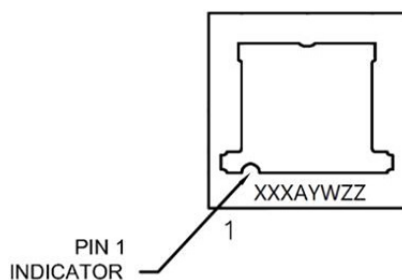
XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFN9 3.30x3.30x0.58, 0.65P		PAGE 1 OF 1

ADDITIONAL INFORMATION

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