

MOSFET - Power, Single N-Channel, Source Down 33, WDFN9 25 V, 0.58 mΩ, 310 A

NTTFSSH0D7N02X

Features

- Advanced Source-Down Package Technology (3.3 x 3.3 mm) with Excellent Thermal Conduction
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- Low Q_G and Capacitance to Minimize Driving and Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Switching Frequency DC-DC Conversion
- Synchronous Rectifier

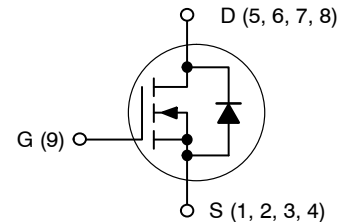
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	25	V
Gate-to-Source Voltage	V_{GS}	-12/+16	V
Continuous Drain Current (Notes 1, 2)	$T_C = 25^\circ\text{C}$	I_D 310	A
	$T_C = 100^\circ\text{C}$	196	
Power Dissipation (Note 1)	$T_C = 25^\circ\text{C}$	P_D 87	W
Pulsed Drain Current	$T_C = 25^\circ\text{C}$, $t_p = 100 \mu\text{s}$	I_{DM} 1342	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	146	A
Single Pulse Avalanche Energy (Note 3) ($I_{PK} = 62 \text{ A}$)	E_{AS}	192	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

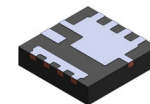
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The entire application environment impacts the thermal resistance values shown, they are not constants and are valid for the particular conditions noted.
- Surface-mounted on FR4 board using a 1 in² pad size, 1 oz Cu pad.
- E_{AS} of 192 mJ is based on started $T_J = 25^\circ\text{C}$, $I_{AS} = 62 \text{ A}$, $V_{GS} = 10 \text{ V}$, 100% avalanche tested.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
25 V	0.58 mΩ @ $V_{GS} = 10 \text{ V}$	310 A
	0.80 mΩ @ $V_{GS} = 4.5 \text{ V}$	



N-CHANNEL MOSFET



WDFN9
CASE 511EB

MARKING DIAGRAM

XXXXXX	0D7N02 = Specific Device Code
XXXXXX	A = Assembly Location
AWLYWW	WL = Wafer Lot
	Y = Year
	WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.4	°C/W
Thermal Resistance, Junction-to-Ambient (Note 4)	$R_{\theta JA}$	60	

4. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz Cu pad.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25°C		21		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}$			10	μA
		$V_{DS} = 20\text{ V}, T_J = 125^\circ\text{C}$			100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 24\text{ A}$		0.51	0.58	m Ω
		$V_{GS} = 6\text{ V}, I_D = 19\text{ A}$		0.56	0.65	
		$V_{GS} = 4.5\text{ V}, I_D = 19\text{ A}$		0.66	0.80	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 484\text{ }\mu\text{A}$	1.1		2.0	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 484\text{ }\mu\text{A}$		-3		mV/°C
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 24\text{ A}$		190		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, V _{DS} = 12 V, f = 1 MHz		3980		pF
Output Capacitance	C _{OSS}			1160		
Reverse Transfer Capacitance	C _{RSS}			124		
Output Charge	Q _{OSS}			22		nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DD} = 12 V; I _D = 24 A		25		
		V _{GS} = 6 V, V _{DD} = 12 V; I _D = 24 A		33		
		V _{GS} = 10 V, V _{DD} = 12 V; I _D = 24 A		55		
Threshold Gate Charge	Q _{G(TH)}			5.7		
Gate-to-Source Charge	Q _{GS}			9.7		
Gate-to-Drain Charge	Q _{GD}			4.1		
Gate Plateau Voltage	V _{GP}			2.5		V
Gate Resistance	R _G	f = 1 MHz		0.4		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 12\text{ V},$ $I_D = 24\text{ A}, R_G = 2.5\text{ }\Omega$		4		ns
Rise Time	t_r			6		
Turn-Off Delay Time	$t_{d(OFF)}$			26		
Fall Time	t_f			57		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 24\text{ A}, T_J = 25^\circ\text{C}$		0.76	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 24\text{ A}, T_J = 125^\circ\text{C}$		0.63		

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ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = 24\text{ A},$ $di/dt = 700\text{ A}/\mu\text{s}, V_{DD} = 12\text{ V}$		17		ns
Charge Time	t_a			10		
Discharge Time	t_b			7		
Reverse Recovery Charge	Q_{RR}			58		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

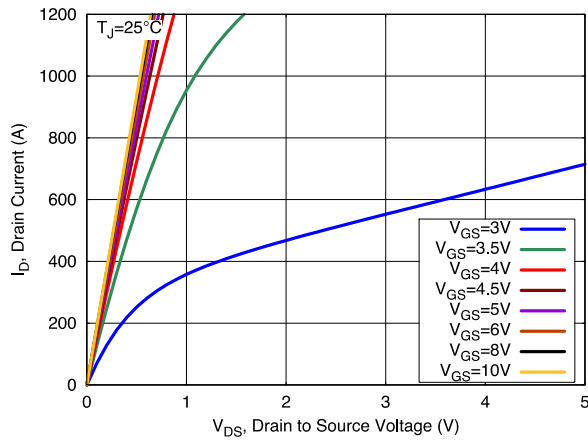


Figure 1. On-Region Characteristics

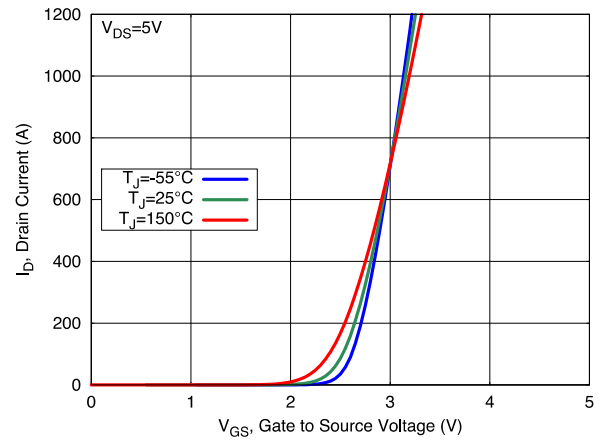


Figure 2. Transfer Characteristics

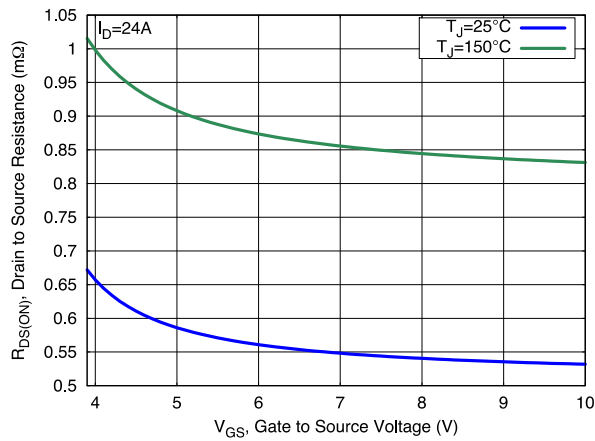


Figure 3. On-Resistance vs. Gate Voltage

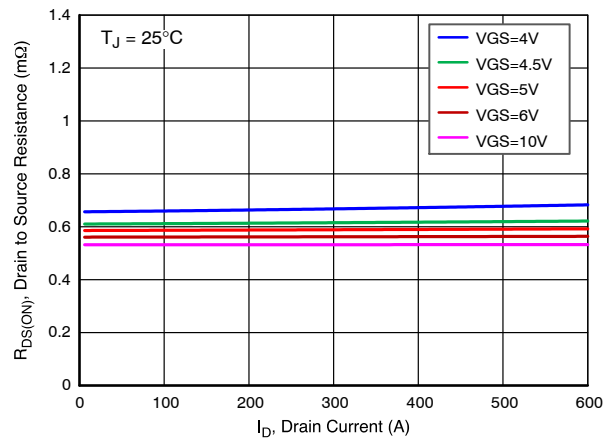


Figure 4. On-Resistance vs. Drain Current

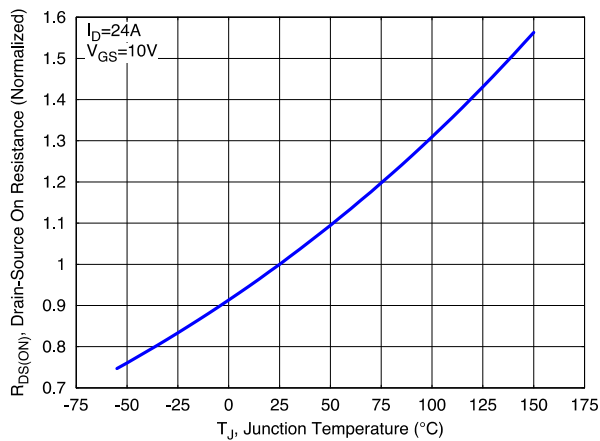


Figure 5. Normalized ON Resistance vs. Junction Temperature

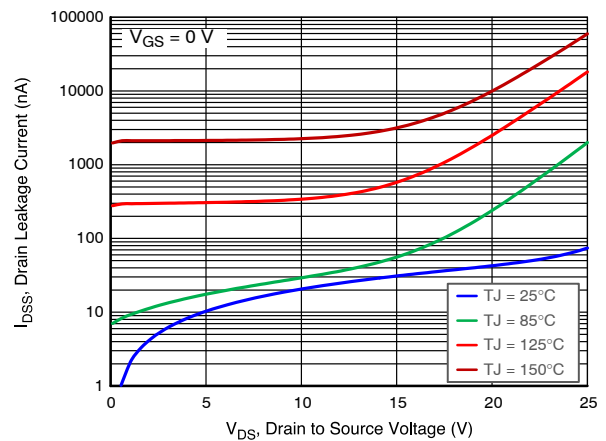


Figure 6. Drain Leakage Current vs Drain Voltage

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TYPICAL CHARACTERISTICS

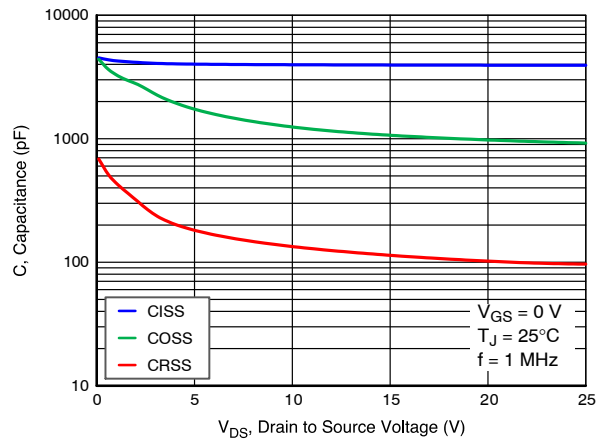


Figure 7. Capacitance Characteristics

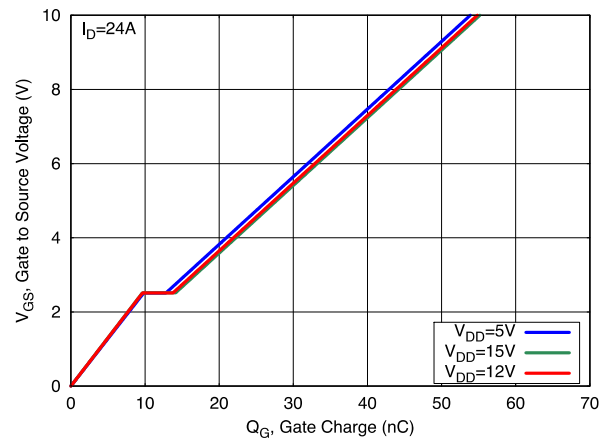


Figure 8. Gate Charge Characteristics

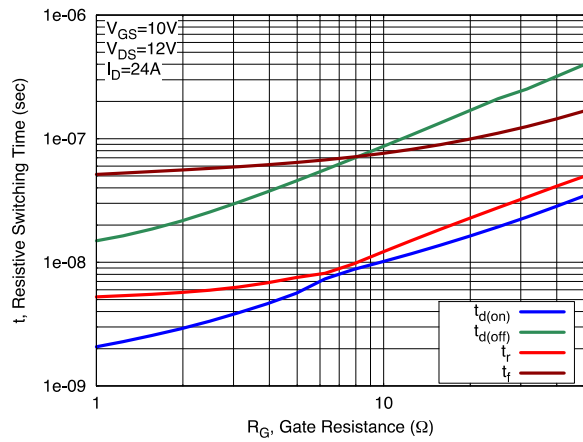


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

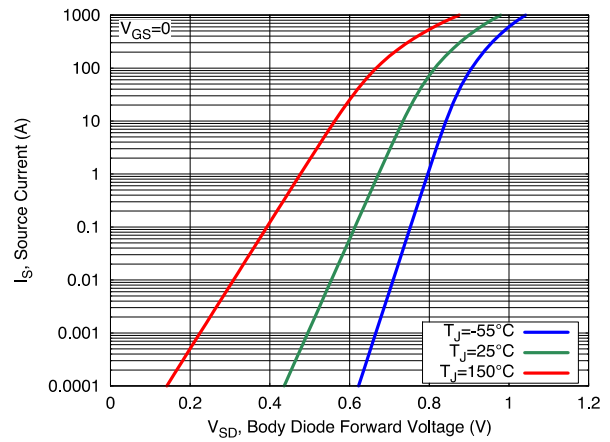


Figure 10. Diode Forward Characteristics

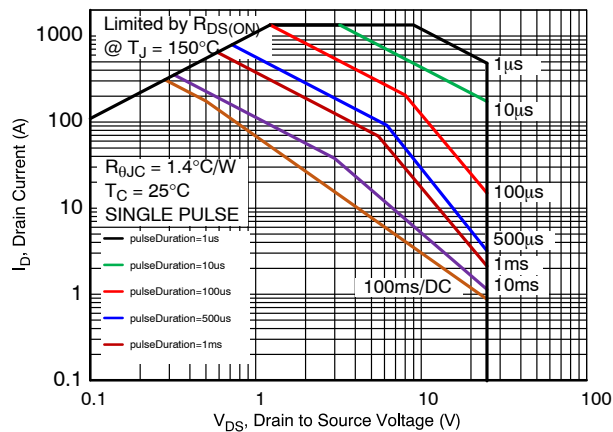


Figure 11. Safe Operating Area (SOA)

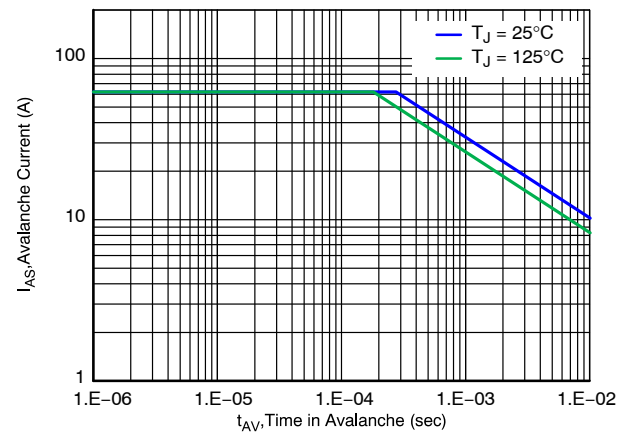


Figure 12. Avalanche Current vs Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

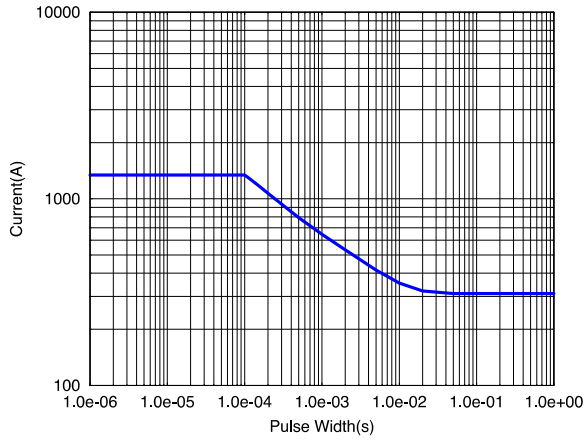


Figure 13. IDM vs Pulse Width

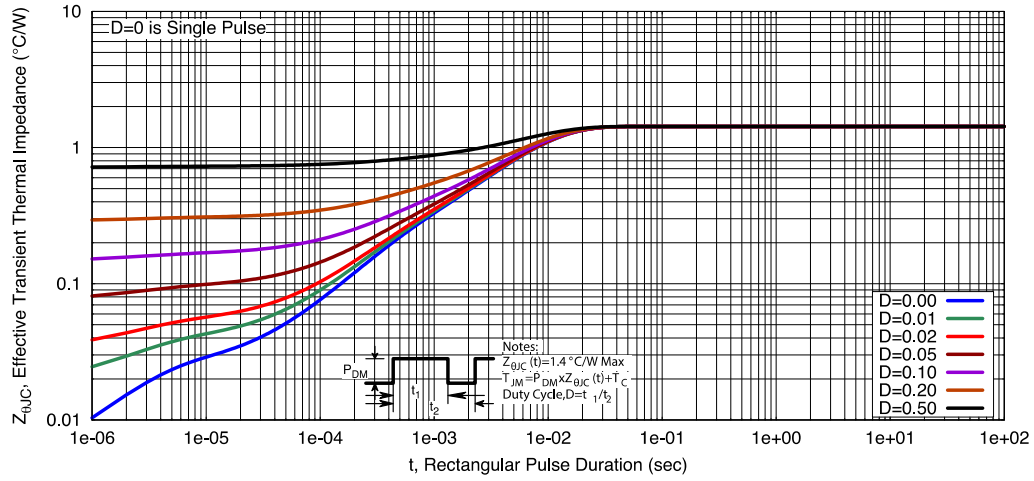
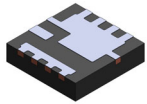


Figure 14. Transient Thermal Response

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTTFSSH0D7N02X	0D7N02	WDFN9 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

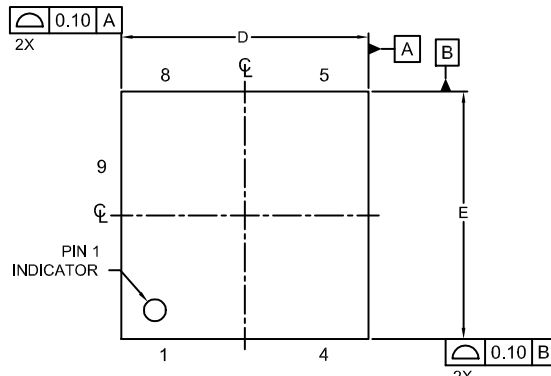


WDFN9 3.3x3.3, 0.65P

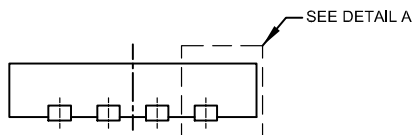
CASE 511EB

ISSUE B

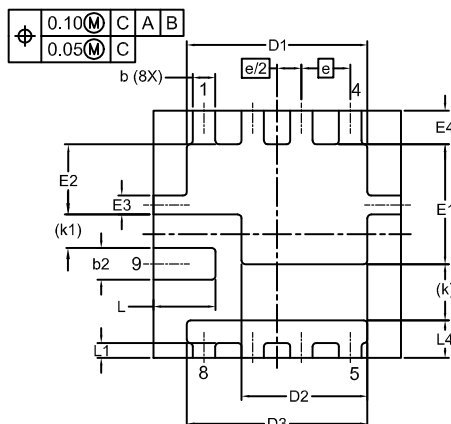
DATE 21 JUL 2021



TOP VIEW



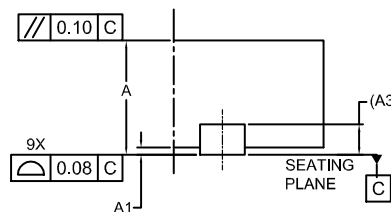
FRONT VIEW



BOTTOM VIEW

NOTES:

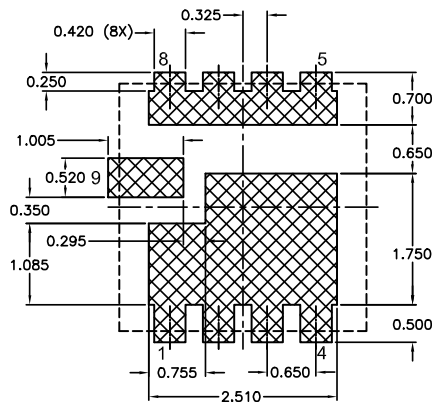
1. CONTROLLING DIMENSION: MILLIMETERS
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D1, D2, E1 AND E2 DO NOT INCLUDE MOLD FLASH.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.



DETAIL A

SCALE: 2:1

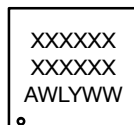
UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
b2	0.37	0.42	0.47
D	3.20	3.30	3.40
D1	2.31	2.41	2.51
D2	1.58	1.68	1.78
D3	2.31	2.41	2.51
E	3.20	3.30	3.40
E1	1.50	1.60	1.70
E2	0.84	0.94	1.04
E3	0.20	0.25	0.30
E4	0.35	0.45	0.55
e	0.650 BSC		
e/2	0.325 BSC		
k	0.75 REF		
k1	0.45 REF		
L	0.73	0.83	0.93
L1	0.10	0.20	0.30
L4	0.40	0.50	0.60



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFN9 3.3x3.3, 0.65P	PAGE 1 OF 1

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