IVN Bus Protector, Single Line LIN & Dual Line CAN

NUP1128, NUP2128

The NUP1128/NUP2128 are designed to protect both CAN and LIN transceivers from ESD and other harmful transient voltage events. These devices provide bidirectional protection for each data line with a single compact SC-70 (SOT-323) or SOD-323 package, giving the system designer a low cost option for improving system reliability and meeting stringent EMI requirements.

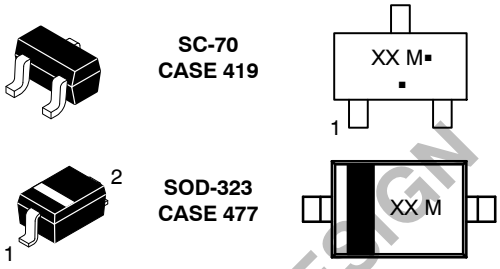
Features

- Low Reverse Leakage Current (< 100 nA)
- SZNUPH1128, SZNUP2128 175 °C $T_{J(max)}$ Devices
  - Rated for High Temperature, Mission Critical and Grade 0 Applications
- IEC Compatibility:
  - IEC 61000-4-2 (ESD): Level 4
  - IEC 61000-4-4 (EFT): 50 A (5/50 ns)
  - IEC 61000-4-5 (Lighting) 3.0 A (8/20 μs)
- ISO 7637-1, Nonrepetitive EMI Surge Pulse 2, 8.0 A (1/50 μs)
- ISO 7637-3, Repetitive Electrical Fast Transient (EFT) EMI Surge Pulses, 50 A (5/50 ns)
- Flammability Rating UL 94 V-0
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

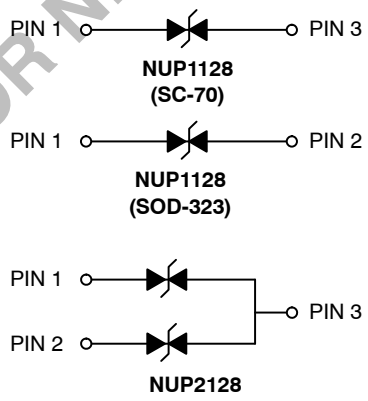
- Automotive Networks
  - CAN / CAN-FD
  - Low and High-Speed CAN
  - Fault Tolerant CAN
  - LIN

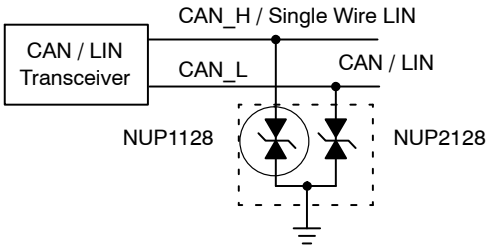
MARKING DIAGRAMS



XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)





ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 7.

MAXIMUM RATINGS (T_J = 25 °C, unless otherwise specified)

Symbol	Rating	Value	Unit
PPK	Peak Power Dissipation, 8/20 μs Double Exponential Waveform (Note 1)	165	W
T_J	Operating Junction Temperature Range NUP1128HT1G, SZNUP1128HT1G All other devices	 −55 to 150 −55 to 175	°C
T_J	Storage Temperature Range NUP1128HT1G, SZNUP1128HT1G All other devices	 −55 to 150 −55 to 175	°C
T_L	Lead Solder Temperature (10 s)	260	°C
ESD	Human Body Model (HBM) IEC 61000-4-2 Contact IEC 61000-4-2 Air ISO 10605 Contact (330 pF / 330 Ω) ISO 10605 Contact (330 pF / 2 kΩ) ISO 10605 Contact (150 pF / 2 kΩ)	8.0 ±30 ±30 ±30 ±30 ±30	kV kV kV kV kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Non-repetitive current pulse per Figure 1.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{RWM}	Reverse Working Voltage	(Note 2)			26.5	V
V_{BR}	Breakdown Voltage	I_T = 1 mA (Note 3)	27.5	31	35.5	V
I_R	Reverse Leakage Current	V_{RWM} = 26.5 V T_A = 150 °C		1 150	100 750	nA
V_C	Clamping Voltage	I_{PP} = 1 A (8/20 μs Waveform) (Note 4) I_{PP} = 3 A		39 46	47 55	V
I_{PP}	Maximum Peak Pulse Current	8/20 μs Waveform (Note 4)	3.0			A
C_J	Capacitance	V_R = 0 V, f = 1 MHz (Line to GND)		11	13	pF
ΔC	Diode Capacitance Matching	V_R = 0 V, f = 1 MHz (Note 5)			2	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
3. V_{BR} is measured at pulse test current I_T.
4. Pulse waveform per Figure 1.
5. ΔC is the percentage difference between C_J of lines 1 and 2 measured according to the test conditions given in the electrical characteristics table.

TYPICAL PERFORMANCE CURVES

(T_J = 25 °C unless otherwise noted)

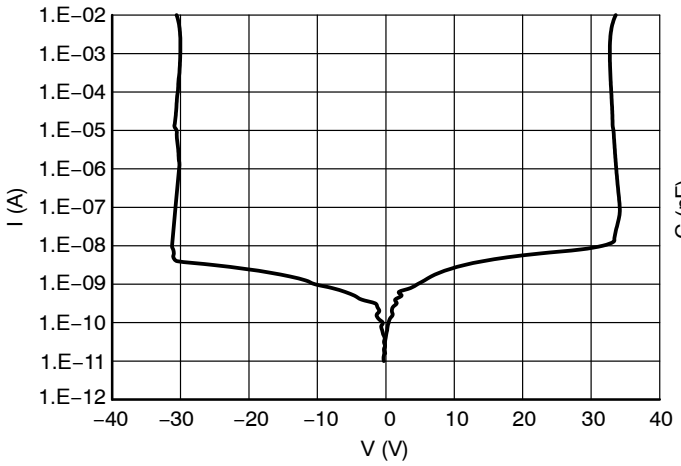


Figure 1. IV Characteristics

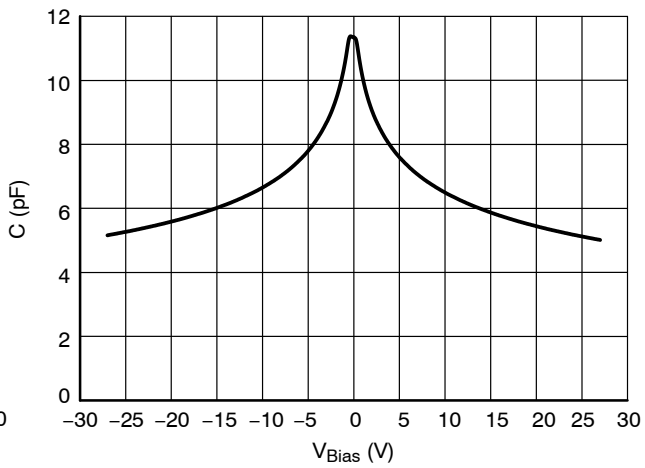


Figure 2. CV Characteristics

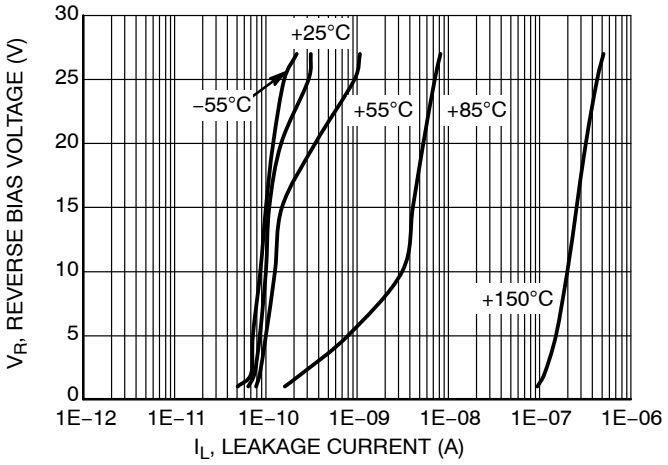


Figure 3. I_R vs Temperature Characteristics

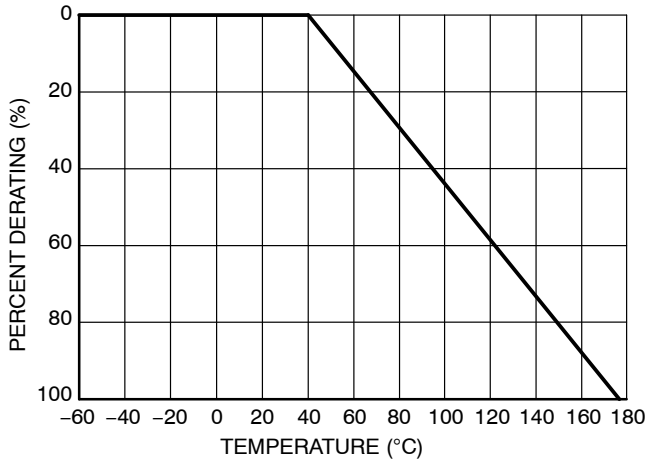


Figure 4. Temperature Power Dissipation Derating

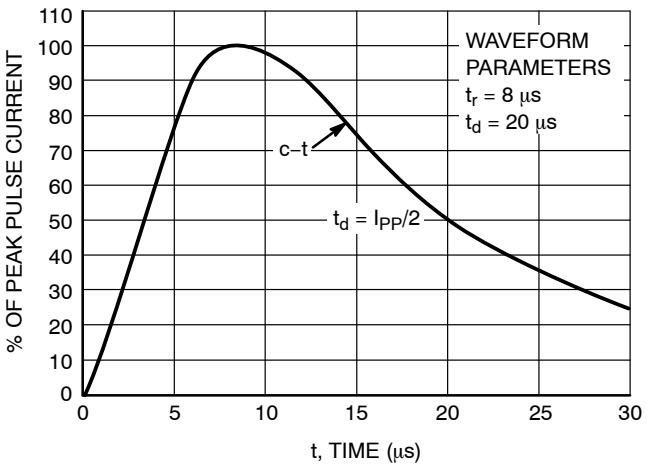


Figure 5. Pulse Waveform (8/20 μs)

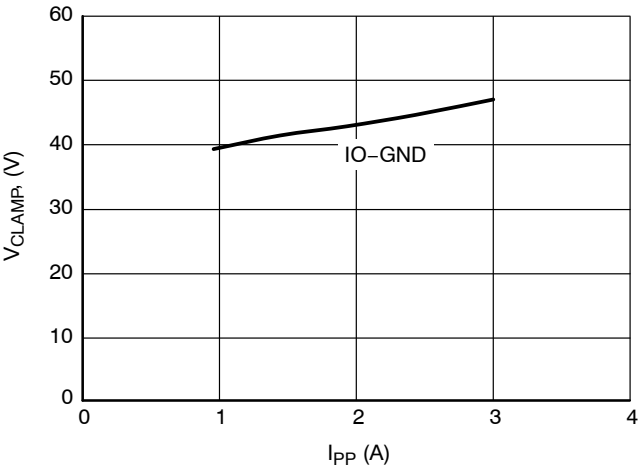


Figure 6. Clamping Voltage vs Peak Pulse Current (8/20 μs)

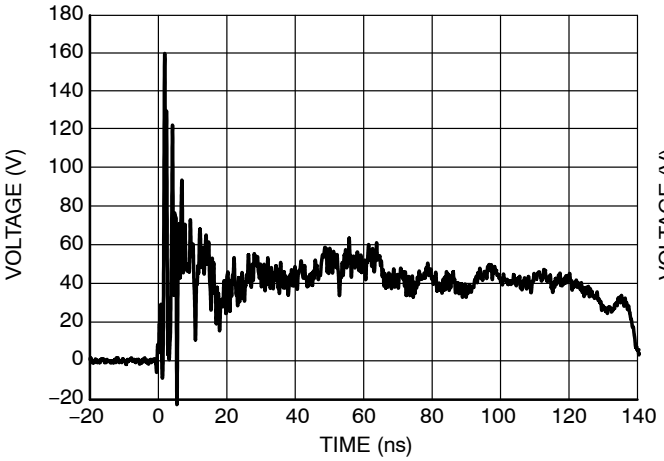


Figure 7. IEC61000-4-2 +8 kV Contact ESD Clamping Voltage

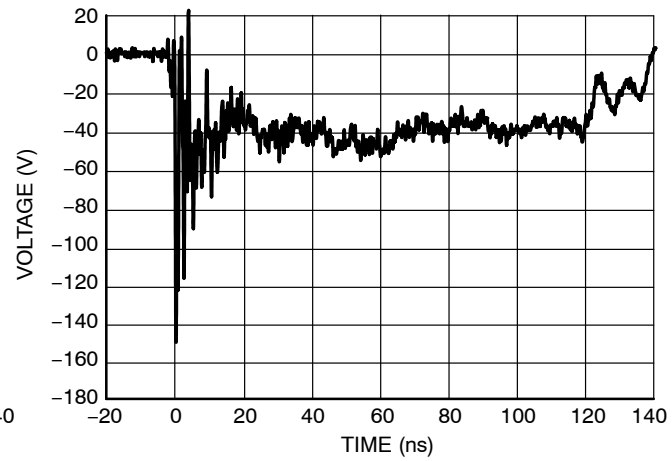


Figure 8. IEC61000-4-2 −8 kV Contact ESD Clamping Voltage

IEC 61000-4-2 Specs

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

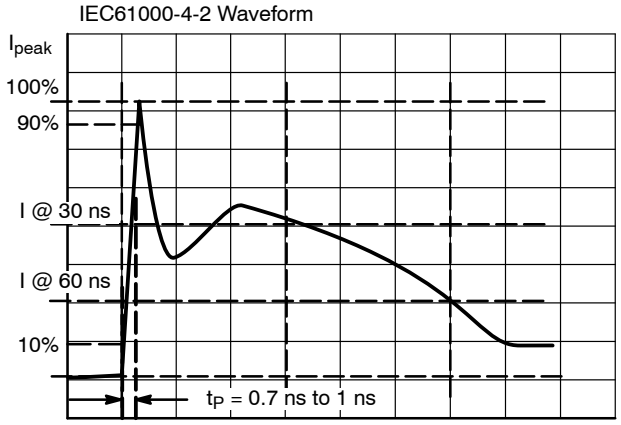


Figure 9. IEC61000-4-2 Spec

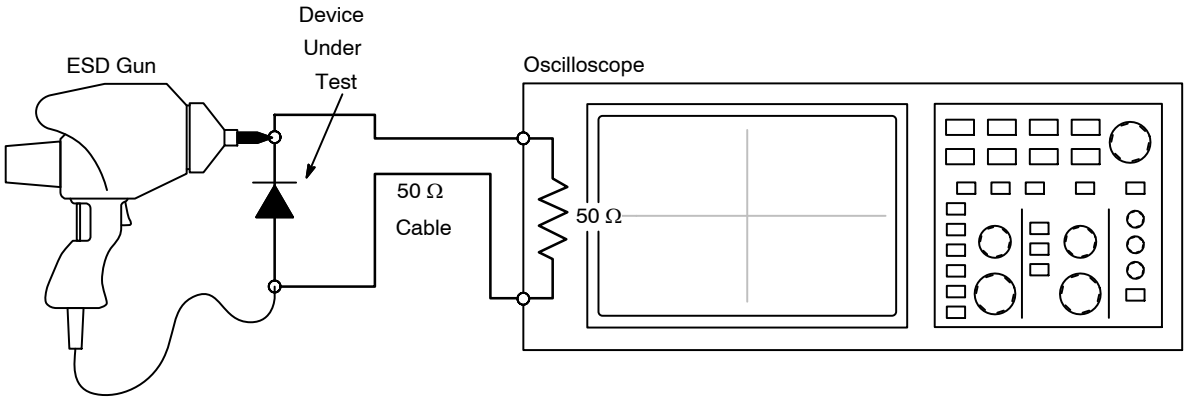


Figure 10. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the data sheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

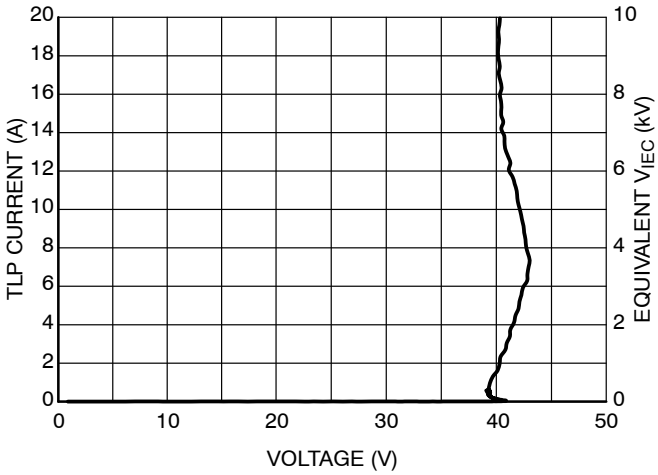


Figure 11. Positive TLP IV Curve

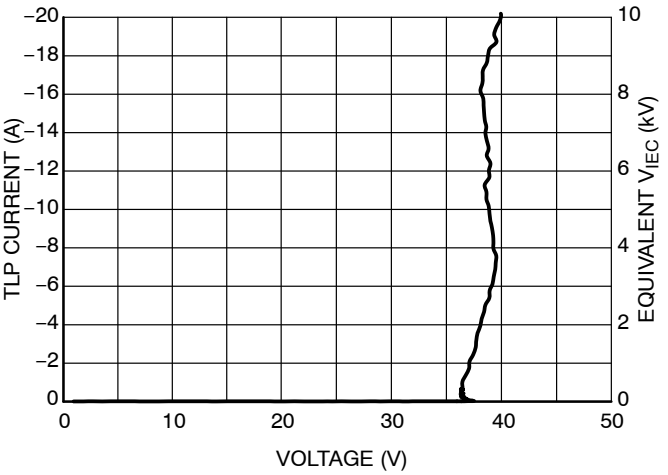


Figure 12. Negative TLP IV Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 13. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 14 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

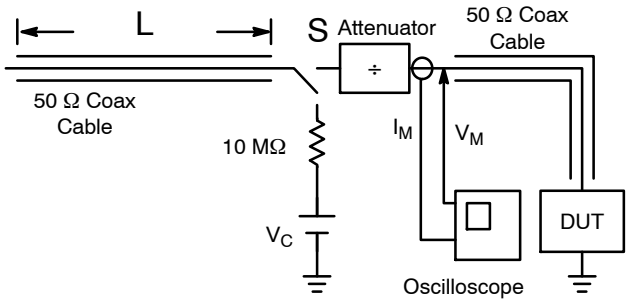


Figure 13. Simplified Schematic of a Typical TLP System

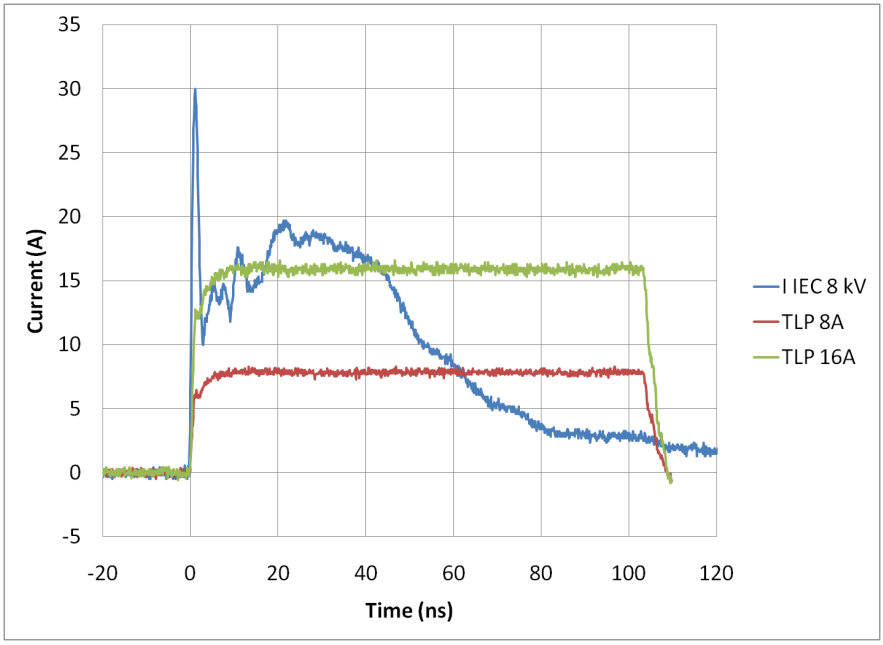


Figure 14. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

ORDERING INFORMATION

Device	Marking	Package	Operating Junction Temperature Range	Shipping†
NUP1128HT1G	7A	SOD-323 (Pb-Free)	−55 to 150 °C	3000 / Tape & Reel
SZNUP1128HT1G*				

DISCONTINUED (Note 6)

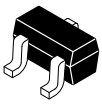
NUP1128WTT1G	7X	SC-70 (Pb-Free)	−55 to 175 °C	3000 / Tape & Reel
SZNUP1128WTT1G*				
NUP2128WTT1G	7U			
SZNUP2128WTT1G*				
NUPH1128HT1G	AL	SOD-323 (Pb-Free)		3000 / Tape & Reel
SZNUPH1128HT1G*				

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

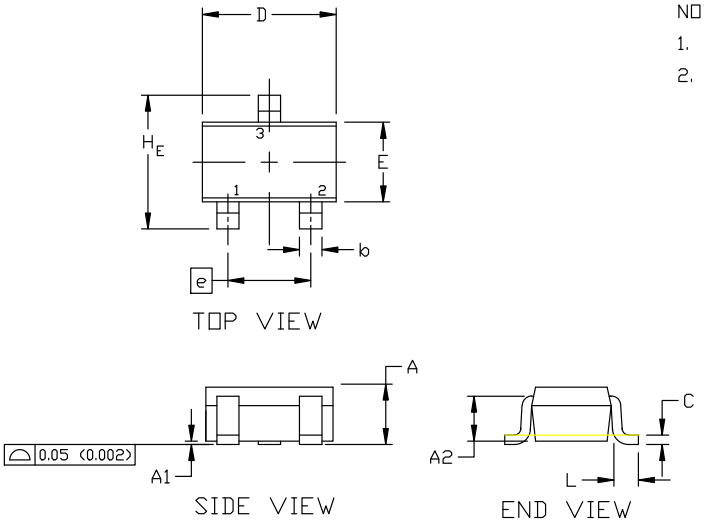
PACKAGE DIMENSIONS



SCALE 4:1

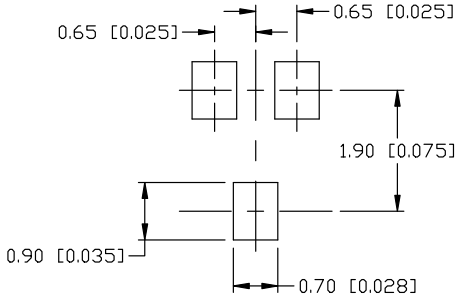
SC−70 (SOT−323)
CASE 419
ISSUE R

DATE 11 OCT 2022



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

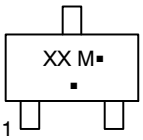
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.70 REF			0.028 BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.00	2.20	0.071	0.080	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

GENERIC MARKING DIAGRAM



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

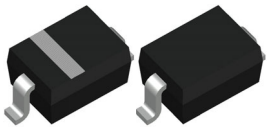
STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE−CATHODE

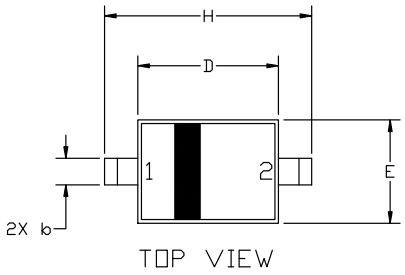
STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

PACKAGE DIMENSIONS



SOD−323 1.70x1.25x0.85
CASE 477
ISSUE K

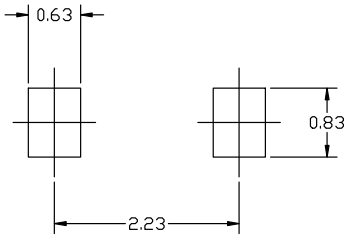
DATE 11 MAR 2024



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS SPECIFIED PER L/F DRAWING WITH SOLDER PLATING.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DIMENSION L IS MEASURE FROM END OF RADIUS.

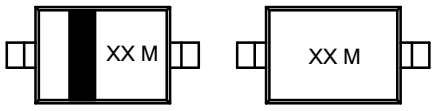
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.05	0.10
A2	0.75	0.85	0.95
A3	0.15 (REF)		
b	0.25	0.32	0.4
c	0.09	0.12	0.18
D	1.60	1.70	1.80
E	1.15	1.25	1.35
H	2.30	2.50	2.70
L	0.08	---	---
L1	0.40 (REF)		



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



STYLE 1 STYLE 2

XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

STYLE 2:
NO POLARITY

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales