

# MOSFET – Power, N-Channel

100 V, 1.4 mΩ

## NVCR4LS1D4N10MCA

### Features

- Typical  $R_{DS(on)}$  = 1.1 mΩ at  $V_{GS} = 10$  V
- Typical  $Q_{g(tot)}$  = 131 nC at  $V_{GS} = 10$  V
- AEC-Q101 Qualified
- RoHS Compliant

### DIMENSION (μm)

Die Size	7080 × 4515
Die Size (Sawn)	7060 ±15 × 4495 ±15
Source Attach Area	(6508 × 2055.6) × 2
Gate Attach Area	330 × 600
Die Thickness	101.6 ±19.1

Gate and Source: AlSiCu  
 Drain: Ti-NiV-Ag (back side of die)  
 Passivation: Polyimide  
 Wafer Diameter: 8 inch  
 Wafer Sawn on UV Tape  
 Bad Dice Identified in Inking  
 Gross Die Counts: 765

The Chip is 100% Probed to Meet the Conditions and Limits Specified at  $T_J = 25^{\circ}\text{C}$ .

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100	-	-	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	10	μA
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 799 \mu\text{A}$	2.0	-	4.0	V
* $R_{DS(on)}$	Bare Die Drain to Source On Resistance	$I_D = 40 \text{ A}, V_{GS} = 10 \text{ V}$	-	1.1	1.4	mΩ
* $V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 40 \text{ A}, V_{GS} = 0 \text{ V}$	-	-	1.3	V
$E_{AS}$	Single Pulse Drain-to-Source Avalanche Energy	$L = 0.3 \text{ mH}, I_{AS} = 65 \text{ A}$	633	-	-	mJ

\*Accurate  $R_{DS(on)}$ ,  $V_{SD}$  test at die level is not feasible as limited by the test contact precision attainable in a die form. The max  $R_{DS(on)}$ ,  $V_{SD}$  specification is defined from the historical performance of the die in package but is not guaranteed by test in production. The die  $R_{DS(on)}$  performance depends on the Source wire/ribbon bonding layout.



### ORDERING INFORMATION

Device	Package
NVCR4LS1D4N10MCA	Wafer Sawn on Foil

### RECOMMENDED STORAGE CONDITIONS

Temperature	22 to 28°C
RH	40 to 66%

# NVCR4LS1D4N10MCA

**MOSFET MAXIMUM RATINGS** in Reference to the NVBLS1D5N10MC electrical data in TOLL  
( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current $R_{\theta JC}$ ( $V_{GS} = 10$ ) (Note 1) $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	300 214	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	633	mJ
$P_D$	Power Dissipation $R_{\theta JC}$	331	W
	Derate Above $25^\circ\text{C}$	2.2	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	$-55$ to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.45	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	33	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Current is limited by silicon.
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.3$  mH,  $I_{AS} = 65$  A,  $V_{DD} = 100$  V during inductor charging and  $V_{DD} = 0$  V during time in avalanche.
- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a  $650$  mm<sup>2</sup> pad of 2oz copper.

**ELECTRICAL CHARACTERISTICS** in Reference to the NVBLS1D5N10MC electrical data in TOLL  
( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250$ $\mu\text{A}$ , $V_{GS} = 0$ V	100	–	–	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS} = 100$ V, $V_{GS} = 0$ V	–	–	10	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20$ V	–	–	$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 799$ $\mu\text{A}$	2.0	–	4.0	V
$R_{DS(on)}$	Drain to Source on Resistance	$I_D = 80$ A, $V_{GS} = 10$ V	–	1.2	1.5	m $\Omega$

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 50$ V, $V_{GS} = 0$ V, $f = 1$ MHz	–	10100	–	pF
$C_{oss}$	Output Capacitance		–	5100	–	pF
$C_{rss}$	Reverse Transfer Capacitance		–	84	–	pF
$Q_{g(ToT)}$	Total Gate Charge	$V_{GS} = 10$ V, $V_{DS} = 50$ V, $I_D = 80$ A	–	131	–	nC
$Q_{g(th)}$	Threshold Gate Charge		–	25	–	nC
$Q_{gs}$	Gate to Source Gate Charge		–	49	–	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		–	21	–	nC

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay	$V_{DS} = 50$ V, $I_D = 80$ A, $V_G = 10$ V, $R_G = 6$ $\Omega$	–	39	–	ns
$t_r$	Rise Time		–	71	–	ns
$t_{d(off)}$	Turn-Off Delay		–	83	–	ns
$t_f$	Fall Time		–	90	–	ns

### DRAIN-SOURCE DIODE CHARACTERISTIC

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 80$ A, $V_{GS} = 0$ V	–	–	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = 71$ A, $dI_{SD}/dt = 100$ A/ $\mu\text{s}$	–	110	–	ns
$Q_{rr}$	Reverse Recovery Charge		–	143	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## TYPICAL CHARACTERISTICS

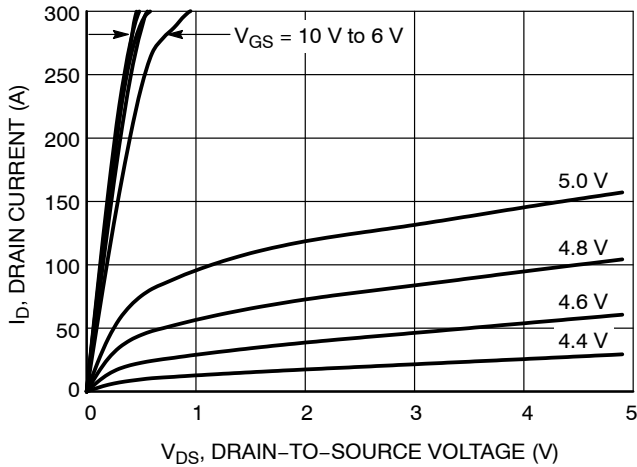


Figure 1. On-Region Characteristics

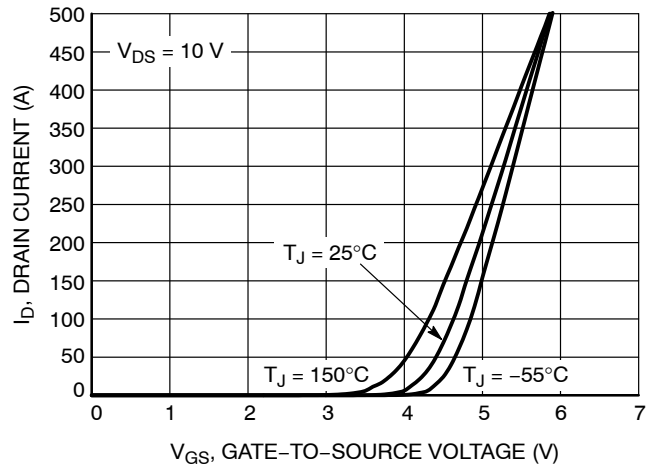


Figure 2. Transfer Characteristics

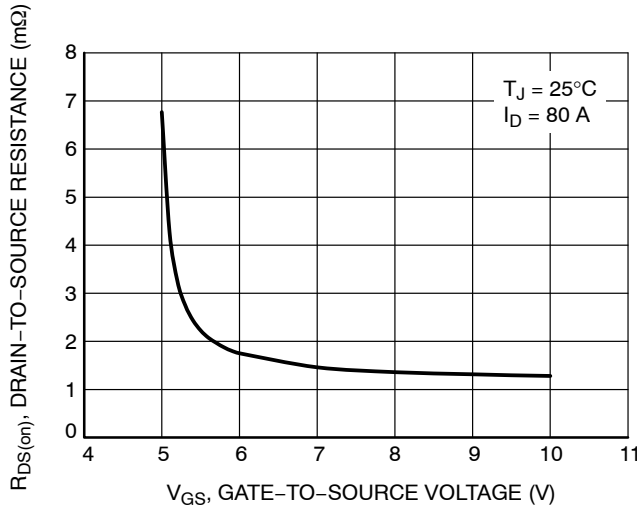


Figure 3. On-Resistance vs. Gate-to-Source Voltage

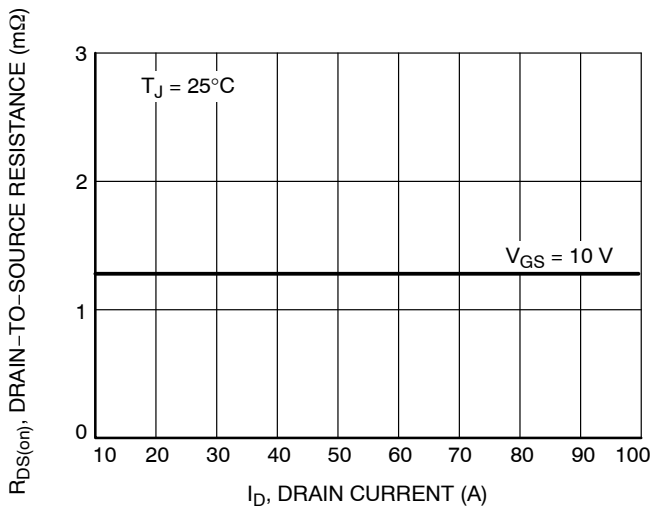


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

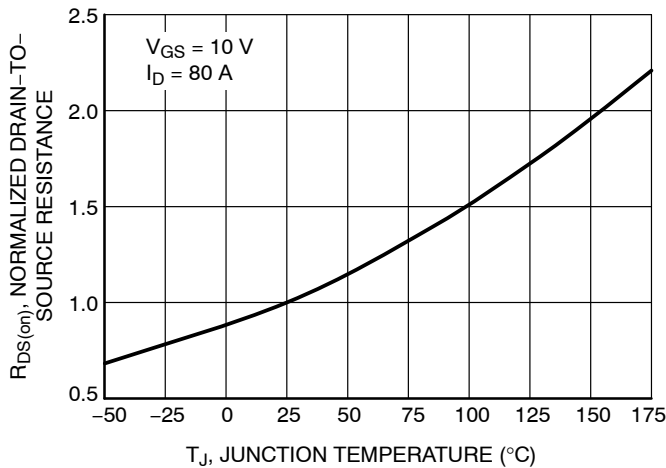


Figure 5. On-Resistance Variation with Temperature

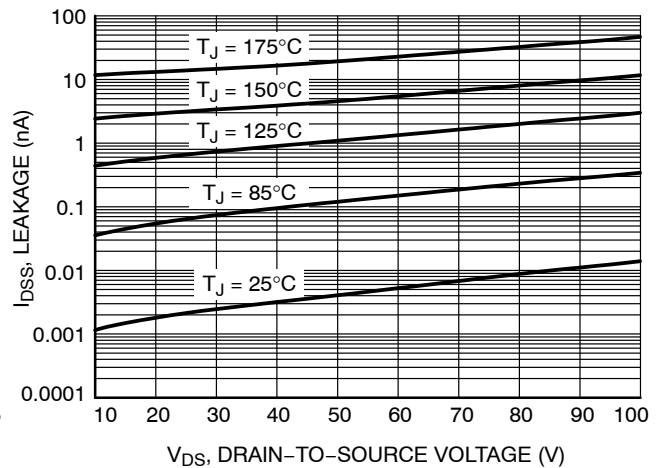


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS

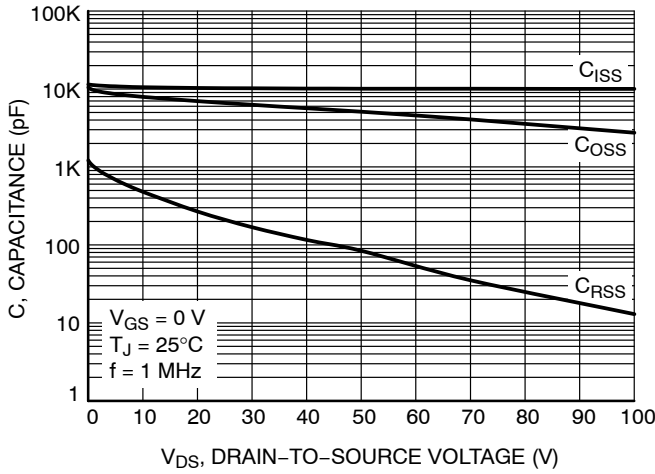


Figure 7. Capacitance Variation

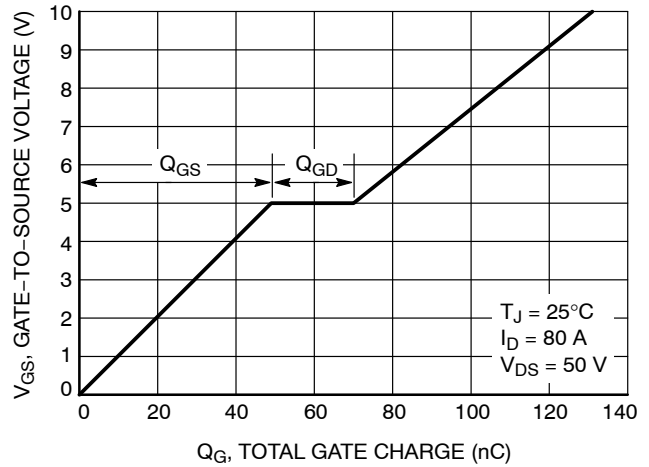


Figure 8. Gate-to-Source Voltage vs. Total Charge

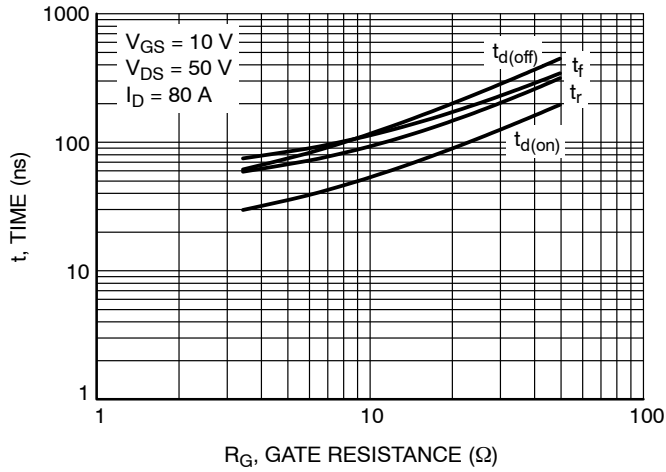


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

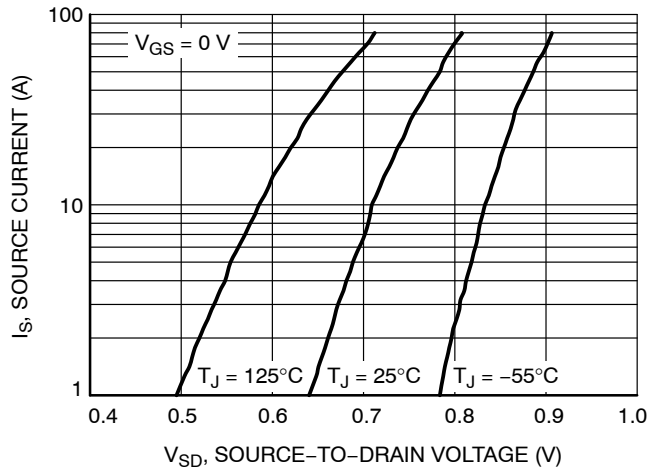


Figure 10. Diode Forward Voltage vs. Current

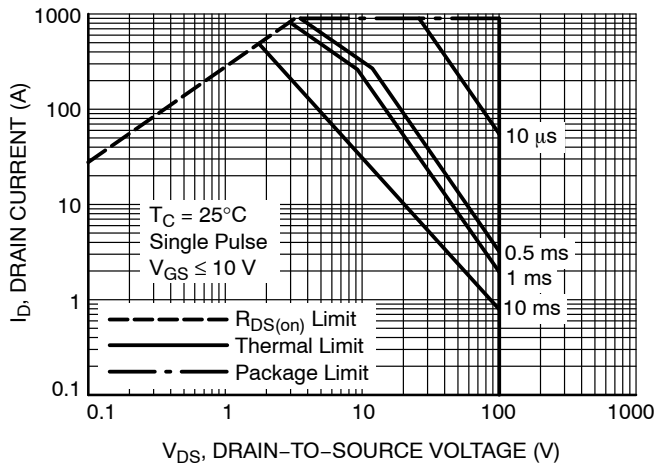


Figure 11. Maximum Rated Forward Biased Safe Operating Area

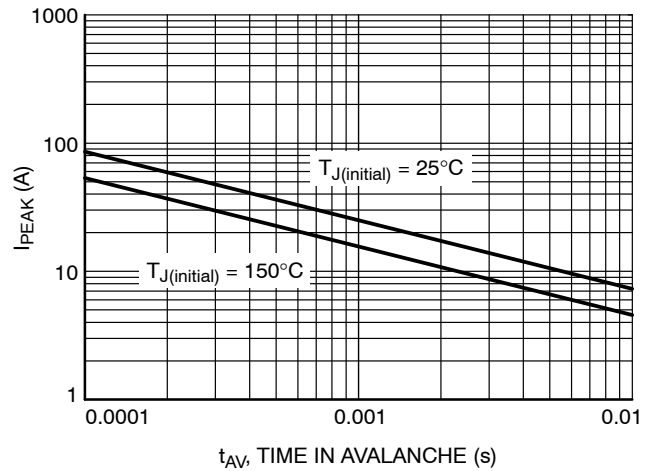


Figure 12. Maximum Drain Current vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS

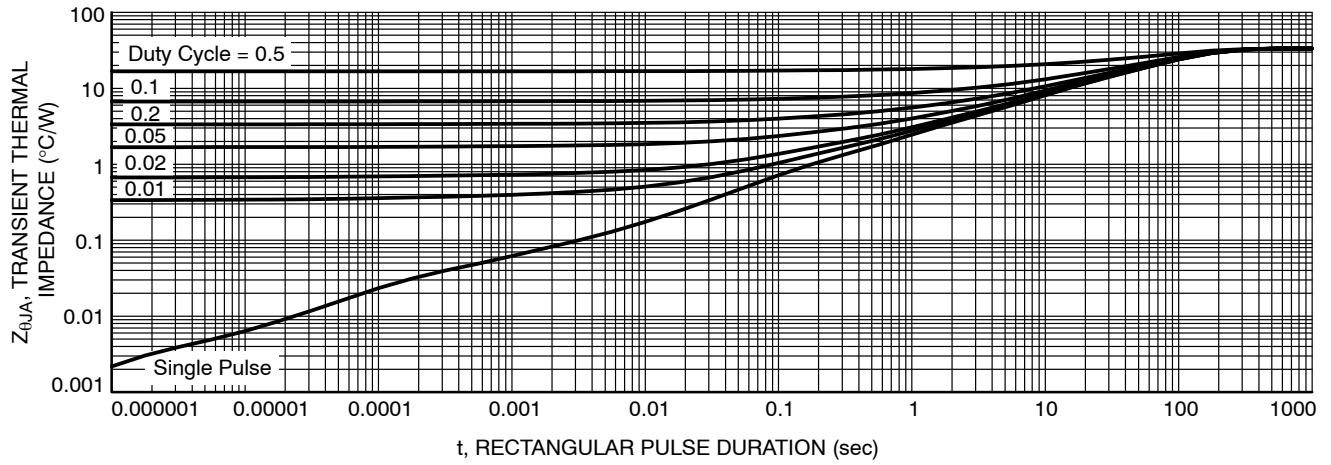


Figure 13. Transient Thermal Impedance

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