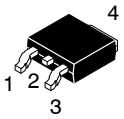
MOSFET – Power, Single N-Channel

60 V, 4.1 mΩ, 89 A

NVD5C648NL

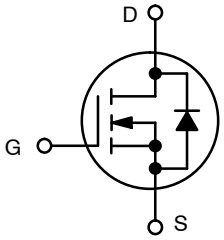
$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
60 V	4.1 mΩ @ 10 V	89 A
	5.7 mΩ @ 4.5 V	



DPAK
CASE 369C
STYLE 2

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant



N−CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain−to−Source Voltage			60	V
V_{GS}	Gate−to−Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	Steady State	T_C = 25°C	89	A
			T_C = 100°C	63	
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	72	W
			T_C = 100°C	36	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	Steady State	T_A = 25°C	18	A
			T_A = 100°C	13	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	T_A = 25°C	3.1	W
			T_A = 100°C	1.5	
I_{DM}	Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		510	A
T_J, T_{stg}	Operating Junction and Storage Temperature			−55 to 175	°C
I_S	Source Current (Body Diode)			85	A
E_{AS}	Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, $I_{L(pk)}$ = 7.0 A)			223	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

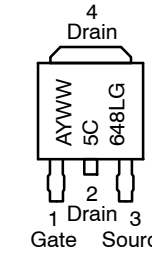
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction−to−Case (Drain) (Note 1)	2.07	°C/W
$R_{\theta JA}$	Junction−to−Ambient − Steady State (Note 2)	48.1	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location
Y = Year
WW = Work Week
5C648L = Device Code
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		60	–	–	V
$V_{(BR)DSS}/T_J$	Drain−to−Source Breakdown Voltage Temperature Coefficient			–	24	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C	–	–	10	μA
			T_J = 125°C	–	–	250	
I_{GSS}	Gate−to−Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V		–	–	100	nA
ON CHARACTERISTICS (Note 4)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		1.2	–	2.1	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient			–	5.2	–	mV/°C
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 45 A		–	3.4	4.1	mΩ
		V_{GS} = 4.5 V, I_D = 45 A		–	4.6	5.7	
g_{FS}	Forward Transconductance	V_{DS} = 5.0 V, I_D = 45 A		–	120	–	S
CHARGES, CAPACITANCES AND GATE RESISTANCES							
C_{iss}	Input Capacitance	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V		–	2900	–	pF
C_{oss}	Output Capacitance			–	1300	–	
C_{rss}	Reverse Transfer Capacitance			–	28	–	
$Q_{G(TOT)}$	Total Gate Charge	V_{DS} = 48 V, I_D = 45 A	V_{GS} = 4.5 V	–	17	–	nC
			V_{GS} = 10 V	–	39	–	
$Q_{G(TH)}$	Threshold Gate Charge	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 45 A		–	4.8	–	nC
Q_{GS}	Gate−to−Source Charge			–	8.8	–	
Q_{GD}	Gate−to−Drain Charge			–	3.5	–	
V_{GP}	Plateau Voltage			–	3.2	–	V
SWITCHING CHARACTERISTICS (Note 5)							
$t_{d(on)}$	Turn−On Delay Time	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 45 A, R_G = 2.5 Ω		–	21	–	ns
t_r	Rise Time			–	91	–	
$t_{d(off)}$	Turn−Off Delay Time			–	47	–	
t_f	Fall Time			–	68	–	
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 45 A	T_J = 25°C	–	0.9	1.2	V
			T_J = 125°C	–	0.8	–	
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 45 A		–	47	–	ns
ta	Charge Time			–	23	–	
tb	Discharge Time			–	24	–	
Q_{RR}	Reverse Recovery Charge			–	30	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

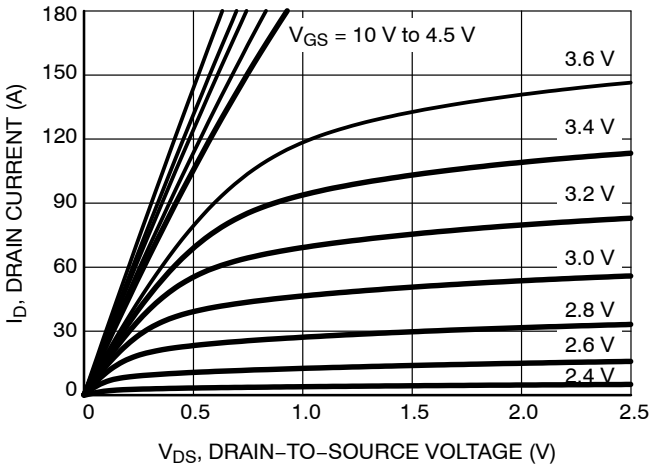


Figure 1. On−Region Characteristics

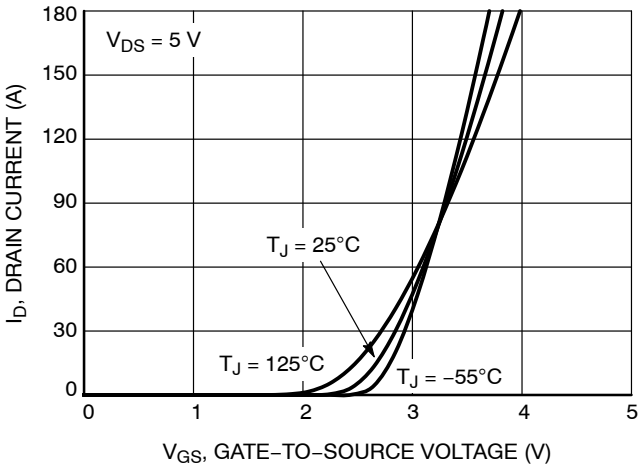


Figure 2. Transfer Characteristics

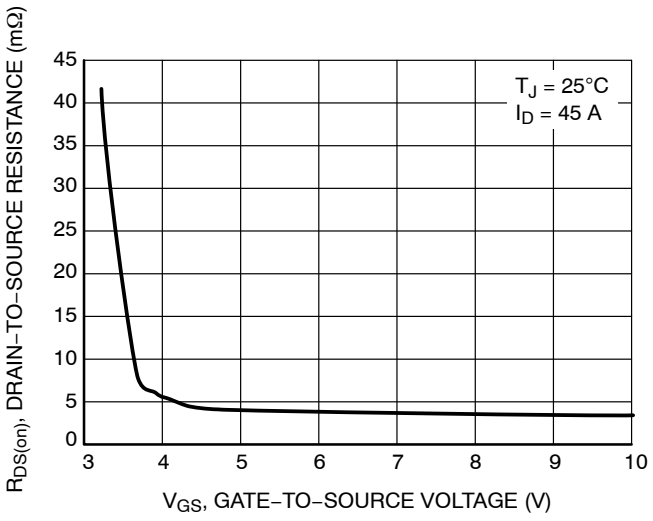


Figure 3. On−Resistance vs. Gate−to−Source Voltage

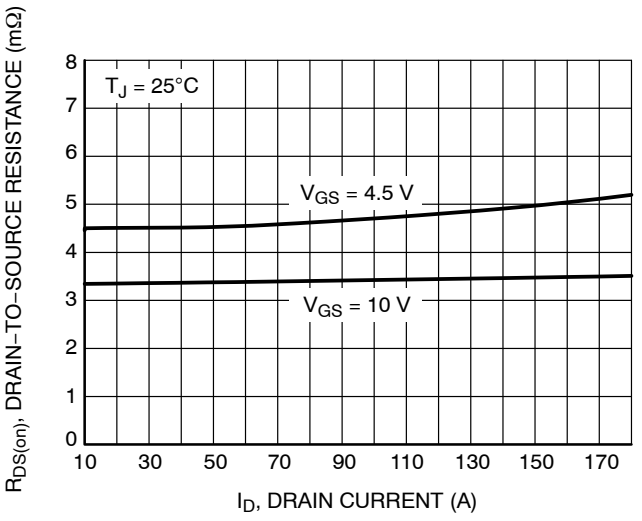


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

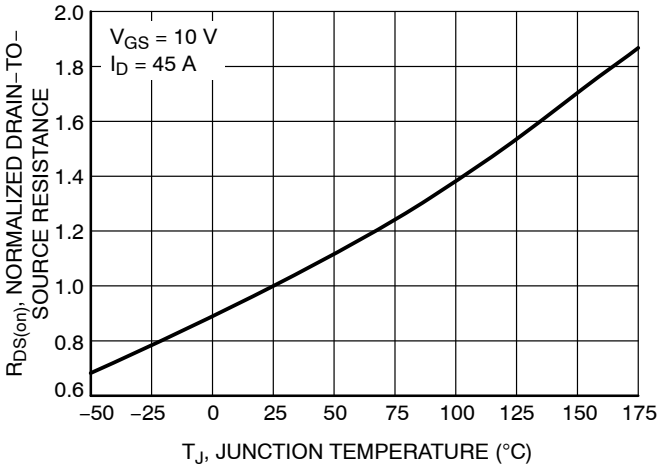


Figure 5. On−Resistance Variation with Temperature

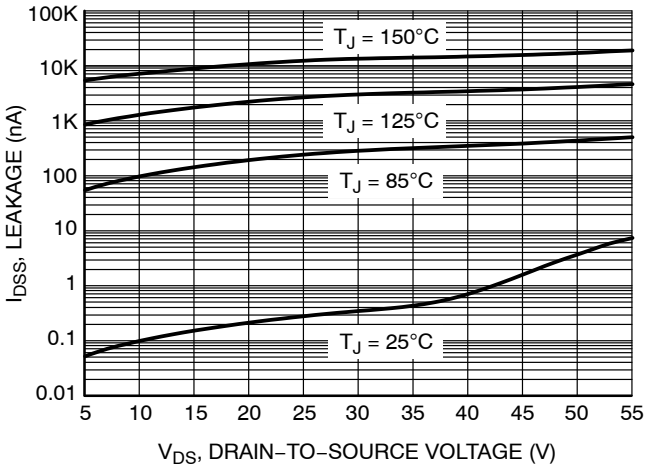


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

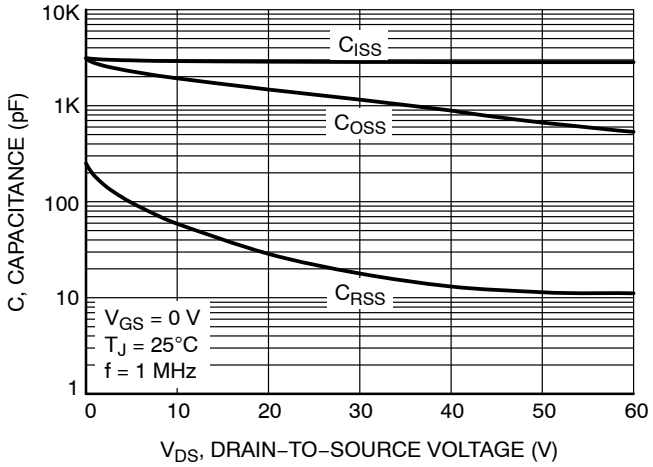


Figure 7. Capacitance Variation

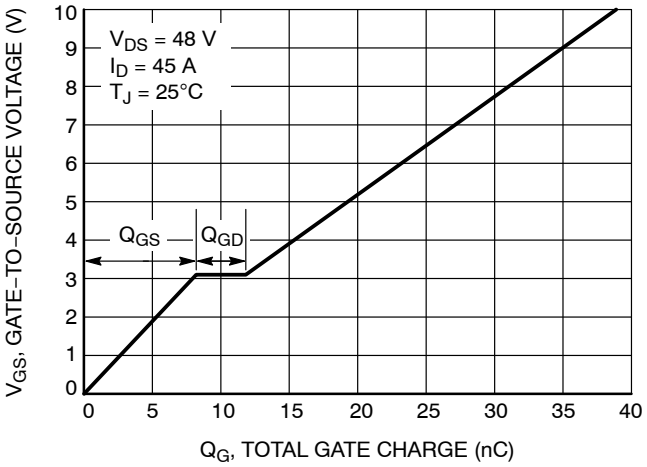


Figure 8. Gate−to−Source vs. Total Charge

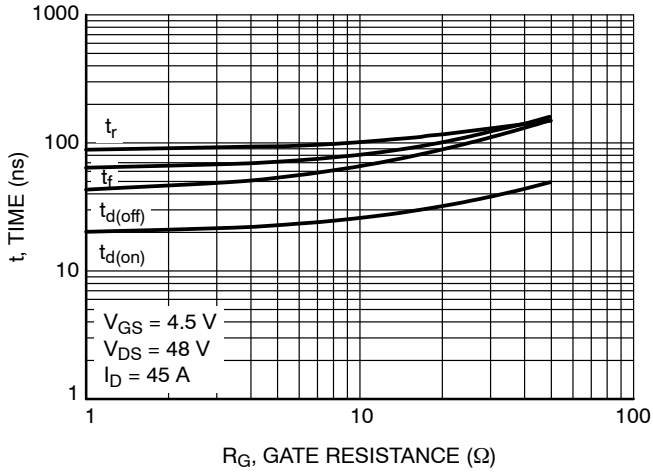


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

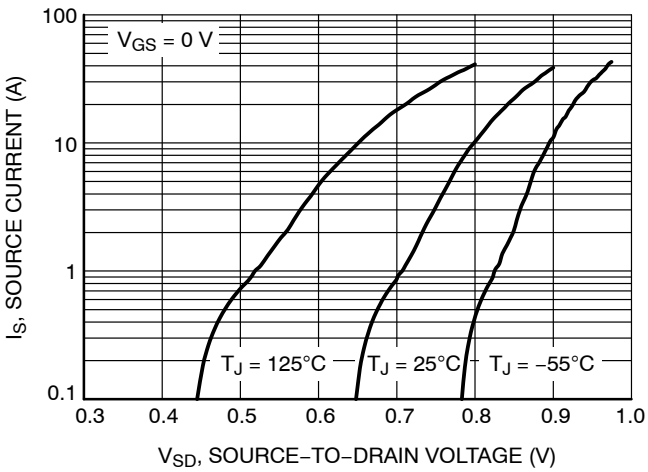


Figure 10. Diode Forward Voltage vs. Current

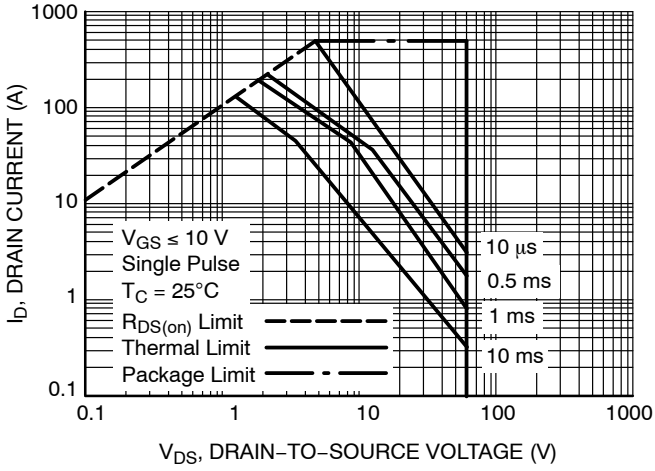


Figure 11. Maximum Rated Forward Biased Safe Operating Area

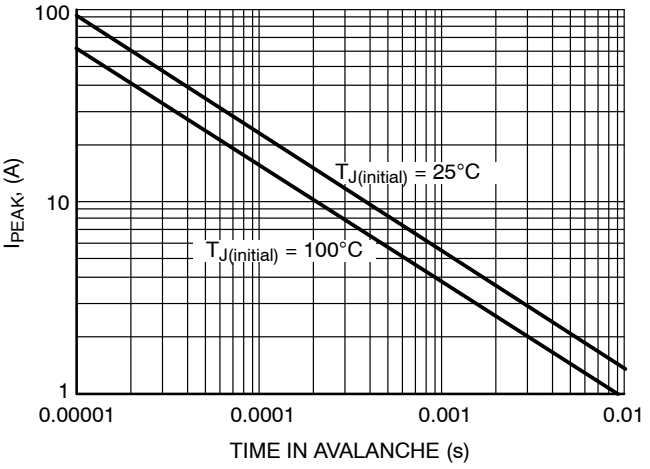


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)

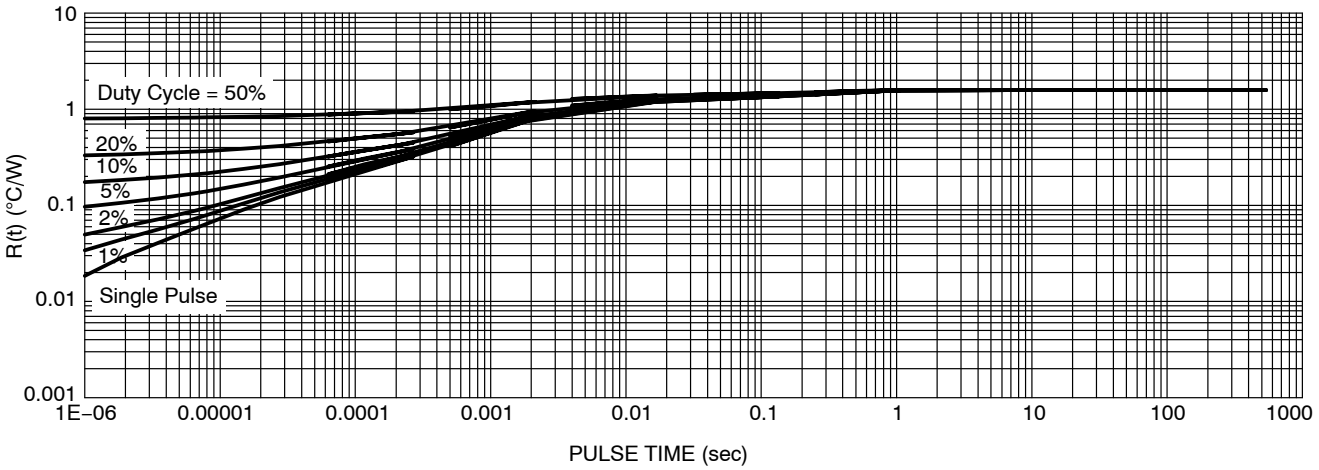
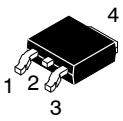


Figure 13. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping†
NVD5C648NLT4G	DPAK (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

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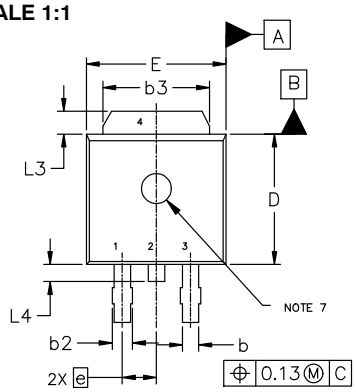
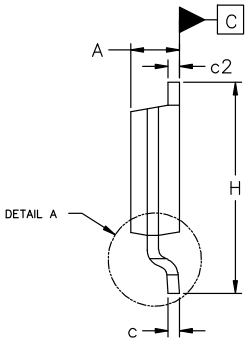
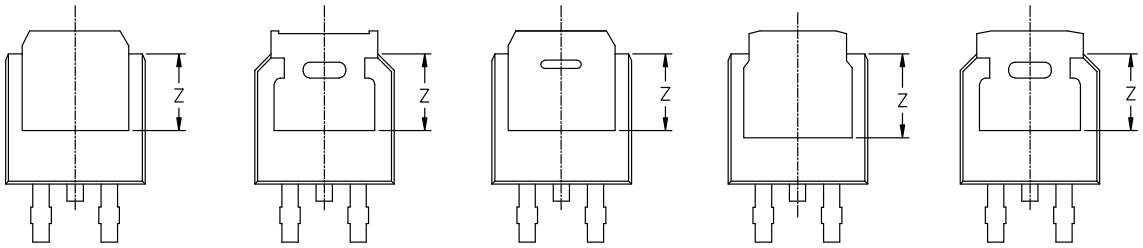


TOP VIEW



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---

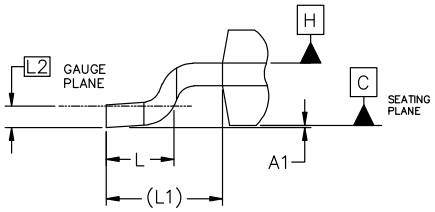


BOTTOM VIEW

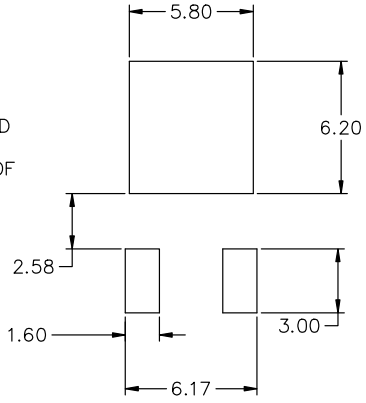
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

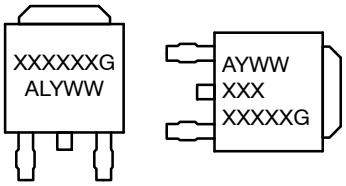
*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales