

# MOSFET – Power, Single N-Channel

## 60 V, 27.4 mΩ, 17 A

### NVD5C688NL

#### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	60	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 16$	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	Steady State	$T_C = 25\text{ }^\circ\text{C}$	$I_D$ 17	A
		$T_C = 100\text{ }^\circ\text{C}$	12	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25\text{ }^\circ\text{C}$	$P_D$ 18	W
		$T_C = 100\text{ }^\circ\text{C}$	9.0	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	$I_D$ 7.0	A
		$T_A = 100\text{ }^\circ\text{C}$	5.0	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	$P_D$ 2.9	W
		$T_A = 100\text{ }^\circ\text{C}$	1.45	
Pulsed Drain Current	$T_A = 25\text{ }^\circ\text{C}, t_p = 10\text{ }\mu\text{s}$	$I_{DM}$ 77	A	
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	20	A	
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25\text{ }^\circ\text{C}, I_{L(pk)} = 1\text{ A}$ )	$E_{AS}$	48	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

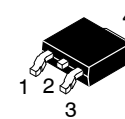
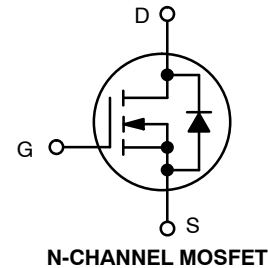
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Note 1)	$R_{\theta JC}$	8.05	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	51.6	

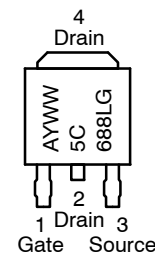
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$	$I_D$
60 V	27.4 mΩ @ 10 V	17 A
	40 mΩ @ 4.5 V	



**DPAK  
CASE 369C  
STYLE 2**

#### MARKING DIAGRAM & PIN ASSIGNMENT



- A = Assembly Location
- Y = Year
- WW = Work Week
- 5C688L = Device Code
- G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NVD5C688NL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			27		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V	T <sub>J</sub> = 25 °C		10	μA
			T <sub>J</sub> = 125 °C		250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 15 μA	1.2		2.1	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			4.4		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		22.8	27.4	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		32	40	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 10 A		20		S

### CHARGES, CAPACITANCES AND GATE RESISTANCES

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V		400		pF
Output Capacitance	C <sub>oss</sub>			170		
Reverse Transfer Capacitance	C <sub>rss</sub>			12		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>DS</sub> = 48 V, I <sub>D</sub> = 10 A	V <sub>GS</sub> = 4.5 V	3.4		nC
			V <sub>GS</sub> = 10 V	7.0		
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 10 A		0.9		nC
Gate-to-Source Charge	Q <sub>GS</sub>			1.5		
Gate-to-Drain Charge	Q <sub>GD</sub>			1.1		
Plateau Voltage	V <sub>GP</sub>			2.9		

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 10 A, R <sub>G</sub> = 2.5 Ω		8		ns
Rise Time	t <sub>r</sub>			42		
Turn-Off Delay Time	t <sub>d(off)</sub>			11		
Fall Time	t <sub>f</sub>			24		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10 A	T <sub>J</sub> = 25 °C		0.9	1.2	V
			T <sub>J</sub> = 125 °C		0.8		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 10 A		17		ns	
Charge Time	t <sub>a</sub>			8			
Discharge Time	t <sub>b</sub>			9			
Reverse Recovery Charge	Q <sub>RR</sub>			10			nC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

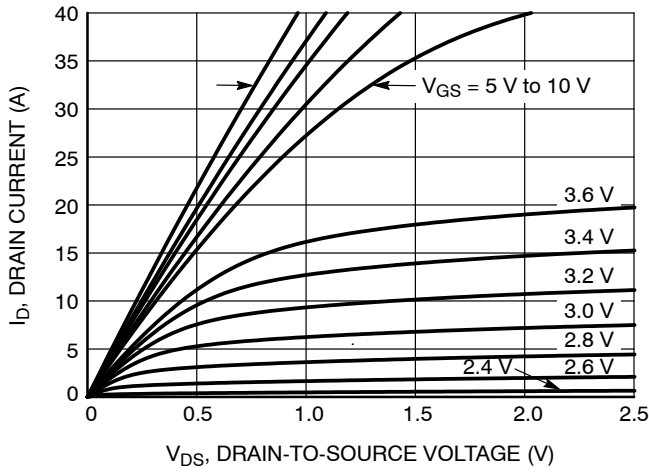


Figure 1. On-Region Characteristics

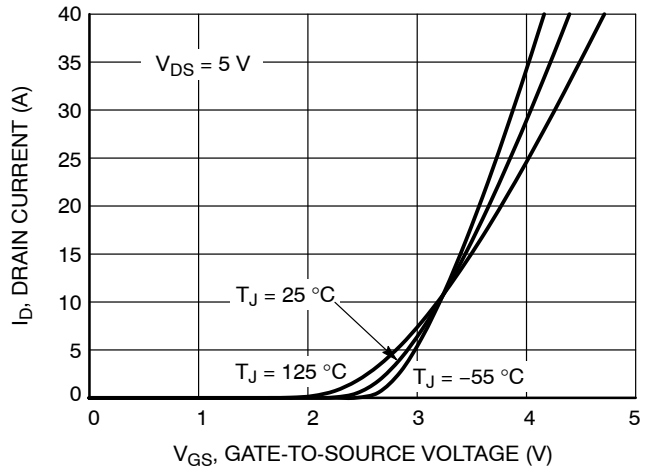


Figure 2. Transfer Characteristics

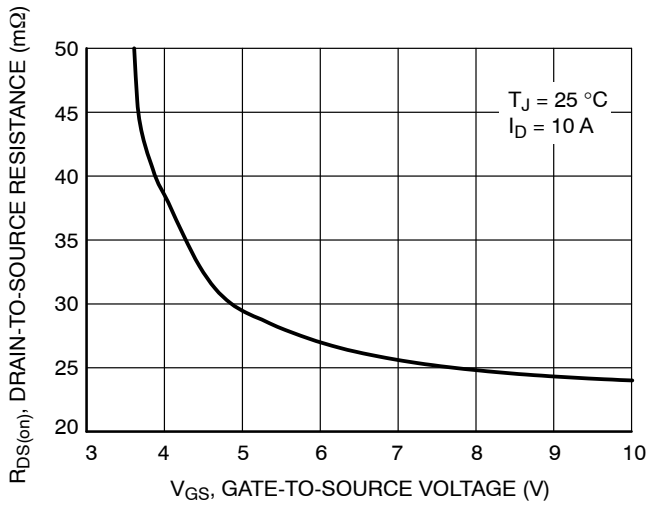


Figure 3. On-Resistance vs. Gate-to-Source Voltage

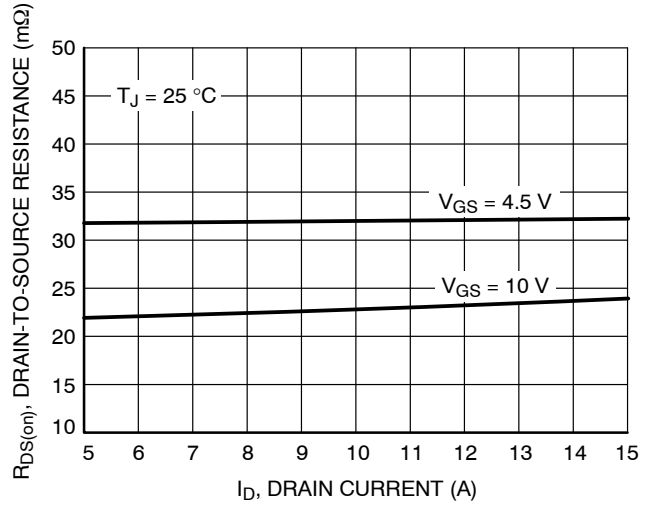


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

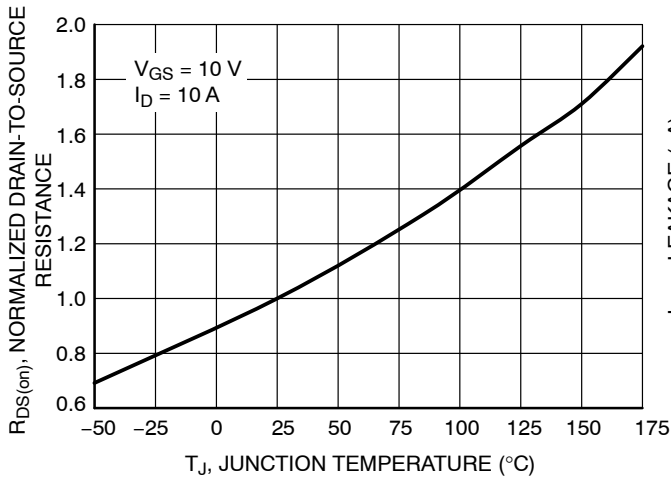


Figure 5. On-Resistance Variation with Temperature

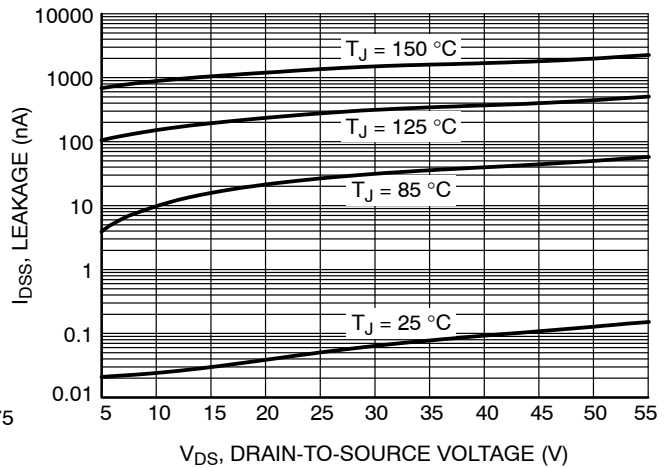


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS

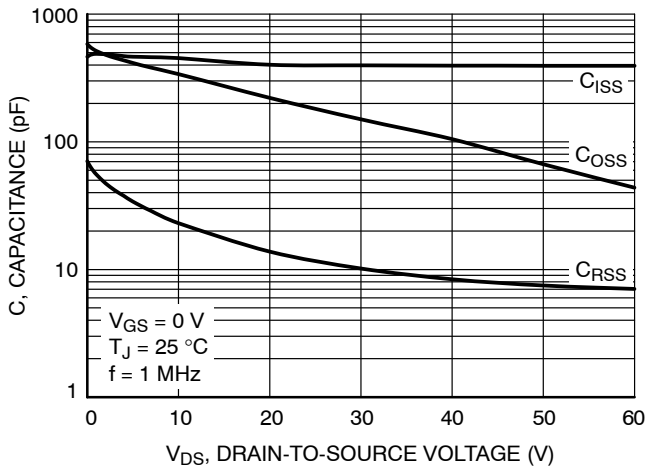


Figure 7. Capacitance Variation

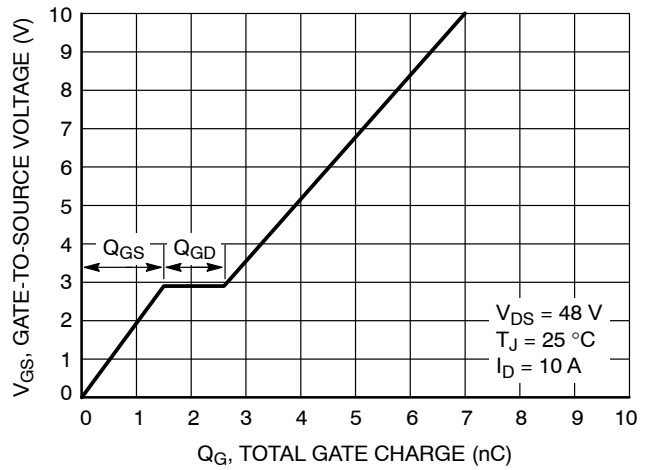


Figure 8. Gate-to-Source vs. Total Charge

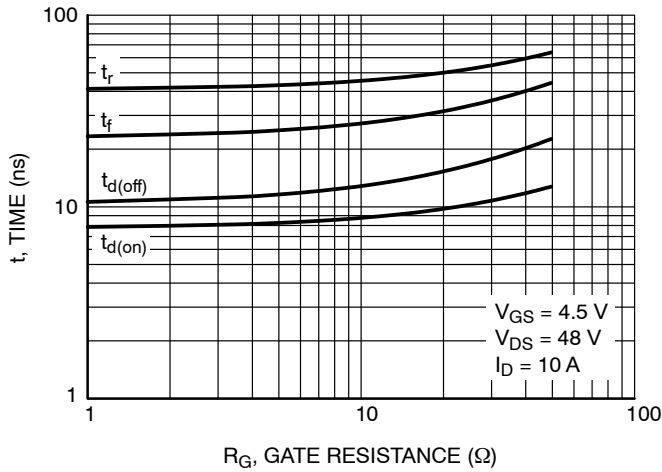


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

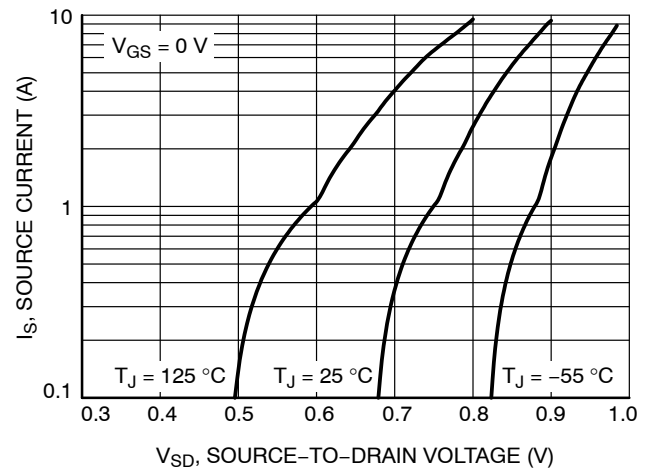


Figure 10. Diode Forward Voltage vs. Current

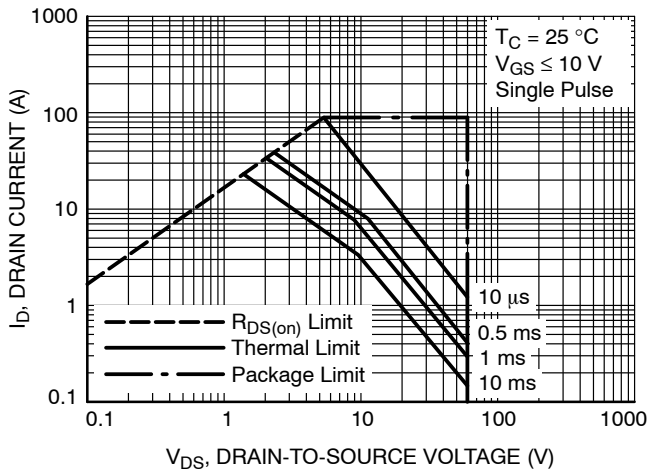


Figure 11. Maximum Rated Forward Biased Safe Operating Area

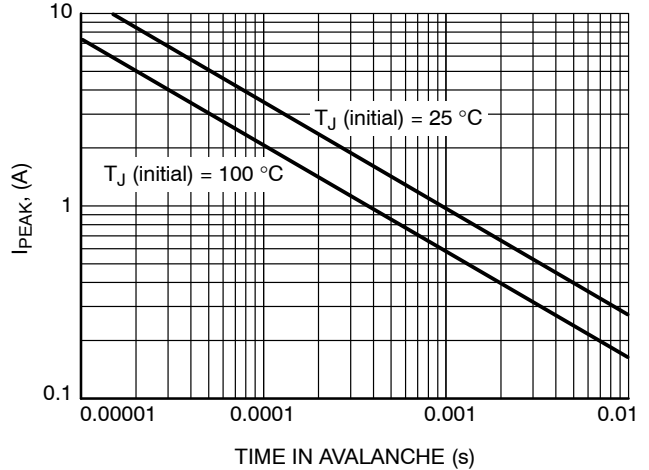


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS

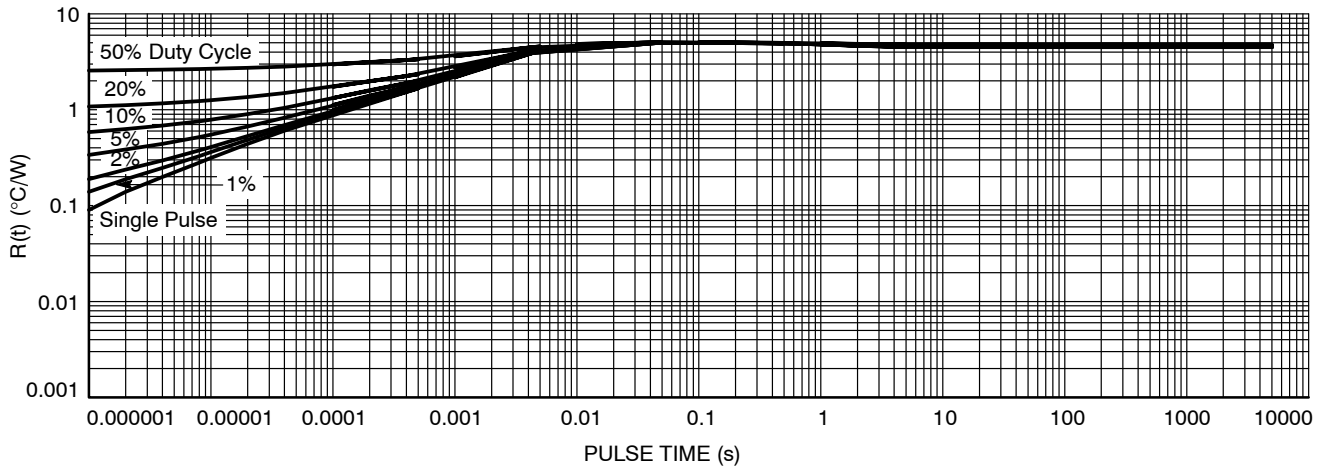


Figure 13. Thermal Response

### ORDERING INFORMATION

Order Number	Package	Shipping <sup>†</sup>
NVD5C688NLT4G	DPAK (Pb-Free)	2500 / Tape & Reel

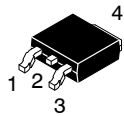
<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# NVD5C688NL

## REVISION HISTORY

Revision	Description of Changes	Date
3	Rebranding to <b>onsemi</b> format.	3/16/2026

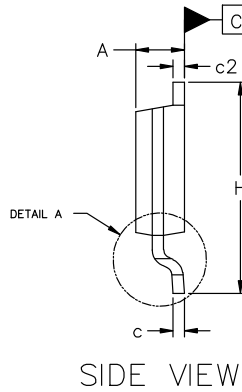
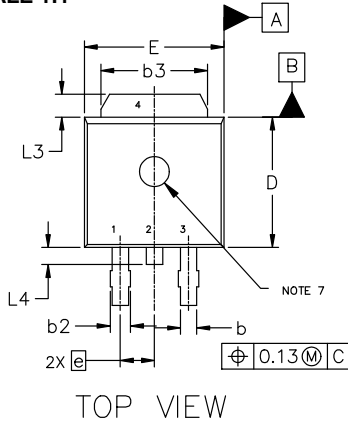
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



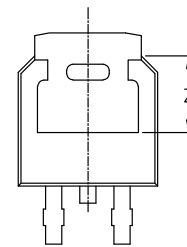
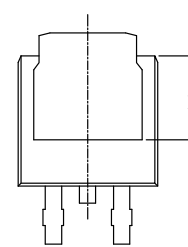
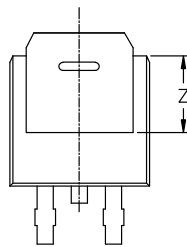
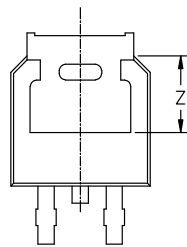
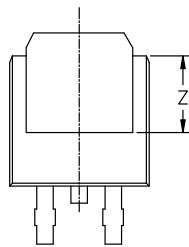
DPAK3 6.10x6.54x2.28, 2.29P  
CASE 369C  
ISSUE J

DATE 12 AUG 2025

SCALE 1:1



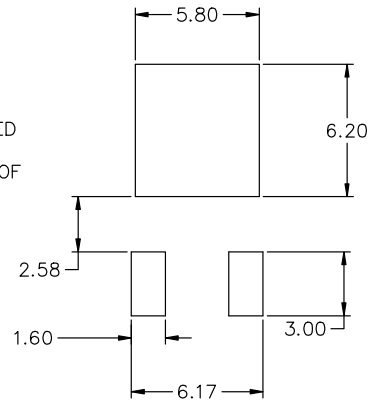
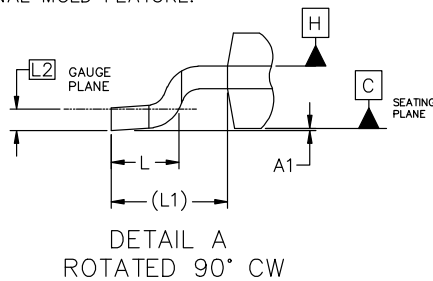
MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

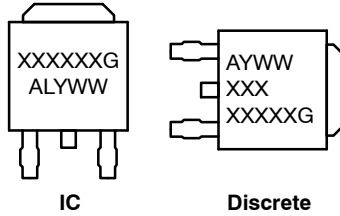
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**DPAK3 6.10x6.54x2.28, 2.29P**  
**CASE 369C**  
**ISSUE J**

DATE 12 AUG 2025

**GENERIC  
MARKING DIAGRAM\***



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- |  |  |   |   |  |
|--|--|---|---|--|
| <p>STYLE 1:<br/> PIN 1. BASE<br/> 2. COLLECTOR<br/> 3. EMITTER<br/> 4. COLLECTOR</p> | <p>STYLE 2:<br/> PIN 1. GATE<br/> 2. DRAIN<br/> 3. SOURCE<br/> 4. DRAIN</p>          | <p>STYLE 3:<br/> PIN 1. ANODE<br/> 2. CATHODE<br/> 3. ANODE<br/> 4. CATHODE</p> | <p>STYLE 4:<br/> PIN 1. CATHODE<br/> 2. ANODE<br/> 3. GATE<br/> 4. ANODE</p>              | <p>STYLE 5:<br/> PIN 1. GATE<br/> 2. ANODE<br/> 3. CATHODE<br/> 4. ANODE</p>     |
| <p>STYLE 6:<br/> PIN 1. MT1<br/> 2. MT2<br/> 3. GATE<br/> 4. MT2</p>                 | <p>STYLE 7:<br/> PIN 1. GATE<br/> 2. COLLECTOR<br/> 3. EMITTER<br/> 4. COLLECTOR</p> | <p>STYLE 8:<br/> PIN 1. N/C<br/> 2. CATHODE<br/> 3. ANODE<br/> 4. CATHODE</p>   | <p>STYLE 9:<br/> PIN 1. ANODE<br/> 2. CATHODE<br/> 3. RESISTOR ADJUST<br/> 4. CATHODE</p> | <p>STYLE 10:<br/> PIN 1. CATHODE<br/> 2. ANODE<br/> 3. CATHODE<br/> 4. ANODE</p> |

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