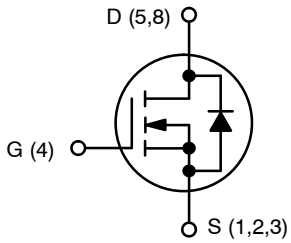
MOSFET – Power, Single N-Channel

40 V, 1.7 mΩ, 185 A

NVMJS1D7N04C

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	1.7 mΩ @ 10 V	185 A

LFPAK8
CASE 760AA



N–CHANNEL MOSFET

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPAK8 Package, Industry Standard
- AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain–to–Source Voltage			40	V
V_{GS}	Gate–to–Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	185	A
			T_C = 100°C	131	
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	106	W
			T_C = 100°C	53	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	35	A
			T_A = 100°C	25	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	3.8	W
			T_A = 100°C	1.9	
I_{DM}	Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		900	A
T_J, T_{stg}	Operating Junction and Storage Temperature Range			−55 to +175	°C
I_S	Source Current (Body Diode)			102	A
E_{AS}	Single Pulse Drain–to–Source Avalanche Energy ($I_{L(pk)}$ = 15 A)			338	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

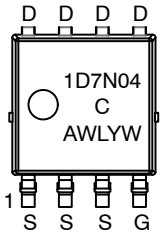
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction–to–Case – Steady State	1.4	°C/W
$R_{\theta JA}$	Junction–to–Ambient – Steady State (Note 2)	36	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface–mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



1D7N04C = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		40			V
$V_{(BR)DSS}/T_J$	Drain−to−Source Breakdown Voltage Temperature Coefficient				21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25 °C			10	μA
			T_J = 125°C			100	
I_{GSS}	Gate−to−Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 130 μA		2.5		3.5	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient				−7.8		mV/°C
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V	I_D = 50 A		1.36	1.7	mΩ
g_{FS}	Forward Transconductance	V_{DS} =15 V, I_D = 50 A			130		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			3300		pF
C_{OSS}	Output Capacitance				1600		
C_{RSS}	Reverse Transfer Capacitance				45		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 50 A			47		nC
$Q_{G(TH)}$	Threshold Gate Charge	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 50 A			10		
Q_{GS}	Gate−to−Source Charge				16		
Q_{GD}	Gate−to−Drain Charge				7.0		
V_{GP}	Plateau Voltage				4.7		V
SWITCHING CHARACTERISTICS (Note 5)							
$t_{d(ON)}$	Turn−On Delay Time	V_{GS} = 10 V, V_{DS} = 20 V, I_D = 50 A, R_G = 2.5 Ω			13		ns
t_r	Rise Time				48		
$t_{d(OFF)}$	Turn−Off Delay Time				29		
t_f	Fall Time				8.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.83	1.2	V
			T_J = 125°C		0.7		
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 50 A			57		ns
t_a	Charge Time				30		
t_b	Discharge Time				27		
Q_{RR}	Reverse Recovery Charge				68		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

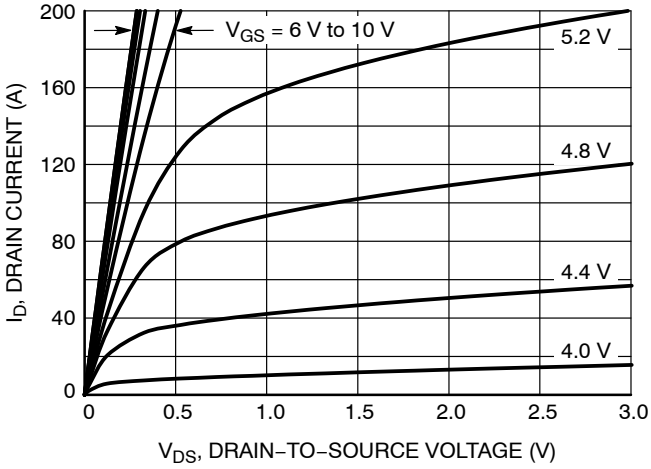


Figure 1. On−Region Characteristics

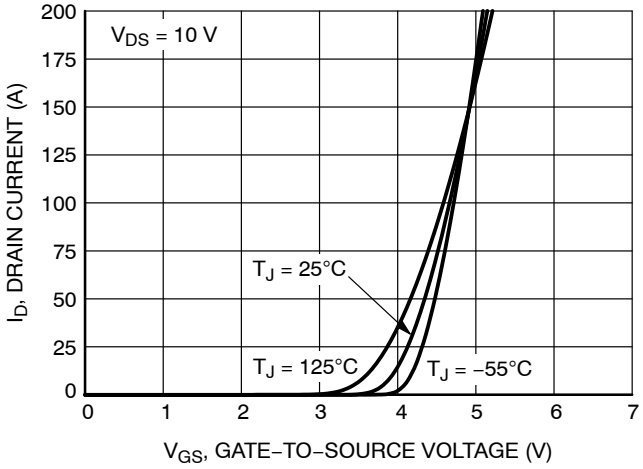


Figure 2. Transfer Characteristics

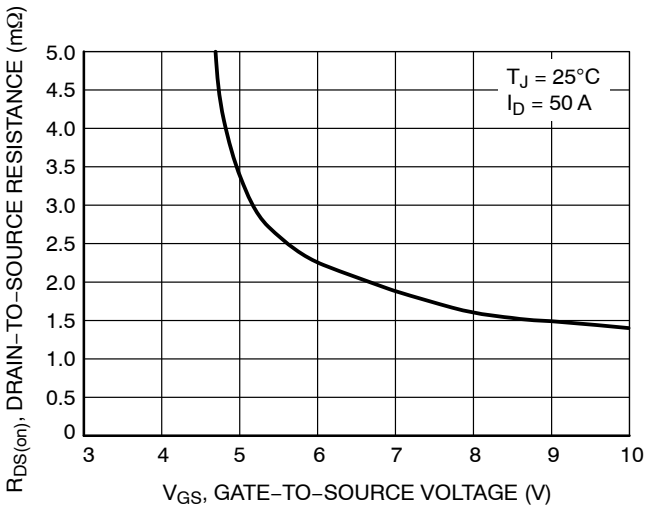


Figure 3. On−Resistance vs. Gate−to−Source Voltage

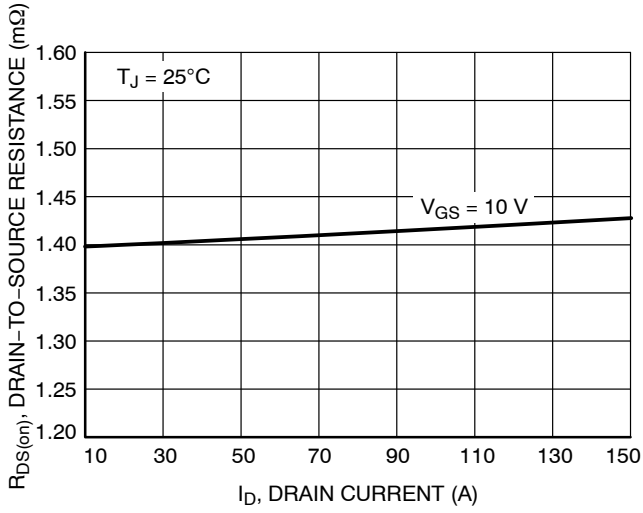


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

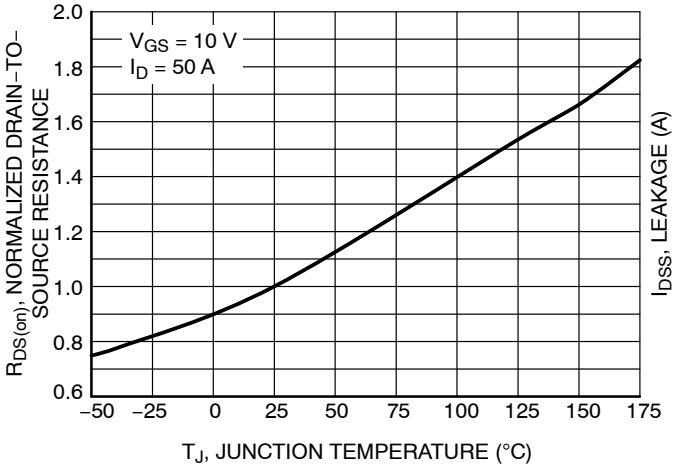


Figure 5. On−Resistance Variation with Temperature

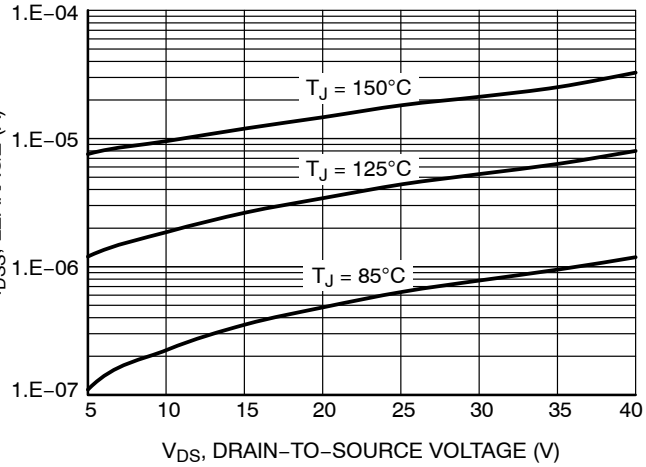


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

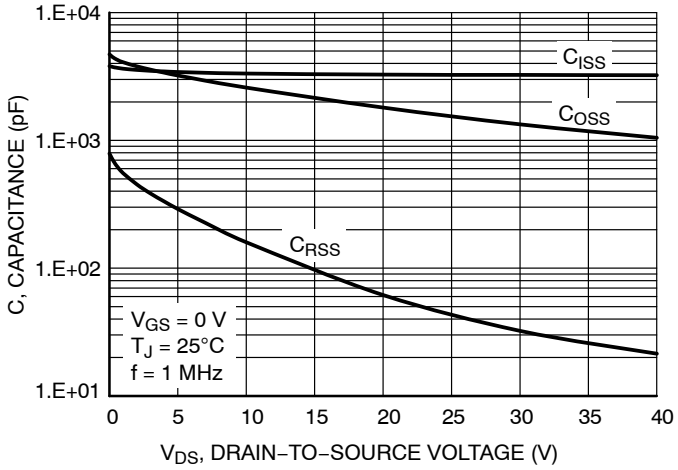


Figure 7. Capacitance Variation

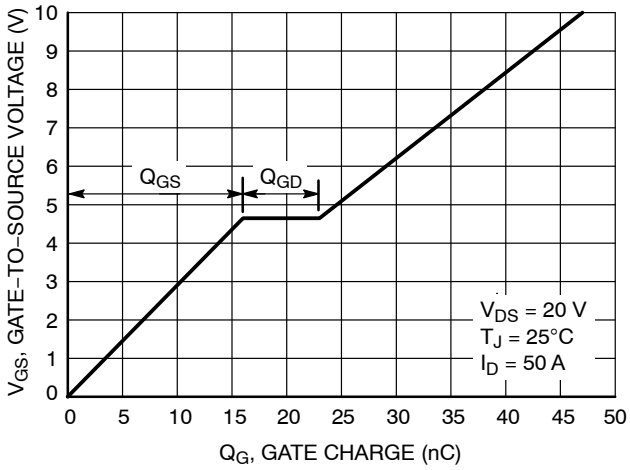


Figure 8. Gate−to−Source Voltage vs. Charge

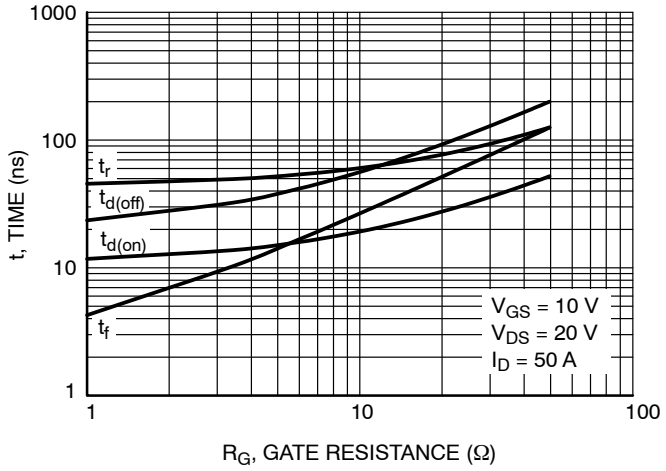


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

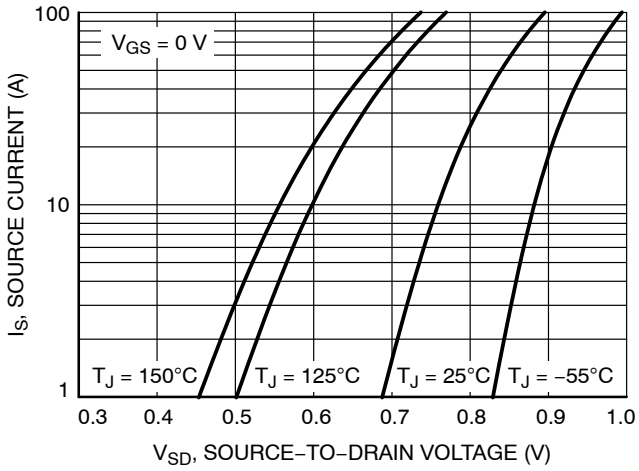


Figure 10. Diode Forward Voltage vs. Current

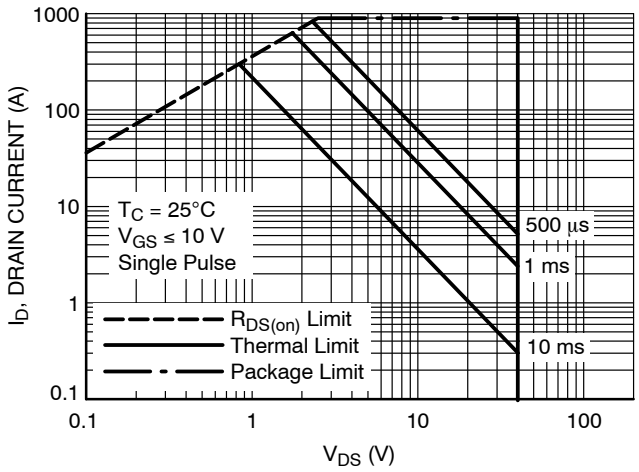


Figure 11. Safe Operating Area

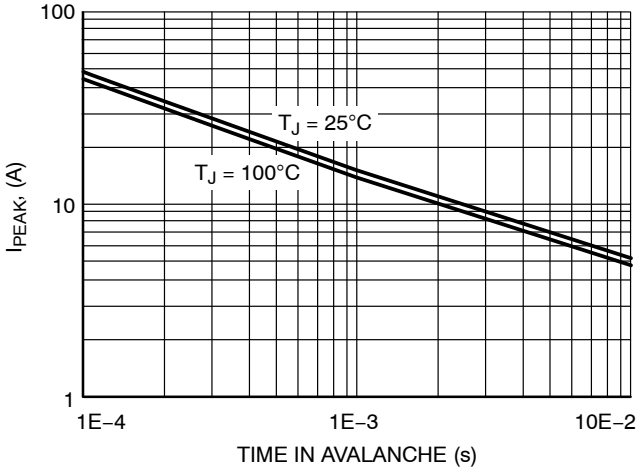


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)

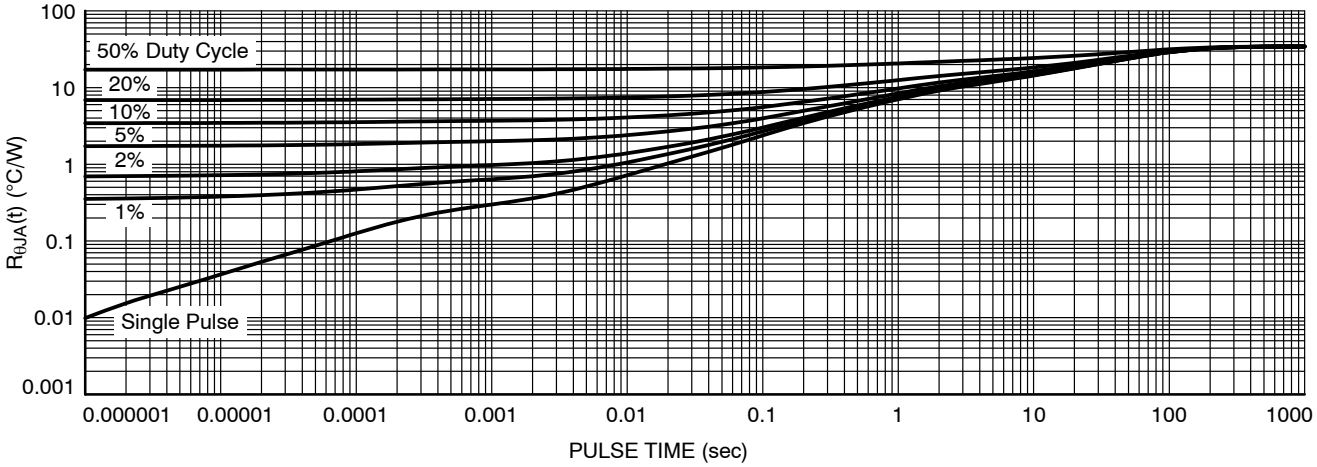


Figure 13. Thermal Characteristics

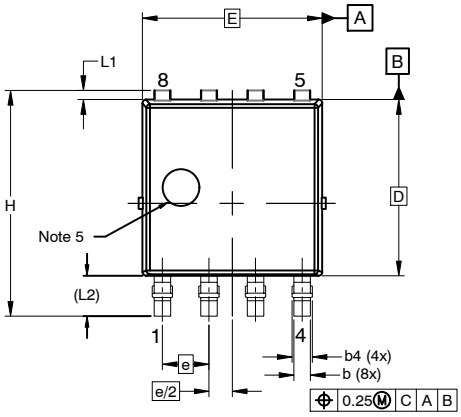
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMJS1D7N04CTWG	1D7N04C	LFPAK8 (Pb−Free)	3,000 / Tape & Reel

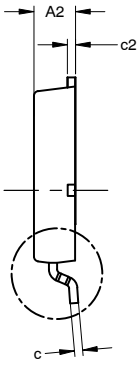
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

LFPAK8 4.90x4.80x1.12MM, 1.27P
CASE 760AA
ISSUE D

DATE 22 APR 2024

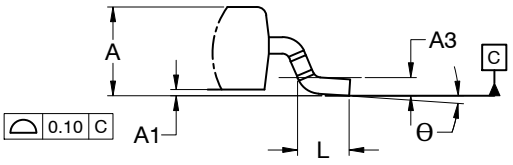


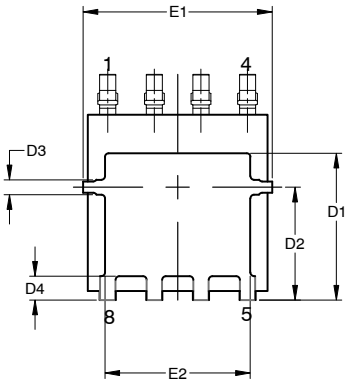
TOP VIEW



SIDE VIEW

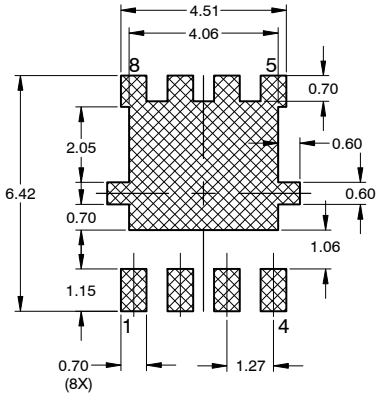
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. OPTIONAL MOLD FEATURE.





BOTTOM VIEW

DETAIL 'A'

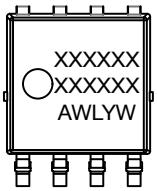


RECOMMENDED LAND PAD

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3		0.25 BSC	
b	0.40	0.45	0.50
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.70	4.80	4.90
D1	3.80	4.00	4.20
D2	2.98	3.08	3.18
D3	0.30	0.40	0.50
D4	0.55	0.65	0.75
E	4.80	4.90	5.00
E1	5.05	5.15	5.25
E2	3.91	3.96	4.01
e		1.27 BSC	
e/2		0.635 BSC	
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.15	0.25	0.35
L2		1.10 REF	
θ	0°	4°	8°

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON82475G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**LFPAK8 4.90x4.80x1.12MM, 1.27P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales