

MOSFET – Power, Single N-Channel

40 V, 1.7 mΩ, 185 A

NVMJS1D7N04C

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPK8 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter			Value	Unit
V _{DSS}	Drain-to-Source Voltage			40	V
V _{GS}	Gate-to-Source Voltage			±20	V
I _D	Continuous Drain Current R _{θJC} (Notes 1, 3)	Steady State	T _C = 25°C	185	A
			T _C = 100°C	131	
P _D	Power Dissipation R _{θJC} (Note 1)		T _C = 25°C	106	W
			T _C = 100°C	53	
I _D	Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	Steady State	T _A = 25°C	35	A
			T _A = 100°C	25	
P _D	Power Dissipation R _{θJA} (Notes 1, 2)		T _A = 25°C	3.8	W
			T _A = 100°C	1.9	
I _{DM}	Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		900	A
T _J , T _{stg}	Operating Junction and Storage Temperature Range			-55 to +175	°C
I _S	Source Current (Body Diode)			102	A
E _{AS}	Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 15 A)			338	mJ
T _L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

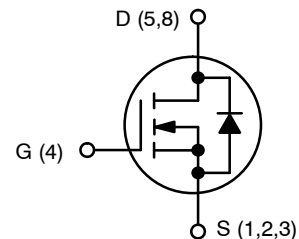
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State	1.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	36	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	1.7 mΩ @ 10 V	185 A

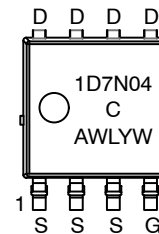


**LFPK8
CASE 760AA**



N-CHANNEL MOSFET

MARKING DIAGRAM



1D7N04C = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMJS1D7N04C

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		100	
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 130\text{ }\mu\text{A}$	2.5		3.5	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient			-7.8		mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		1.36	1.7	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 50\text{ A}$		130		S

CHARGES, CAPACITANCES & GATE RESISTANCE

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$		3300		μF
C_{OSS}	Output Capacitance			1600		
C_{RSS}	Reverse Transfer Capacitance			45		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$		47		nC
$Q_{G(TH)}$	Threshold Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$		10		
Q_{GS}	Gate-to-Source Charge	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$		16		
Q_{GD}	Gate-to-Drain Charge	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$		7.0		
V_{GP}	Plateau Voltage			4.7		V

SWITCHING CHARACTERISTICS (Note 5)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}, I_D = 50\text{ A}, R_G = 2.5\text{ }\Omega$		13		ns
t_r	Rise Time			48		
$t_{d(OFF)}$	Turn-Off Delay Time			29		
t_f	Fall Time			8.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 50 A	T _J = 25°C		0.83	1.2	V
			T _J = 125°C		0.7		
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A			57		ns
t _a	Charge Time				30		
t _b	Discharge Time				27		
Q _{RR}	Reverse Recovery Charge					68	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

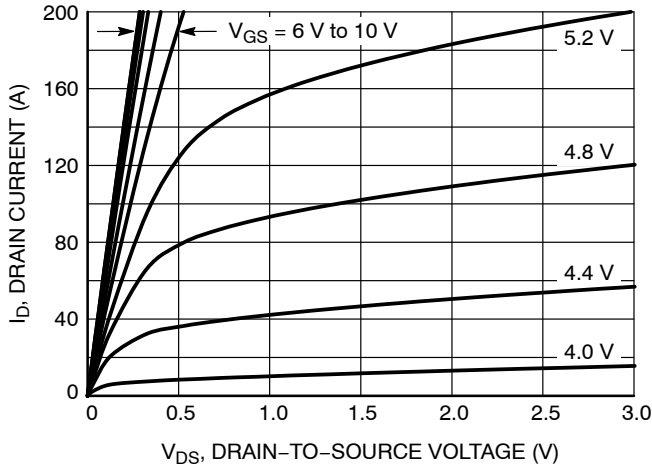


Figure 1. On-Region Characteristics

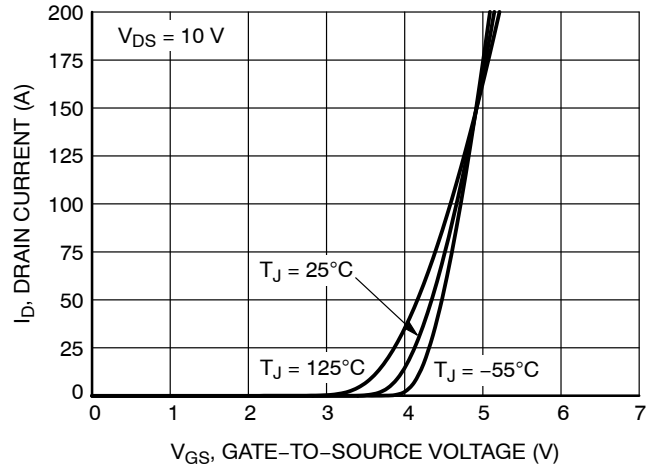


Figure 2. Transfer Characteristics

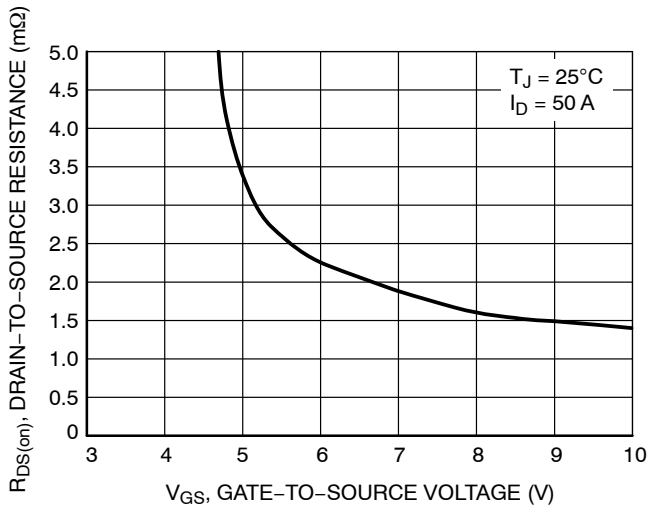


Figure 3. On-Resistance vs. Gate-to-Source Voltage

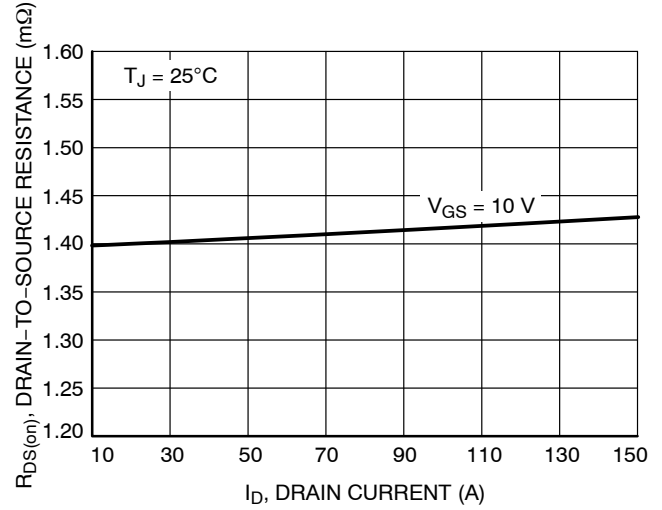


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

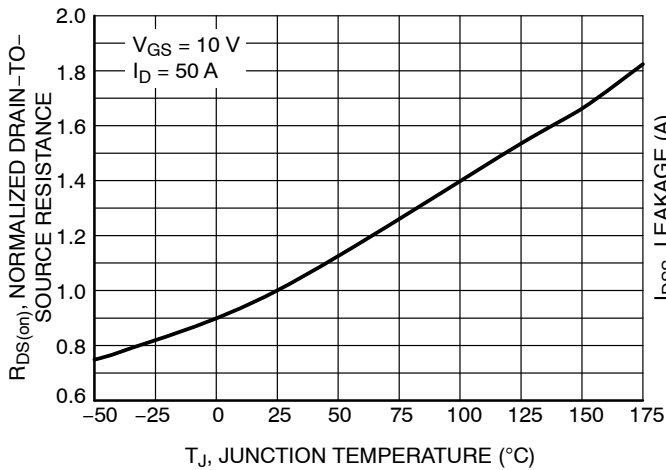


Figure 5. On-Resistance Variation with Temperature

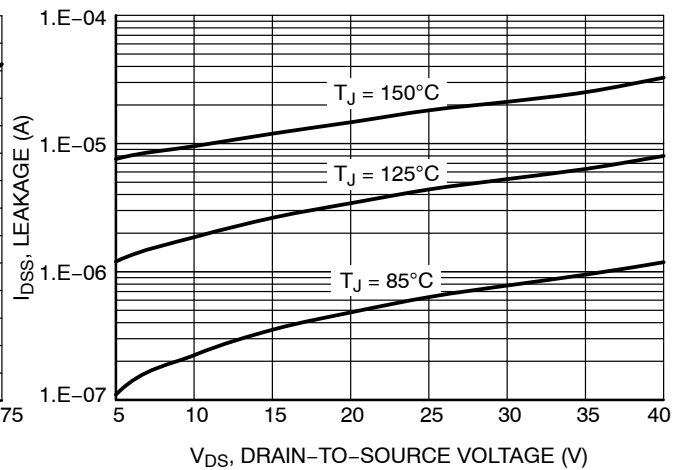


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (continued)

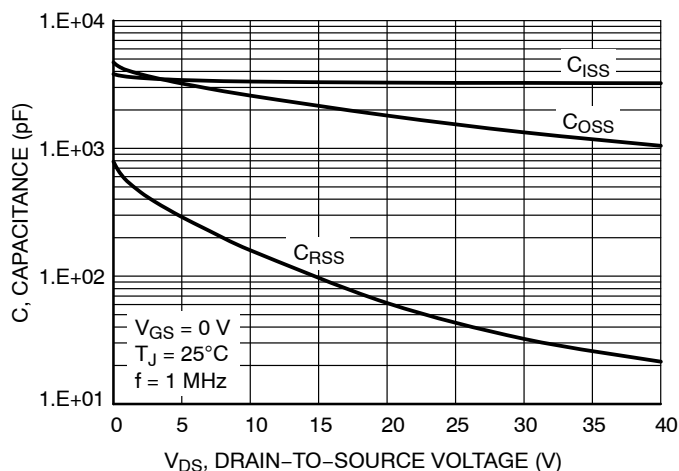


Figure 7. Capacitance Variation

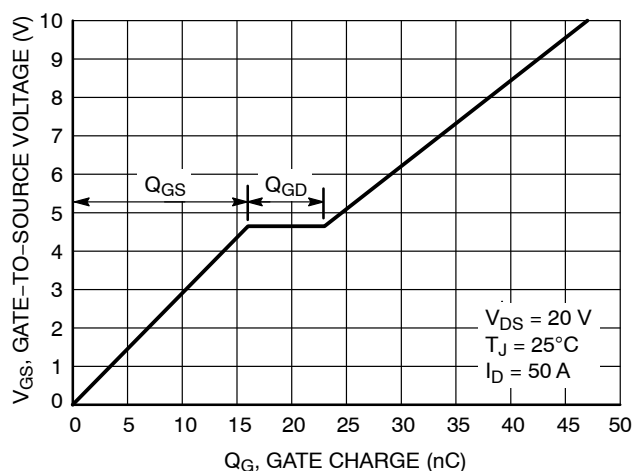


Figure 8. Gate-to-Source Voltage vs. Charge

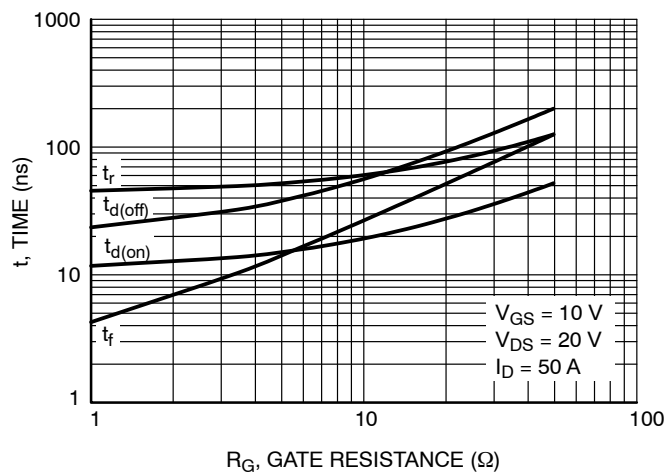


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

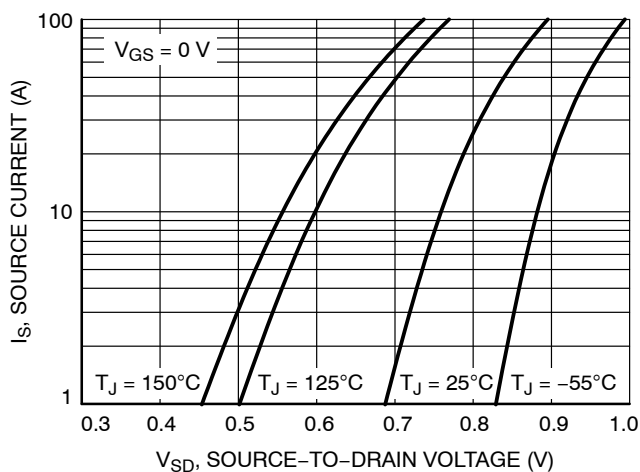


Figure 10. Diode Forward Voltage vs. Current

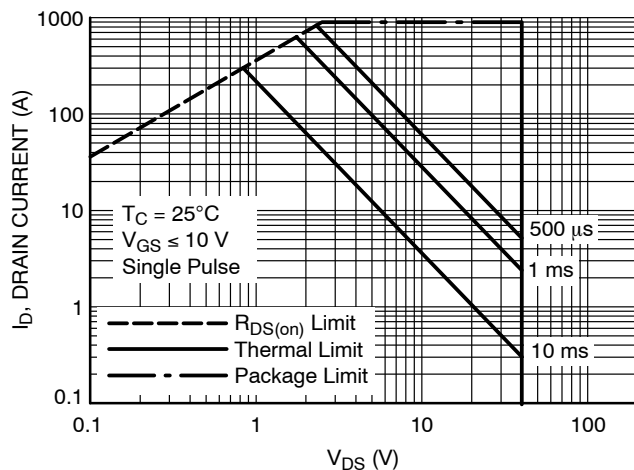


Figure 11. Safe Operating Area

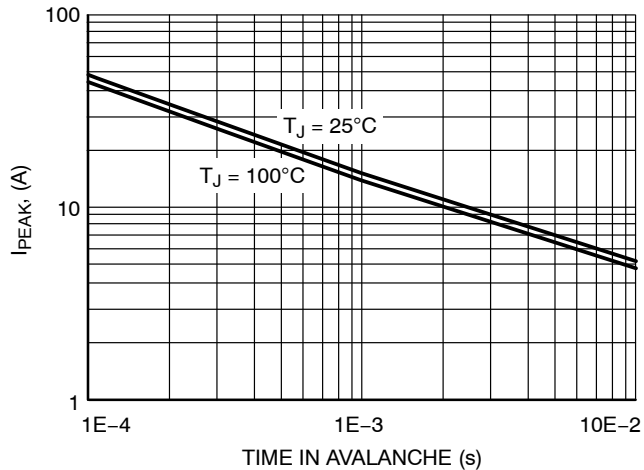


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMJS1D7N04C

TYPICAL CHARACTERISTICS (continued)

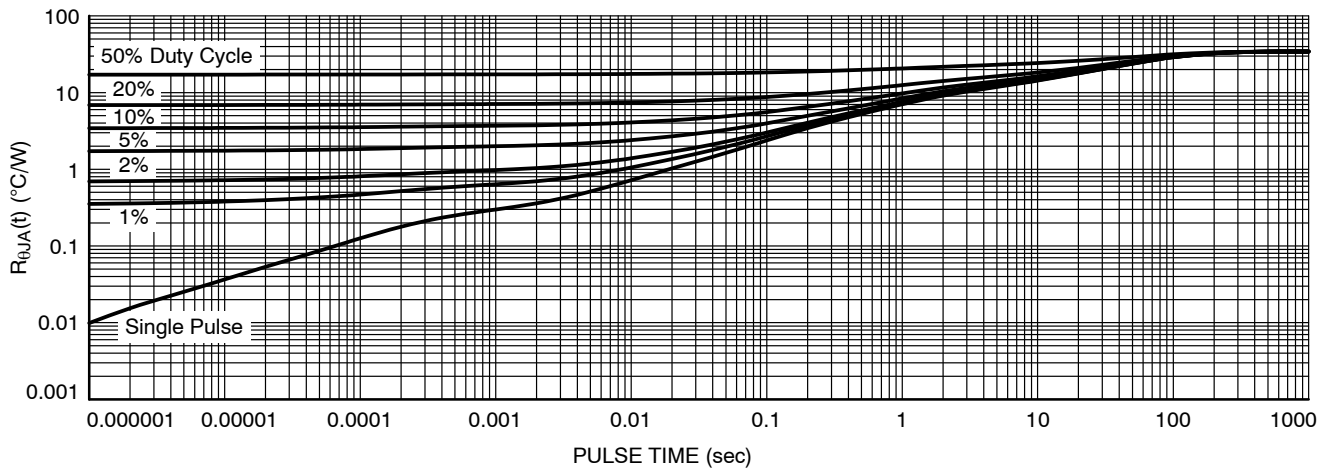


Figure 13. Thermal Characteristics

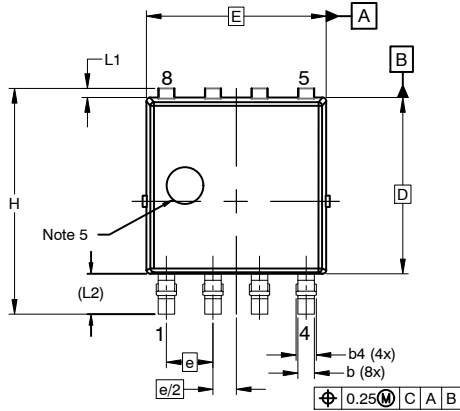
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMJS1D7N04CTWG	1D7N04C	LFPAK8 (Pb-Free)	3,000 / Tape & Reel

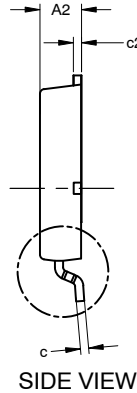
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).


LPAK8 4.90x4.80x1.12MM, 1.27P
CASE 760AA
ISSUE D

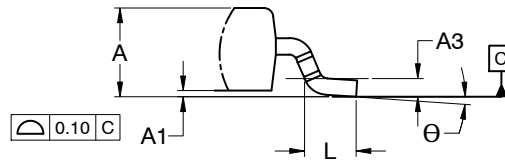
DATE 22 APR 2024



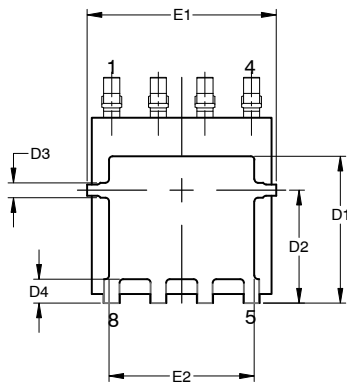
TOP VIEW



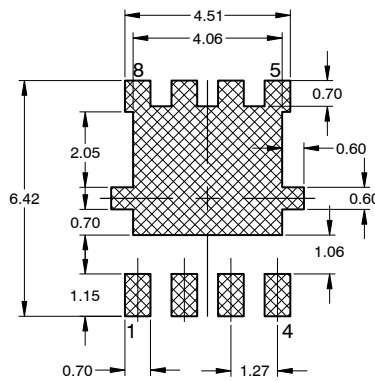
SIDE VIEW



DETAIL 'A'



BOTTOM VIEW



RECOMMENDED LAND PAD

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. OPTIONAL MOLD FEATURE.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 BSC		
b	0.40	0.45	0.50
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.70	4.80	4.90
D1	3.80	4.00	4.20
D2	2.98	3.08	3.18
D3	0.30	0.40	0.50
D4	0.55	0.65	0.75
E	4.80	4.90	5.00
E1	5.05	5.15	5.25
E2	3.91	3.96	4.01
e	1.27 BSC		
e/2	0.635 BSC		
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.15	0.25	0.35
L2	1.10 REF		
Θ	0°	4°	8°

GENERIC
MARKING DIAGRAM*


XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

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