

MOSFET - Power, Single N-Channel, STD Gate, TCPAK57

80 V, 3.3 mΩ, 194 A

Product Preview NVMJST3D3N08X

Features

- Low Q_{RR} , Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AECQ101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- Automotive 48 V System

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

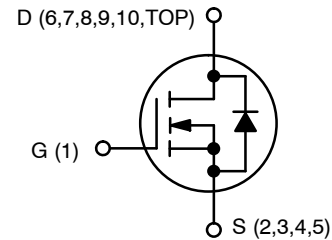
Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}\text{C}$	I_D	194	A
	$T_C = 100^{\circ}\text{C}$		137	
Power Dissipation	$T_C = 25^{\circ}\text{C}$	P_D	258	W
Pulsed Drain Current	$T_C = 25^{\circ}\text{C},$ $t_p = 100\text{ }\mu\text{s}$	I_{DM}	465	A
Pulsed Source Current (Body Diode)		I_{SM}	465	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)		I_S	387	A
Single Pulse Avalanche Energy ($I_{PK} = 47\text{ A}$)		E_{AS}	110	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

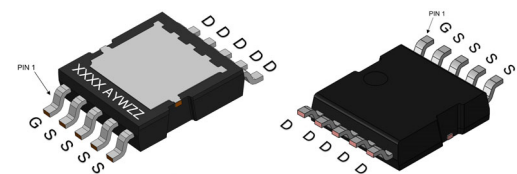
1. Surface-mounted on FR4 board using a 1 in², 1 oz. Cu pad
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. E_{AS} of 140 mJ is based on started $T_J = 25^\circ\text{C}$, $I_{AS} = 53 \text{ A}$, $V_{DD} = 64 \text{ V}$, $V_{GS} = 10 \text{ V}$, 100% avalanche tested.

This document contains information on a product under development. onsemi reserves the right to change or discontinue this product without notice.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	3.3 mΩ @ 10 V	194 A

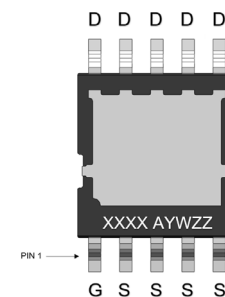


N-CHANNEL MOSFET



TCPAK57
CASE 760AG

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMJST3D3N08X

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.58	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	TBD	

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^{\circ}\text{C}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25°C		33.2		$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, T_J = 25^{\circ}\text{C}$			1	μA
		$V_{DS} = 80\text{ V}, T_J = 125^{\circ}\text{C}$			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 31\text{ A}, T_J = 25^{\circ}\text{C}$		2.79	3.3	$\text{m}\Omega$
		$V_{GS} = 6\text{ V}, I_D = 31\text{ A}, T_J = 25^{\circ}\text{C}$		4.21		
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 153\text{ }\mu\text{A}, T_J = 25^{\circ}\text{C}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 153\text{ }\mu\text{A}$		-7.48		$\text{mV}/^{\circ}\text{C}$
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 31\text{ A}$		96.9		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2747		pF
Output Capacitance	C_{OSS}			798		
Reverse Transfer Capacitance	C_{RSS}			12		
Output Charge	Q_{OSS}	$V_{DD} = 40\text{ V}, I_D = 31\text{ A}, V_{GS} = 10\text{ V}$		57.2		nC
Total Gate Charge	$Q_{G(TOT)}$			38.6		
Threshold Gate Charge	$Q_{G(TH)}$			8.44		
Gate-to-Source Charge	Q_{GS}			12.9		
Gate-to-Drain Charge	Q_{GD}			6.08		
Gate Resistance	R_G	$f = 1\text{ MHz}$		0.6		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load $V_{GS} = 0/10\text{ V}, V_{DD} = 64\text{ V}, I_D = 31\text{ A}, R_G = 2.5\text{ }\Omega$		22.2		ns
Rise Time	t_r			8.85		
Turn-Off Delay Time	$t_{d(OFF)}$			33.9		
Fall Time	t_f			5.33		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 31\text{ A}, T_J = 25^{\circ}\text{C}$		0.83	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 31\text{ A}, T_J = 125^{\circ}\text{C}$		0.67		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = 31\text{ A}, dI/dt = 1000\text{ A}/\mu\text{s}, V_{DD} = 64\text{ V}$		22.6		ns
Charge Time	t_a			12.7		
Discharge Time	t_b			9.94		
Reverse Recovery Charge	Q_{RR}			151		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

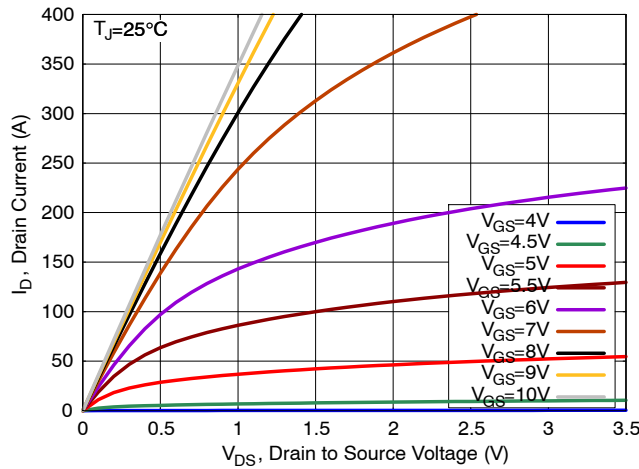


Figure 1. On-Region Characteristics

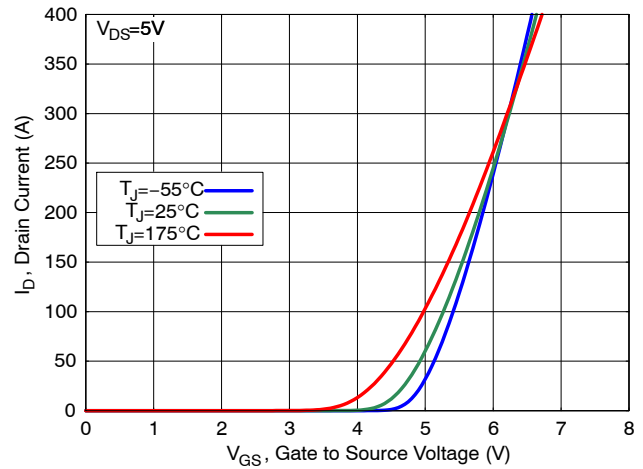


Figure 2. Transfer Characteristics

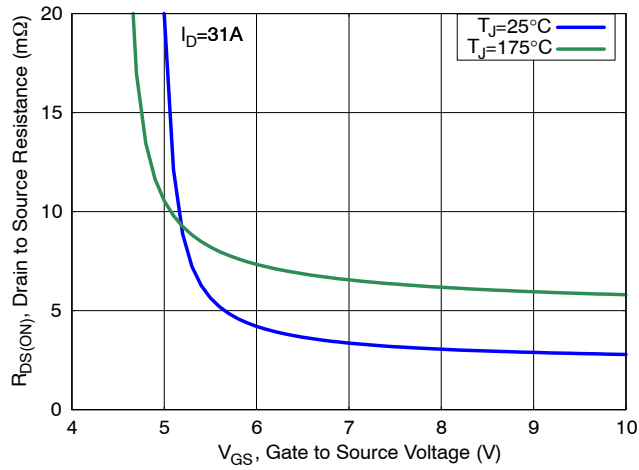


Figure 3. On-Resistance vs. Gate Voltage

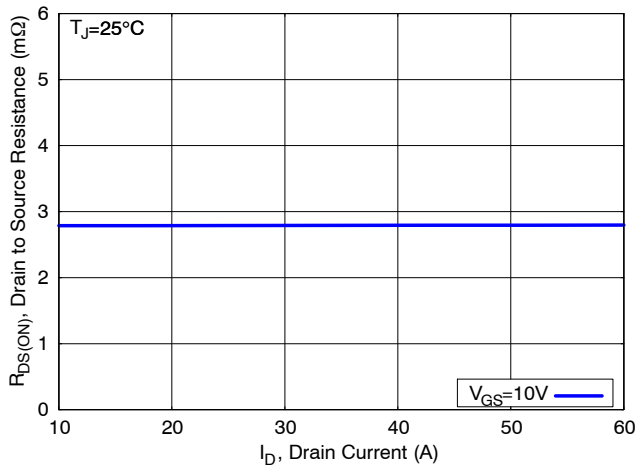


Figure 4. On-Resistance vs. Drain Current

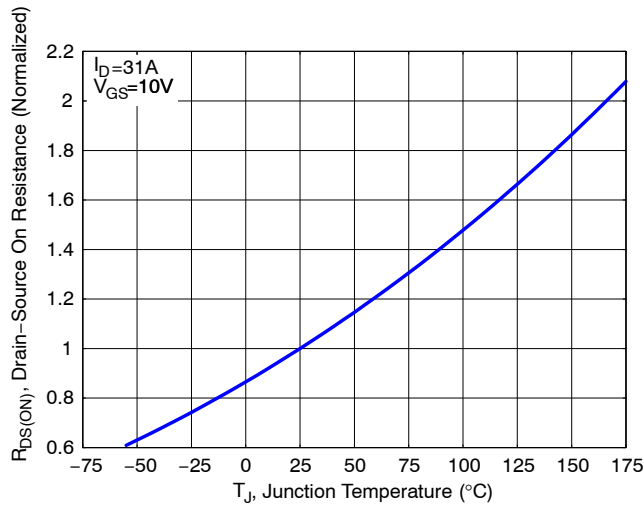


Figure 5. Normalized ON Resistance vs. Junction Temperature

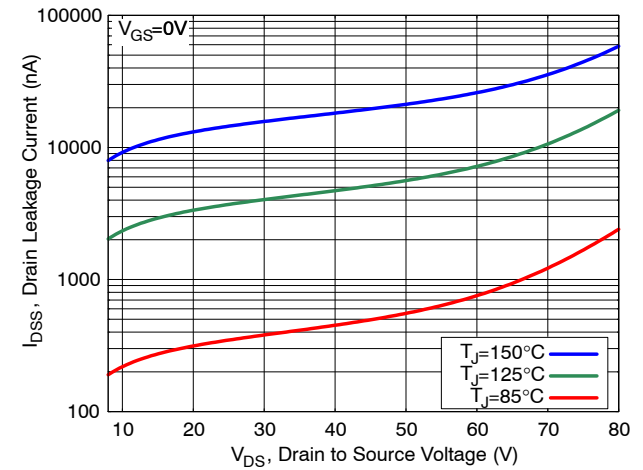


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

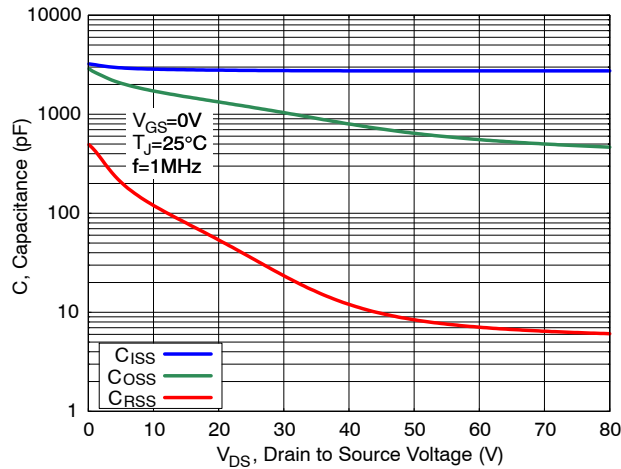


Figure 7. Capacitance Characteristics

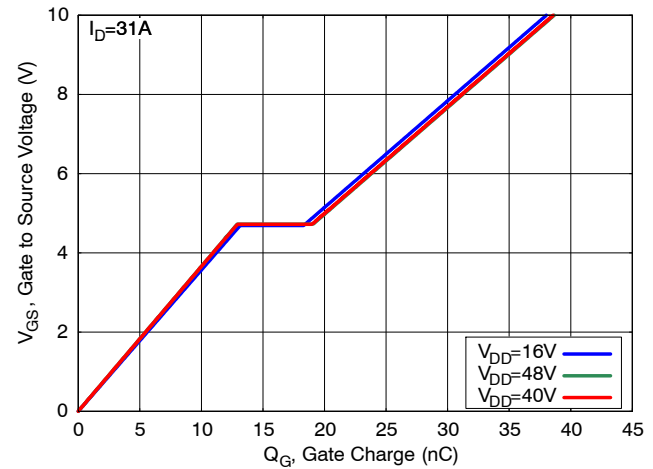


Figure 8. Gate Charge Characteristics

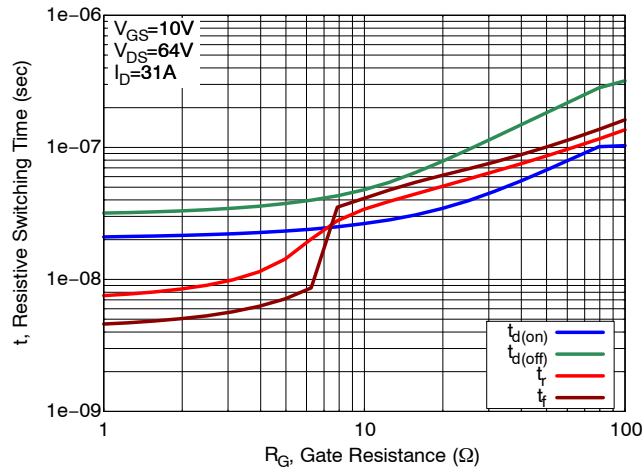


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

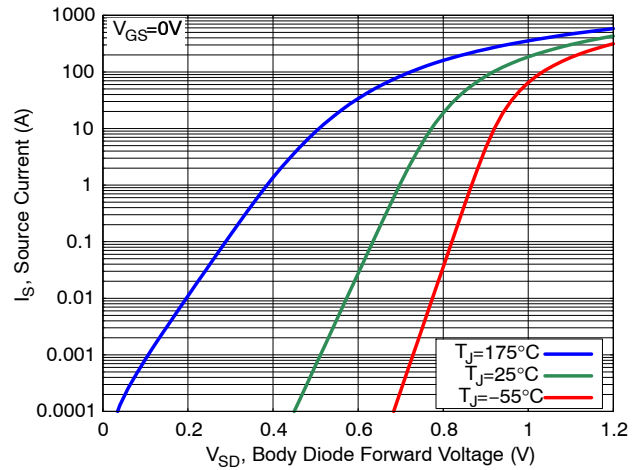


Figure 10. Diode Forward Characteristics

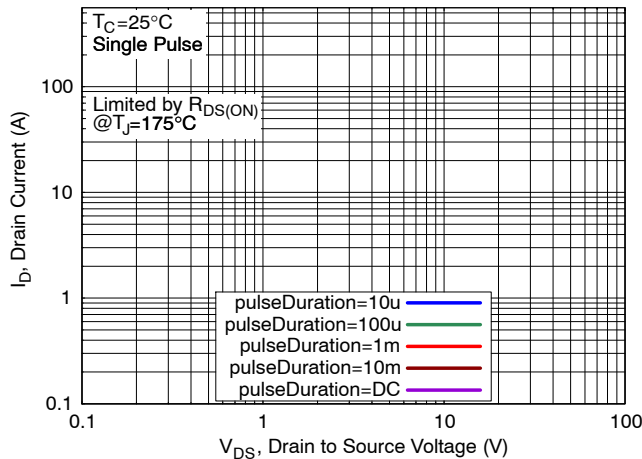


Figure 11. Safe Operating Area (SOA)

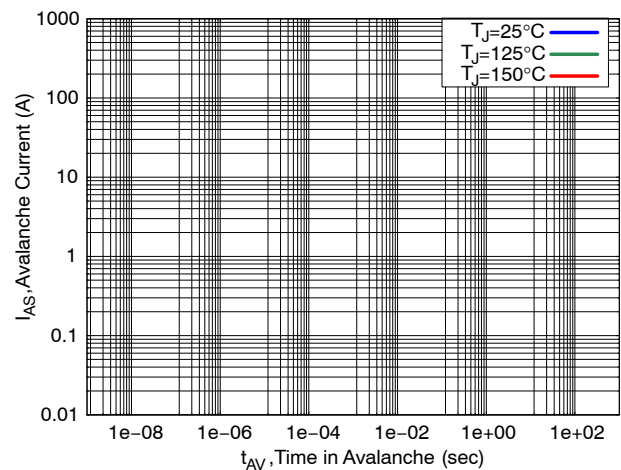


Figure 12. Avalanche Current vs. Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

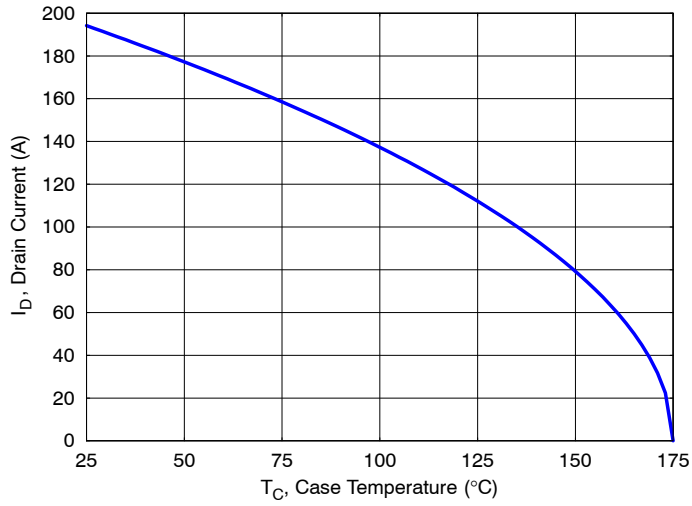


Figure 13. Maximum Current vs. Case Temperature

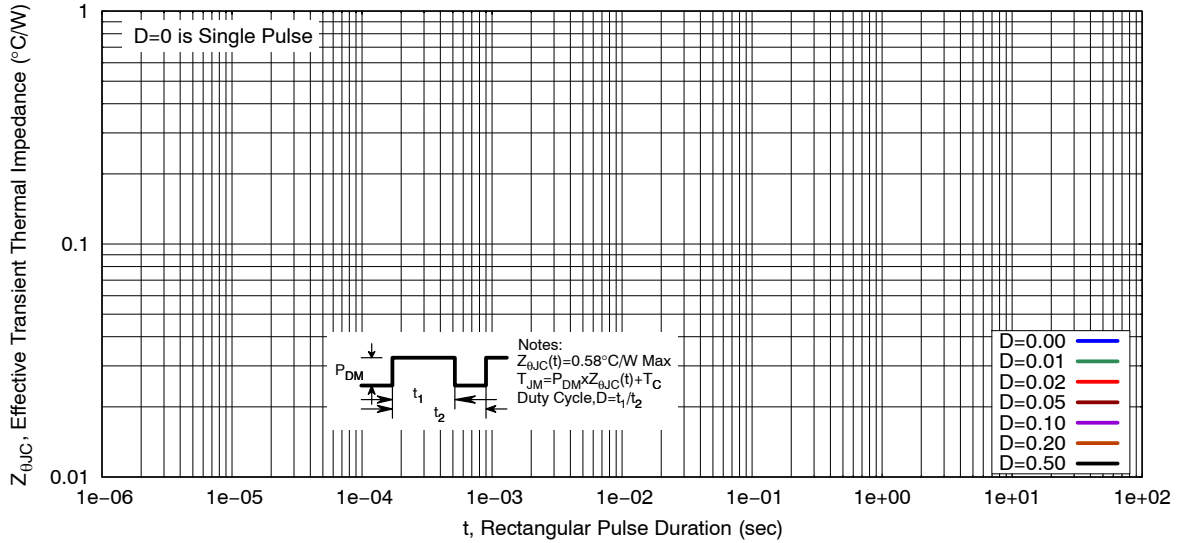


Figure 14. Transient Thermal Response

DEVICE ORDERING INFORMATION

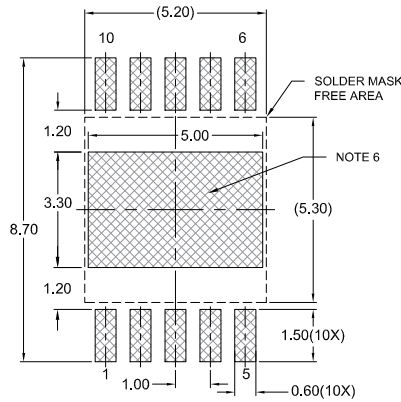
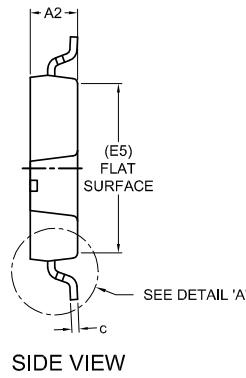
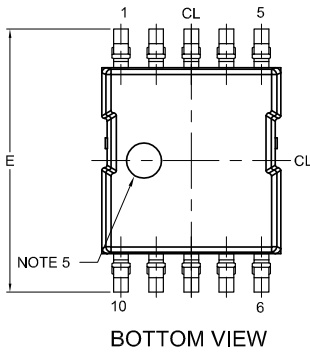
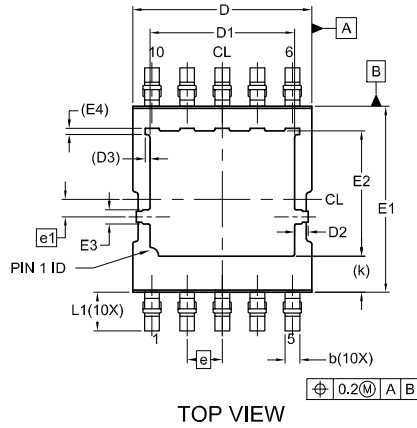
Device	Marking	Package	Shipping [†]
NVMJST3D3N08XTXG	TBD	TCPAK57 Top Cool (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

TCPAK10 5.1x7.5, 1.0P CASE 760AG ISSUE D



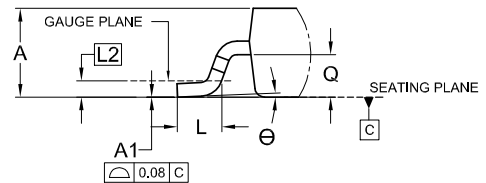
LAND PAD RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. UNIT DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. OPTIONAL MOLD FEATURE.
6. LAND PAD UNDER THE PACKAGE BODY IS FOR MECHANICAL SUPPORT ONLY. SOLDER CONNECTION IS NOT REQUIRED.
7. DIMENSION A1 IS THE LEAD STAND-OFF FROM THE BOTTOM SURFACE OF THE PACKAGE BODY.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.30	1.35	1.45
A1	-0.05	0.00	0.05
A2	1.30	1.35	1.40
b	0.36	0.41	0.46
c	0.16	0.21	0.26
D	5.00	5.10	5.20
D1	4.02	4.12	4.22
D2	0.30	0.40	0.50
D3	0.14 REF		
E	7.40	7.50	7.60
E1	5.20	5.30	5.40
E2	3.47	3.57	3.67
E3	0.30	0.40	0.50
E4	0.17 REF		
E5	4.82 REF		
e	1.00 BSC		
e1	0.50 BSC		
k	1.03 REF		
L	0.49	0.69	0.89
L1	0.90	1.10	1.30
L2	0.25 BSC		
Q	0.60	0.65	0.70
Θ	0°	2.5°	5°



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