

MOSFET - Power, Single N-Channel, STD Gate, PQFN88-3L

80 V, 1.1 mΩ, 299 A

Product Preview
NVMTS1D1N08X

Features

- Low Q_{RR} , Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AECQ101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- Automotive 48 V System

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

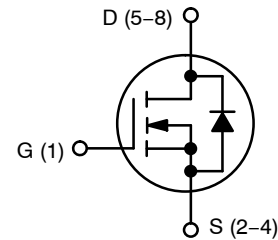
Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	80	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	W
Pulsed Drain Current	I_{DM}	$T_C = 25^\circ\text{C}$, $t_p = 100 \mu\text{s}$	A
Pulsed Source Current (Body Diode)			
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to $+175$	$^\circ\text{C}$
Source Current (Body Diode)	I_S	287	A
Single Pulse Avalanche Energy ($I_{PK} = 60 \text{ A}$)	E_{AS}	180	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

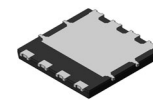
1. Surface-mounted on FR4 board using a 1 in², 1 oz. Cu pad
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. E_{AS} is based on started $T_J = 25^\circ\text{C}$, rated I_{AS} , $V_{DD} = 64 \text{ V}$, $V_{GS} = 10 \text{ V}$, 100% avalanche tested.

This document contains information on a product under development. onsemi reserves the right to change or discontinue this product without notice.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	1.1 mΩ @ 10 V	299 A

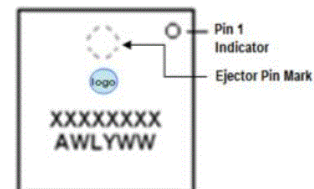


N-CHANNEL MOSFET



TDFNW8
 SINGLE COOL
 CASE 507AP

MARKING DIAGRAM



XXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot Code
 Y = Year Code
 WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.76	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	TBD	

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^{\circ}\text{C}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25°C		30.9		$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, T_J = 25^{\circ}\text{C}$			1	μA
		$V_{DS} = 80\text{ V}, T_J = 125^{\circ}\text{C}$			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 100\text{ A}, T_J = 25^{\circ}\text{C}$		1.01	1.1	$\text{m}\Omega$
		$V_{GS} = 6\text{ V}, I_D = 100\text{ A}, T_J = 25^{\circ}\text{C}$		1.47		
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 490\text{ }\mu\text{A}, T_J = 25^{\circ}\text{C}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 490\text{ }\mu\text{A}$		-7.47		$\text{mV}/^{\circ}\text{C}$
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 100\text{ A}$		296		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		8625		pF
Output Capacitance	C_{OSS}			2460		
Reverse Transfer Capacitance	C_{RSS}			36.7		
Output Charge	Q_{OSS}	$V_{DD} = 40\text{ V}, I_D = 100\text{ A}, V_{GS} = 10\text{ V}$		176		nC
Total Gate Charge	$Q_{G(TOT)}$			120		
Threshold Gate Charge	$Q_{G(TH)}$			26.5		
Gate-to-Source Charge	Q_{GS}			40.7		
Gate-to-Drain Charge	Q_{GD}			18.7		
Gate Resistance	R_G	$f = 1\text{ MHz}$		0.71		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 64\text{ V}, I_D = 100\text{ A}, R_G = 2.5\text{ }\Omega$		39.4		ns
Rise Time	t_r			97.7		
Turn-Off Delay Time	$t_{d(OFF)}$			65.2		
Fall Time	t_f			12.3		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 100\text{ A}, T_J = 25^{\circ}\text{C}$		0.84	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 100\text{ A}, T_J = 125^{\circ}\text{C}$		0.69		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = 100\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}, V_{DD} = 64\text{ V}, T_J = 25^{\circ}\text{C}$		33.7		ns
Charge Time	t_a			18		
Discharge Time	t_b			15.8		
Reverse Recovery Charge	Q_{RR}			316		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

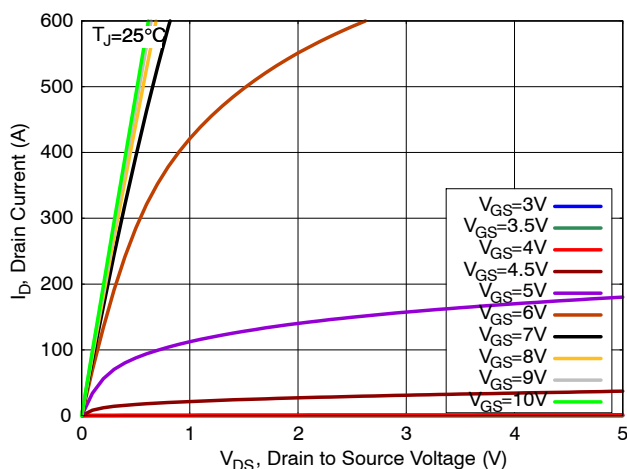


Figure 1. On-Region Characteristics

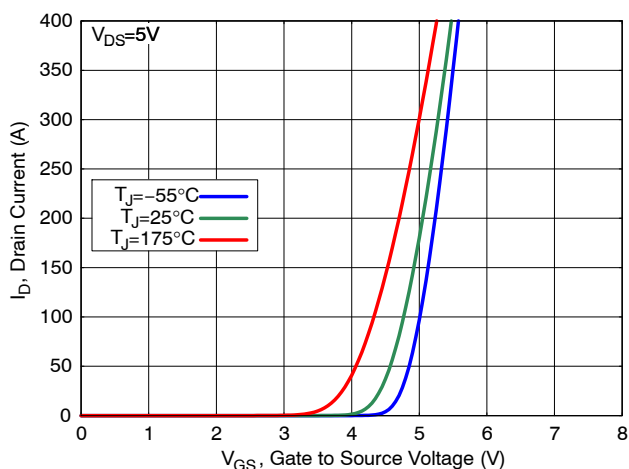


Figure 2. Transfer Characteristics

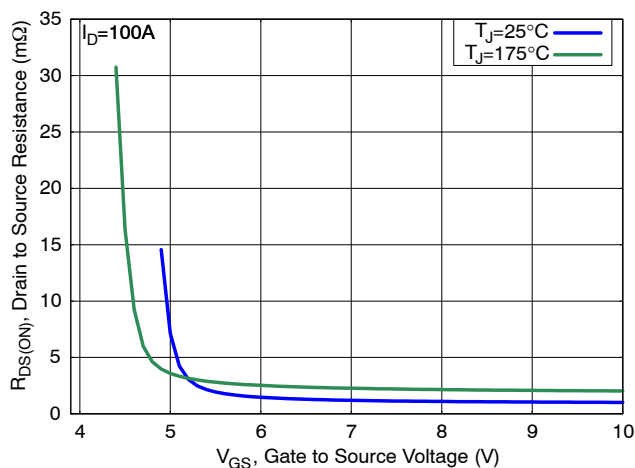


Figure 3. On-Resistance vs. Gate Voltage

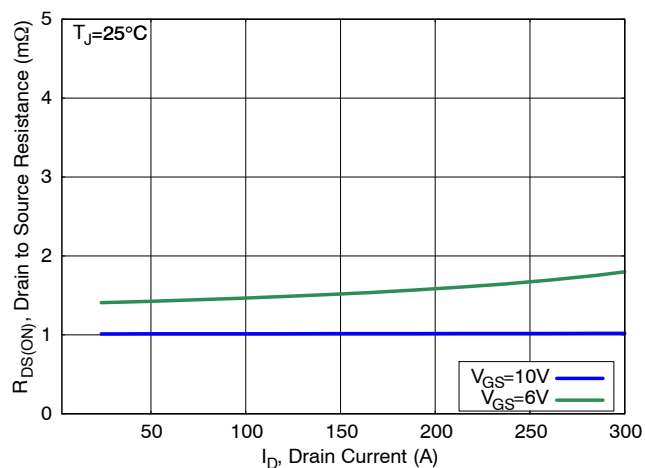


Figure 4. On-Resistance vs. Drain Current

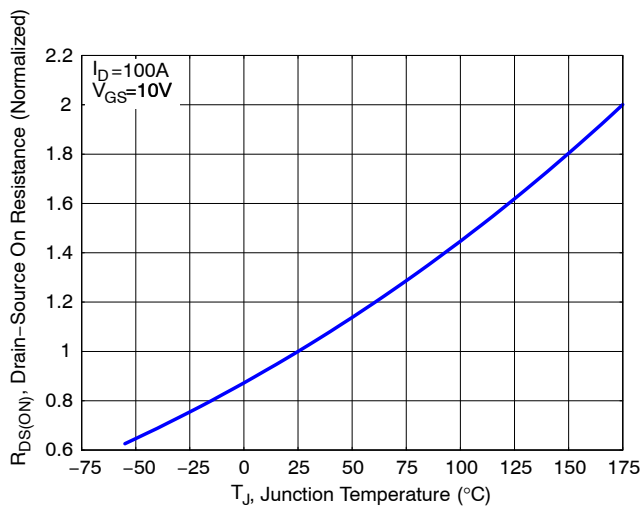


Figure 5. Normalized ON Resistance vs. Junction Temperature

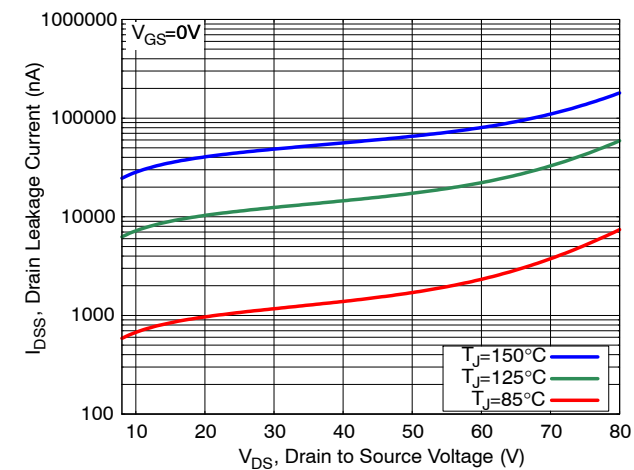


Figure 6. Drain Leakage Current vs. Drain Voltage

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TYPICAL CHARACTERISTICS

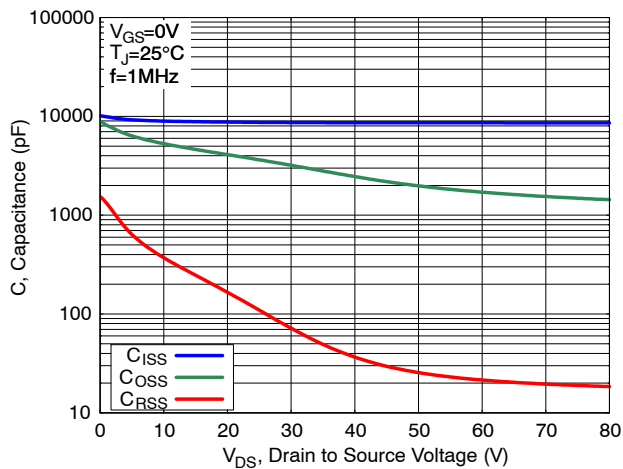


Figure 7. Capacitance Characteristics

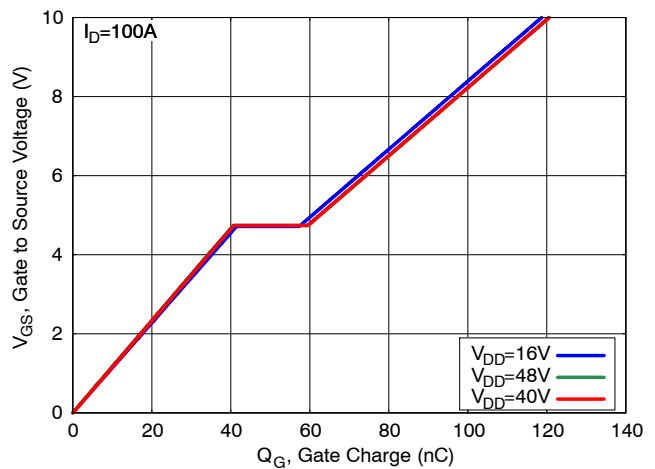


Figure 8. Gate Charge Characteristics

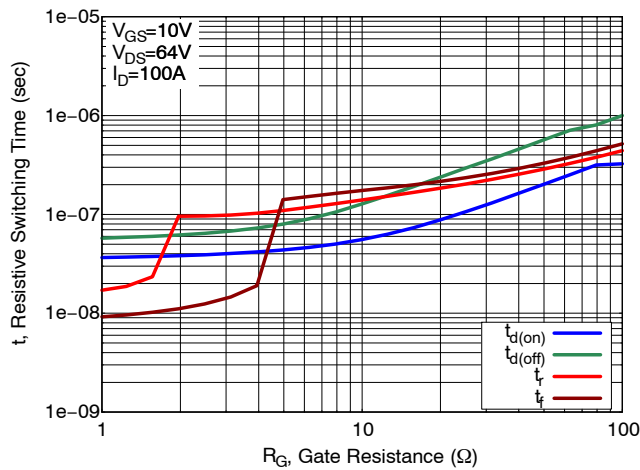


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

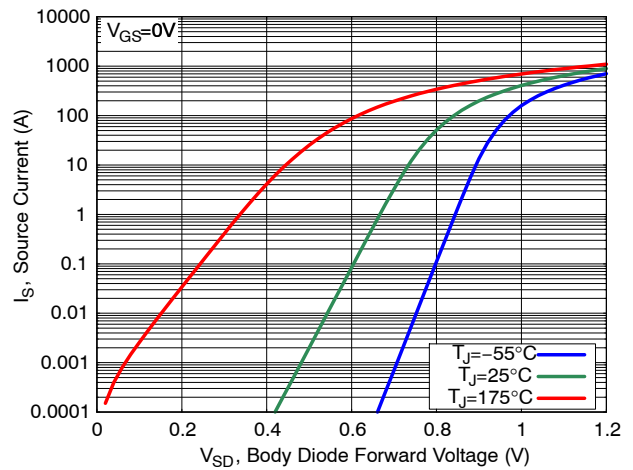


Figure 10. Diode Forward Characteristics

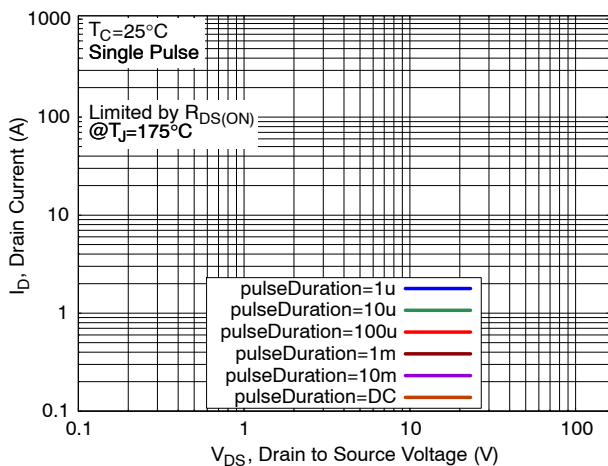


Figure 11. Safe Operating Area (SOA)

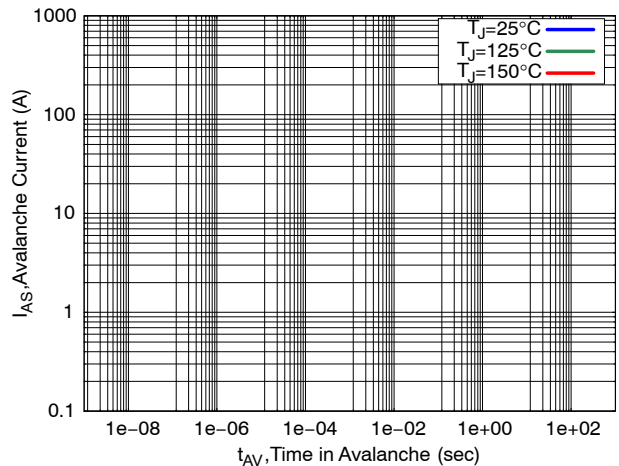


Figure 12. Avalanche Current vs. Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

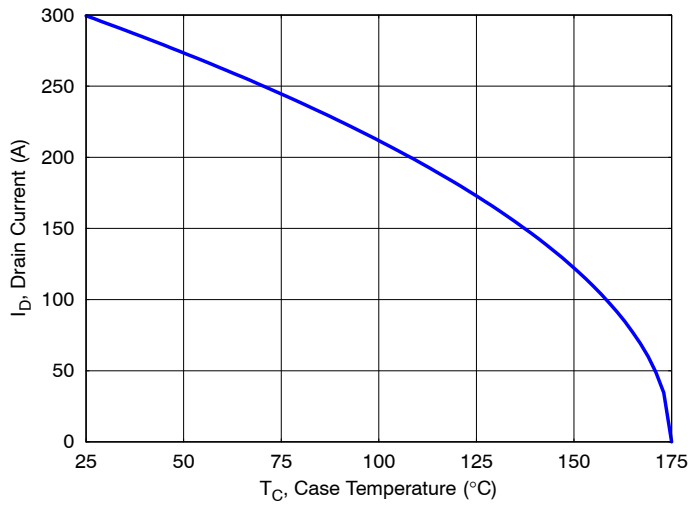


Figure 13. Maximum Current vs. Case Temperature

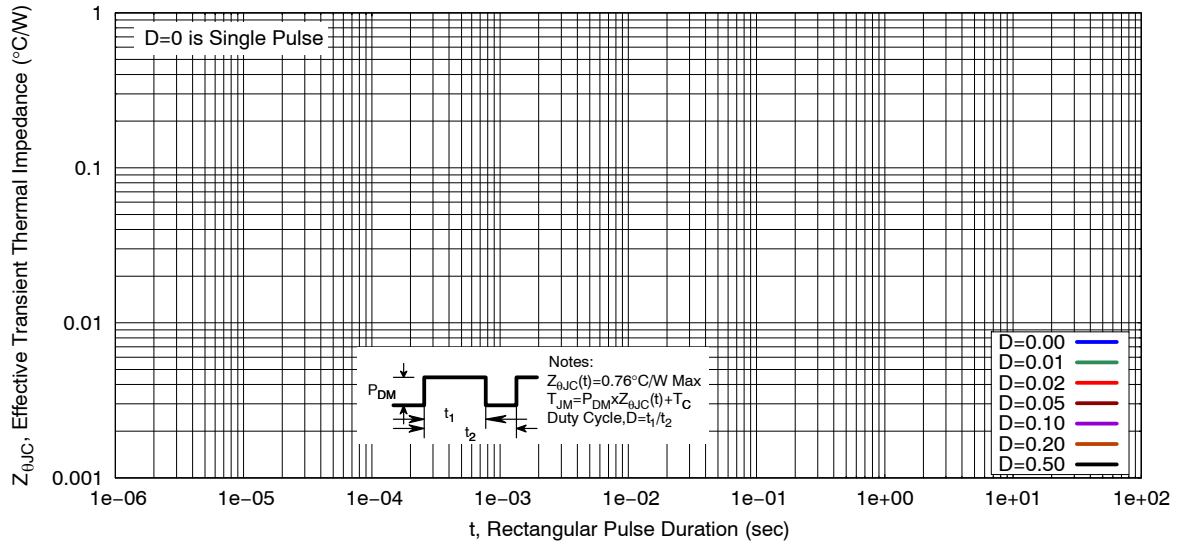


Figure 14. Transient Thermal Response

DEVICE ORDERING INFORMATION

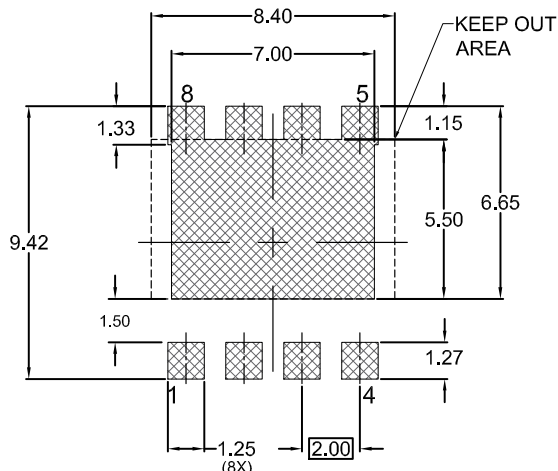
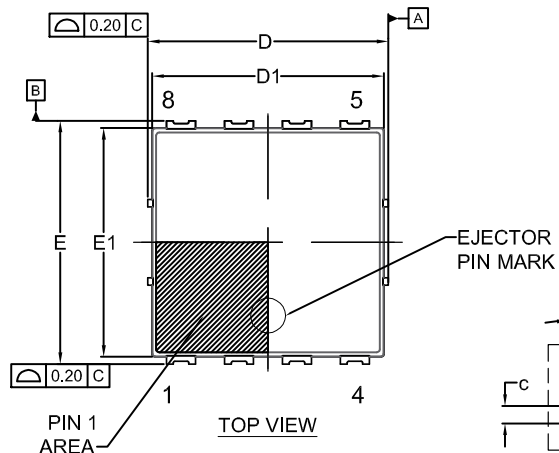
Device	Marking	Package	Shipping [†]
NVMTS1D1N08XTXG	TBD	TDFNW8	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

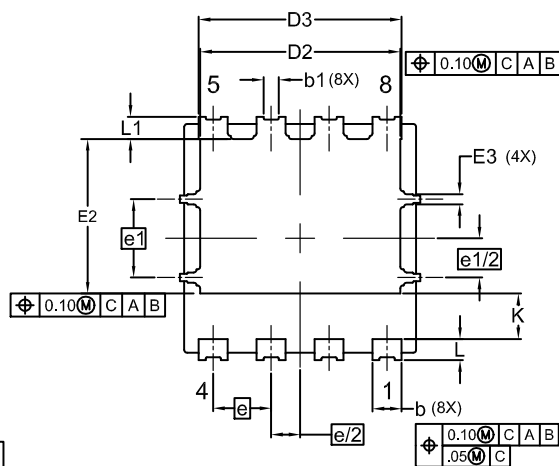
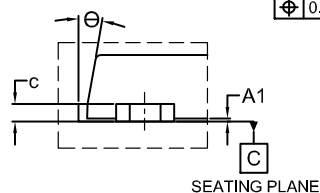
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PACKAGE DIMENSIONS

TDFNW8 8.3x8.4, 2.0P, SINGLE COOL
CASE 507AP
ISSUE D



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	—	12°

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