

# Silicon Carbide (SiC) Module - EliteSiC, 6 mohm, 1200 V, SiC M3 MOSFET, 2-PACK Half Bridge Topology, F2 Package with HPS DBC

## NXH006P120M3F2PTHG

The NXH006P120M3F2PTHG is a power module containing 6 mΩ / 1200 V SiC MOSFET half-bridge and a thermistor with HPS DBC in an F2 package.

### Features

- 6 mΩ / 1200 V M3S SiC MOSFET Half-Bridge
- HPS DBC
- Thermistor
- Pre-Applied Thermal Interface Material (TIM)
- Press-Fit Pins
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

### Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Electric Vehicle Charging Stations
- Industrial Power

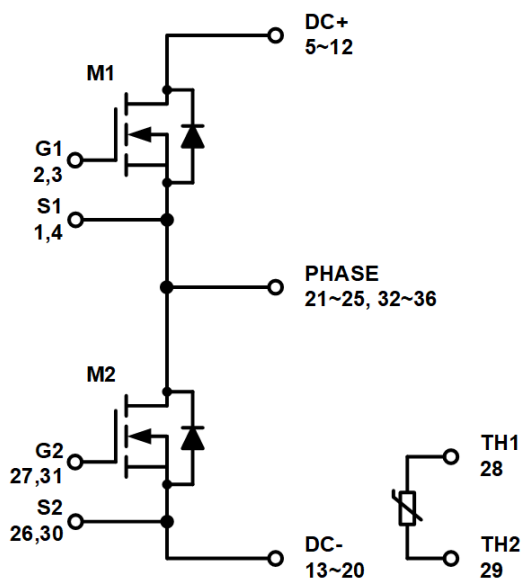
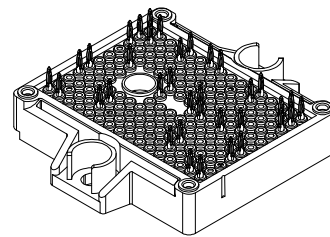


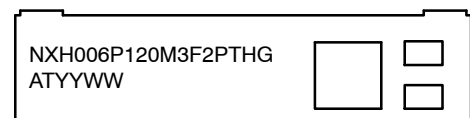
Figure 1. NXH006P120M3F2 Schematic Diagram

### PACKAGE PICTURE



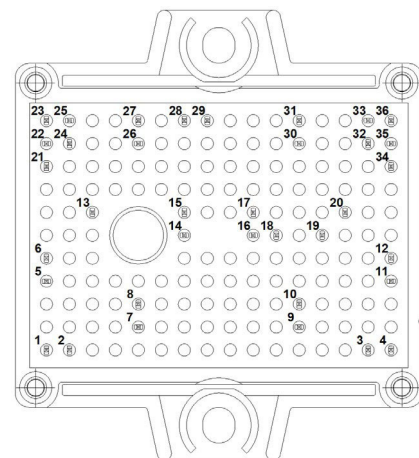
PIM36 56.7x42.5 (PRESS FIT)  
CASE 180BY

### MARKING DIAGRAM



NXH006P120M3F2PTHG = Specific Device Code  
AT = Assembly & Test Site Code  
YYWW = Year and Work Week Code

### PIN CONNECTIONS



See Pin Function Description for pin names

### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

# NXH006P120M3F2PTHG

## PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	S1	Q1 Kelvin Emitter (High side switch)
2	G1	Q1 Gate (High side switch)
3	G1	Q1 Gate (High side switch)
4	S1	Q1 Kelvin Emitter (High side switch)
5	DC+	DC Positive Bus connection
6	DC+	DC Positive Bus connection
7	DC+	DC Positive Bus connection
8	DC+	DC Positive Bus connection
9	DC+	DC Positive Bus connection
10	DC+	DC Positive Bus connection
11	DC+	DC Positive Bus connection
12	DC+	DC Positive Bus connection
13	DC-	DC Negative Bus connection
14	DC-	DC Negative Bus connection
15	DC-	DC Negative Bus connection
16	DC-	DC Negative Bus connection
17	DC-	DC Negative Bus connection
18	DC-	DC Negative Bus connection
19	DC-	DC Negative Bus connection
20	DC-	DC Negative Bus connection
21	PHASE	Center point of half bridge
22	PHASE	Center point of half bridge
23	PHASE	Center point of half bridge
24	PHASE	Center point of half bridge
25	PHASE	Center point of half bridge
26	S2	Q2 Kelvin Emitter (Low side switch)
27	G2	Q2 Gate (Low side switch)
28	TH1	Thermistor Connection 1
29	TH2	Thermistor Connection 2
30	S2	Q2 Kelvin Emitter (Low side switch)
31	G2	Q2 Gate (Low side switch)
32	PHASE	Center point of half bridge
33	PHASE	Center point of half bridge
34	PHASE	Center point of half bridge
35	PHASE	Center point of half bridge
36	PHASE	Center point of half bridge

# NXH006P120M3F2PTHG

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
<b>SIC MOSFET</b>			
Drain-Source Voltage	$V_{DS}$	1200	V
Gate-Source Voltage	$V_{GS}$	+22/-10	V
Continuous Drain Current @ $T_c = 80\text{ }^{\circ}\text{C}$ ( $T_J = 175\text{ }^{\circ}\text{C}$ )	$I_D$	191	A
Pulsed Drain Current ( $T_J = 175\text{ }^{\circ}\text{C}$ )	$I_{Dpulse}$	382	A
Maximum Power Dissipation @ $T_c = 80\text{ }^{\circ}\text{C}$ ( $T_J = 175\text{ }^{\circ}\text{C}$ )	$P_{tot}$	556	W
Minimum Operating Junction Temperature	$T_{JMIN}$	-40	$^{\circ}\text{C}$
Maximum Operating Junction Temperature	$T_{JMAX}$	175	$^{\circ}\text{C}$

## THERMAL PROPERTIES

Storage Temperature Range	$T_{stg}$	-40 to 150	$^{\circ}\text{C}$
TIM Layer Thickness	$T_{TIM}$	160 $\pm$ 20	$\mu\text{m}$

## INSULATION PROPERTIES

Isolation Test Voltage, $t = 1\text{ s}$ , 60 Hz	$V_{is}$	4800	$V_{RMS}$
Creepage Distance		12.7	mm
CTI		600	
Substrate Ceramic Material		HPS	
Substrate Ceramic Material Thickness		0.38	mm
Substrate Warpage (Note 2)	W	Max 0.18	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. Height difference between horizontal plane and substrate copper bottom.

## RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	$T_J$	-40	150	$^{\circ}\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>SIC MOSFET CHARACTERISTICS</b>						
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 1200\text{ V}$	-	-	300	$\mu\text{A}$
Drain-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 18\text{ V}$ , $I_D = 100\text{ A}$ , $T_J = 25\text{ }^{\circ}\text{C}$	-	6.5	8	$\text{m}\Omega$
		$V_{GS} = 18\text{ V}$ , $I_D = 100\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$	-	10.8	-	
		$V_{GS} = 18\text{ V}$ , $I_D = 100\text{ A}$ , $T_J = 150\text{ }^{\circ}\text{C}$	-	12.4	-	
		$V_{GS} = 18\text{ V}$ , $I_D = 100\text{ A}$ , $T_J = 175\text{ }^{\circ}\text{C}$	-	14.6	-	
Gate-Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 80\text{ mA}$	1.8	2.8	4.4	V
Gate Leakage Current	$I_{GSS}$	$V_{GS} = -10\text{ V} / 20\text{ V}$ , $V_{DS} = 0\text{ V}$	-400	-	400	nA
Gate-Resistance	$R_G$	$f = 1\text{ MHz}$	-	0.375	-	$\Omega$
Input Capacitance	$C_{ISS}$	$V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 100\text{ kHz}$	-	11914	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	48	-	
Output Capacitance	$C_{OSS}$		-	669	-	

# NXH006P120M3F2PTHG

## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>SIC MOSFET CHARACTERISTICS</b>						
Total Gate Charge	$Q_{G(TOTAL)}$	$V_{DS} = 800\text{ V}$ , $V_{GS} = -5/20\text{ V}$ , $I_D = 100\text{ A}$	–	622	–	nC
Gate-Source Charge	$Q_{GS}$		–	109	–	nC
Gate-Drain Charge	$Q_{GD}$		–	120	–	nC
Turn-on Delay Time	$t_{d(on)}$	$T_J = 25\text{ }^{\circ}\text{C}$ $V_{DS} = 600\text{ V}$ , $I_D = 100\text{ A}$ $V_{GS} = -5\text{ V} / 18\text{ V}$ , $R_G = 1\text{ }\Omega$	–	40.53	–	ns
Rise Time	$t_r$		–	13.61	–	
Turn-off Delay Time	$t_{d(off)}$		–	109	–	
Fall Time	$t_f$		–	8.54	–	
Turn-on Switching Loss per Pulse	$E_{ON}$		–	0.89	–	mJ
Turn-off Switching Loss per Pulse	$E_{OFF}$		–	0.44	–	
Turn-on Delay Time	$t_{d(on)}$	$T_J = 150\text{ }^{\circ}\text{C}$ $V_{DS} = 600\text{ V}$ , $I_D = 100\text{ A}$ $V_{GS} = -5\text{ V} / 18\text{ V}$ , $R_G = 1\text{ }\Omega$	–	38.21	–	ns
Rise Time	$t_r$		–	12.92	–	
Turn-off Delay Time	$t_{d(off)}$		–	118	–	
Fall Time	$t_f$		–	8.73	–	
Turn-on Switching Loss per Pulse	$E_{ON}$		–	1.12	–	mJ
Turn-off Switching Loss per Pulse	$E_{OFF}$		–	0.44	–	
Diode Forward Voltage	$V_{SD}$	$I_D = 100\text{ A}$ , $T_J = 25\text{ }^{\circ}\text{C}$	–	5.31	7.5	V
		$I_D = 100\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$	–	4.91	–	
		$I_D = 100\text{ A}$ , $T_J = 150\text{ }^{\circ}\text{C}$	–	4.82	–	
Thermal Resistance – Chip-to-Case	$R_{thJC}$	M1, M2	–	0.171	–	$^{\circ}\text{C/W}$
Thermal Resistance – Chip-to-Heatsink	$R_{thJH}$	Thermal grease, Thickness = 2 Mil +2%, A = 2.8 W/mK	–	0.288	–	$^{\circ}\text{C/W}$

## THERMISTOR CHARACTERISTICS

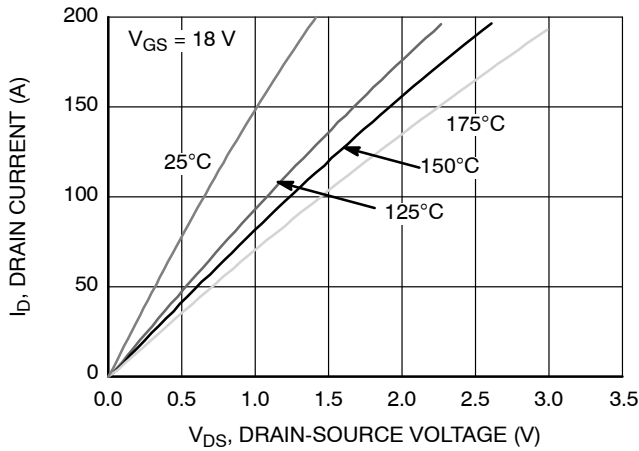
Nominal Resistance	$R_{25}$	$T_{NTC} = 25\text{ }^{\circ}\text{C}$	–	5	–	k $\Omega$
Nominal Resistance	$R_{100}$	$T_{NTC} = 100\text{ }^{\circ}\text{C}$	–	493	–	$\Omega$
Nominal Resistance	$R_{150}$	$T_{NTC} = 150\text{ }^{\circ}\text{C}$	–	159.5	–	$\Omega$
Deviation of $R_{100}$	$\Delta R/R$	$T_{NTC} = 100\text{ }^{\circ}\text{C}$	–5	–	5	%
Power Dissipation – Recommended Limit	$P_D$	0.15 mA, non-self-heating effect	–	0.1	–	mW
Power Dissipation – Absolute Maximum	$P_D$	5 mA	–	34.2	–	mW
Power Dissipation Constant			–	1.4	–	mW/K
B-value		B(25/50), tolerance $\pm 2\%$	–	3375	–	K
B-value		B(25/100), tolerance $\pm 2\%$	–	3436	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

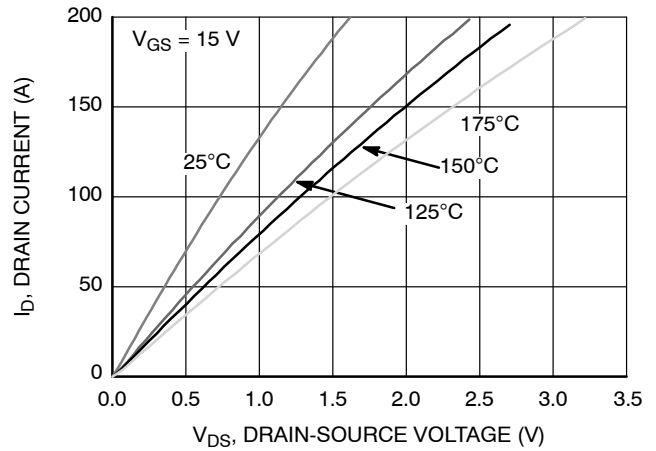
## ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH006P120M3F2PTHG	NXH006P120M3F2PTHG	F2HALFBR: Case 180BY Press-fit Pins with pre-applied thermal interface material (TIM) (Pb-Free / Halide Free)	20 Units / Blister Tray

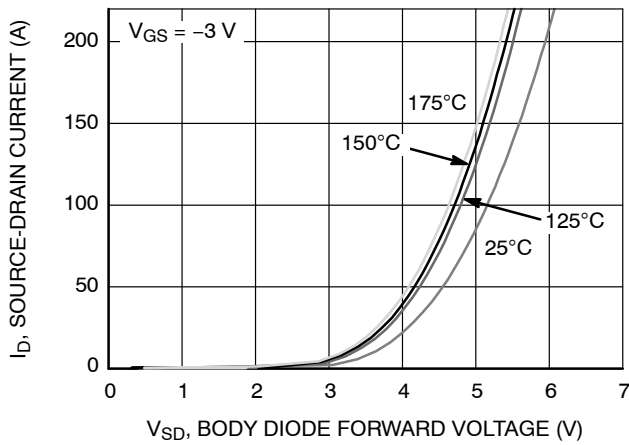
**TYPICAL CHARACTERISTIC**  
(M1/M2 SiC MOSFET CHARACTERISTIC)



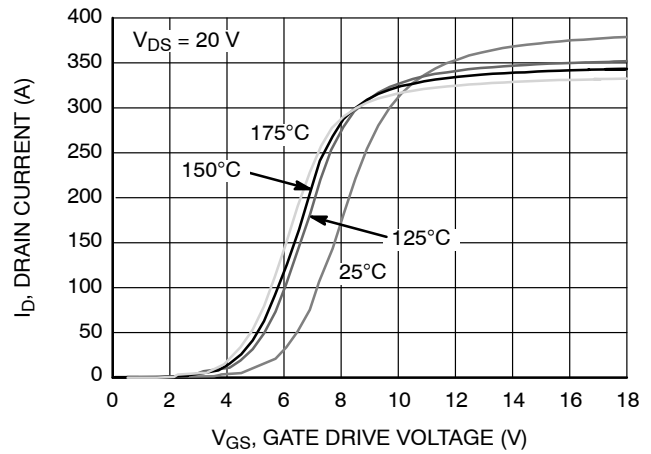
**Figure 2. MOSFET Typical Output Characteristic**



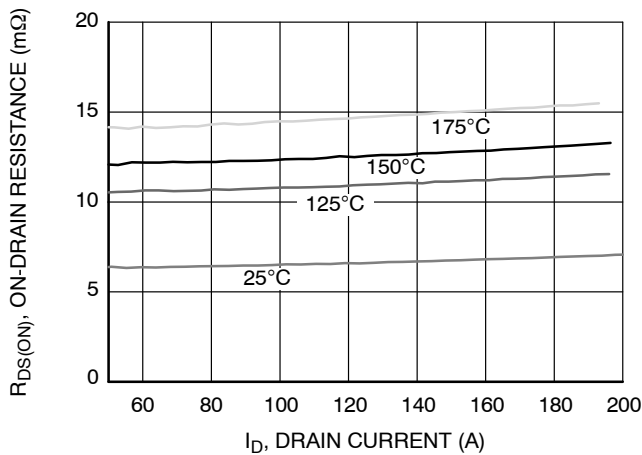
**Figure 3. MOSFET Typical Output Characteristic**



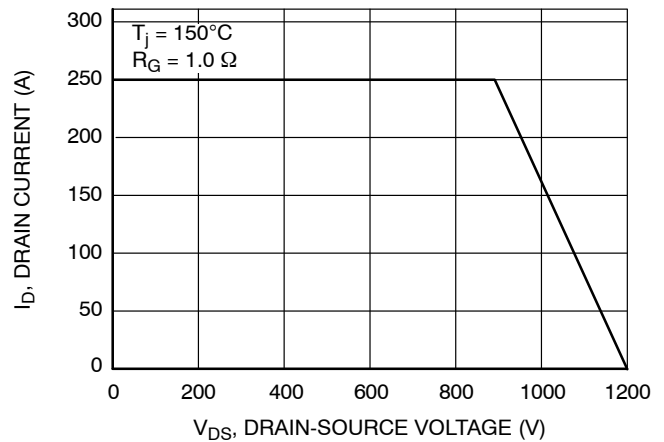
**Figure 4. MOSFET Typical Transfer Characteristic**



**Figure 5. Body Diode Forward Characteristic**

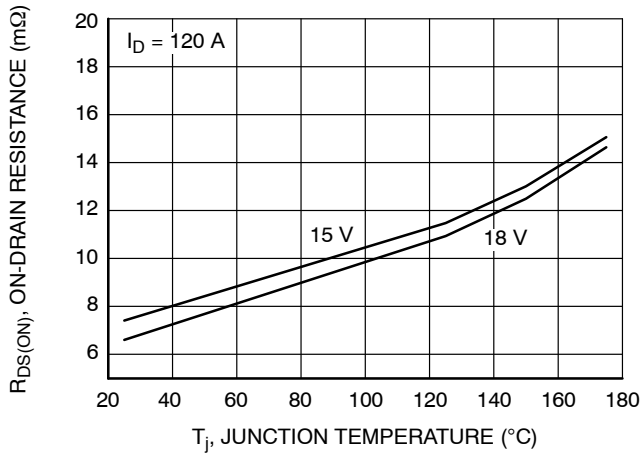


**Figure 6. MOSFET  $R_{DS(ON)}$  vs.  $I_D$**

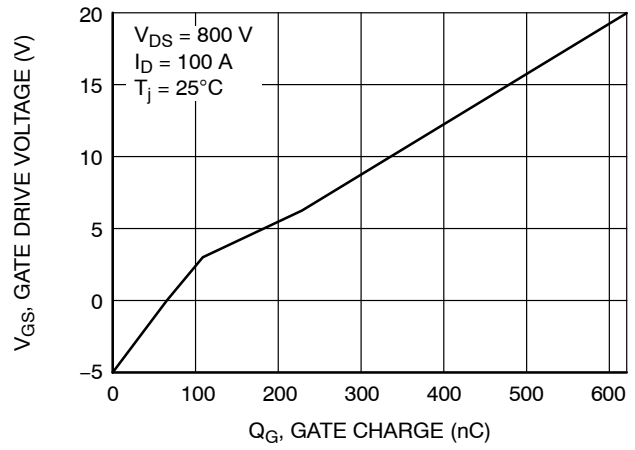


**Figure 7. MOSFET RBSOA**

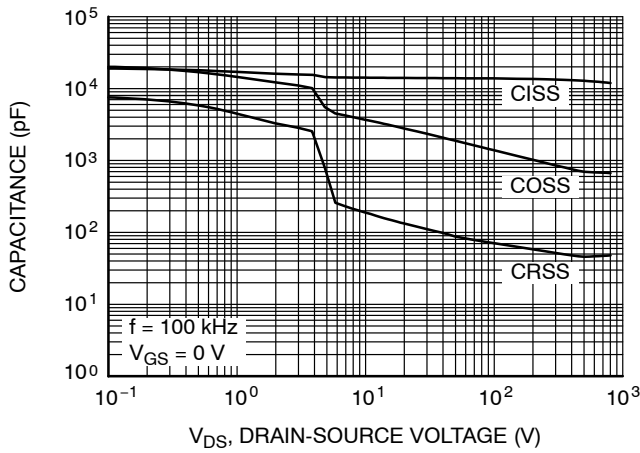
**TYPICAL CHARACTERISTIC**  
(M1/M2 SiC MOSFET CHARACTERISTIC)



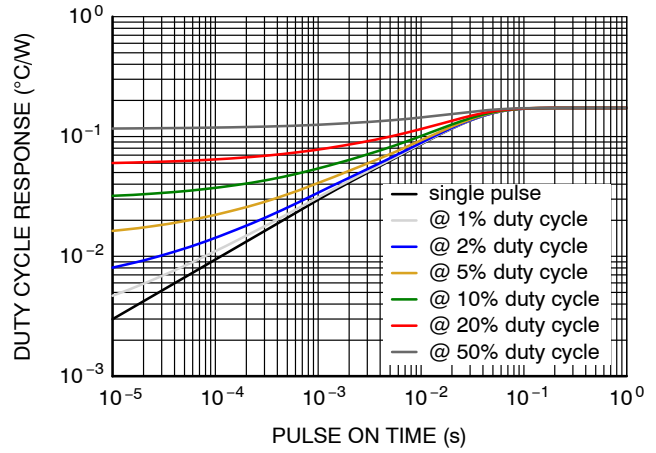
**Figure 8. MOSFET  $R_{DS(ON)}$  vs.  $T_j$**



**Figure 9. Gate-to-Source Voltage vs. Total Charge**

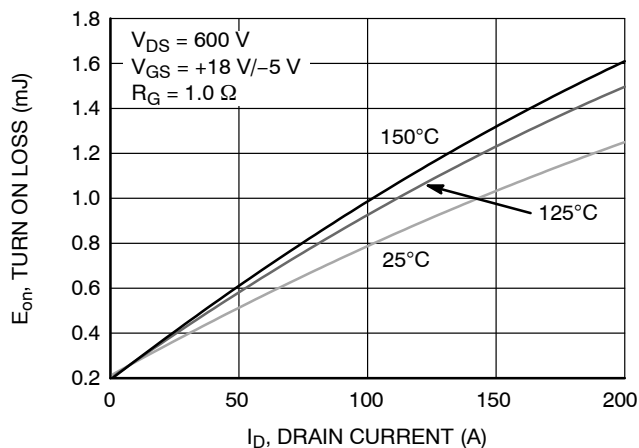


**Figure 10. Capacitance vs. Drain-to-Source Voltage**

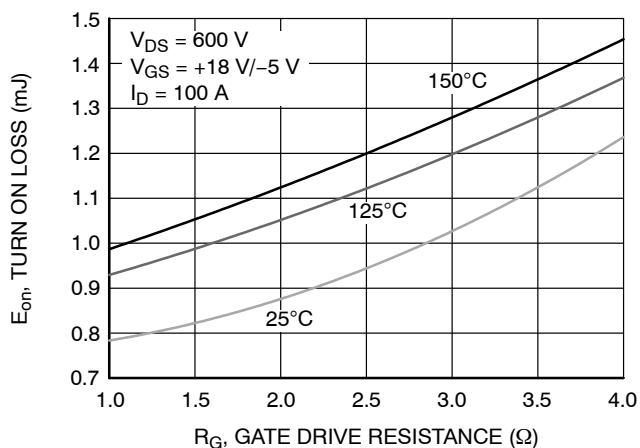


**Figure 11. MOSFET Junction-to-Case Transient Thermal Impedance**

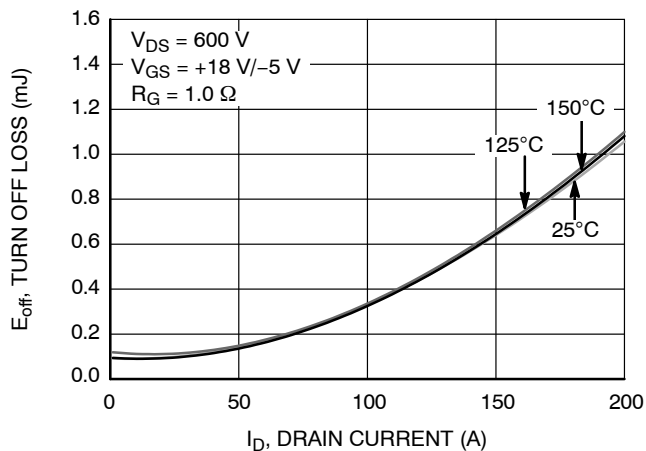
**TYPICAL CHARACTERISTIC**  
(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)



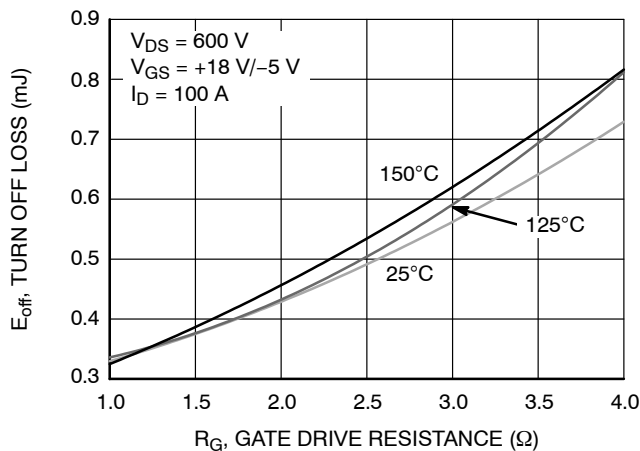
**Figure 12. Typical Switching Loss  $E_{on}$  vs.  $I_D$**



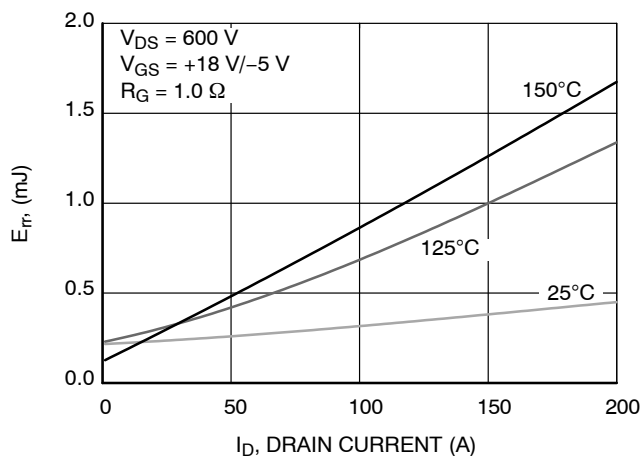
**Figure 13. Typical Switching Loss  $E_{on}$  vs.  $R_G$**



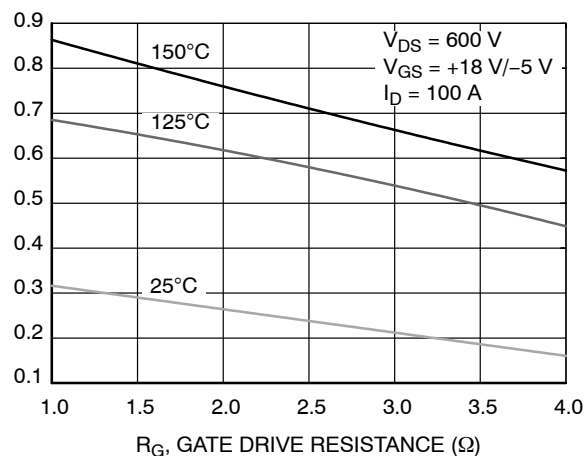
**Figure 14. Typical Switching Loss  $E_{off}$  vs.  $I_D$**



**Figure 15. Typical Switching Loss  $E_{off}$  vs.  $R_G$**

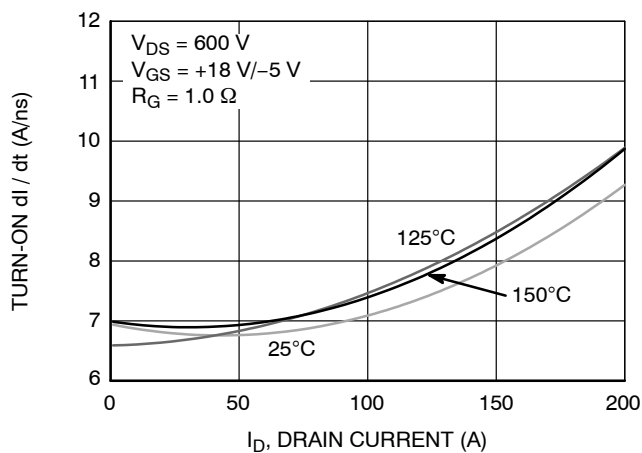


**Figure 16.  $E_{rr}$  vs.  $I_D$**

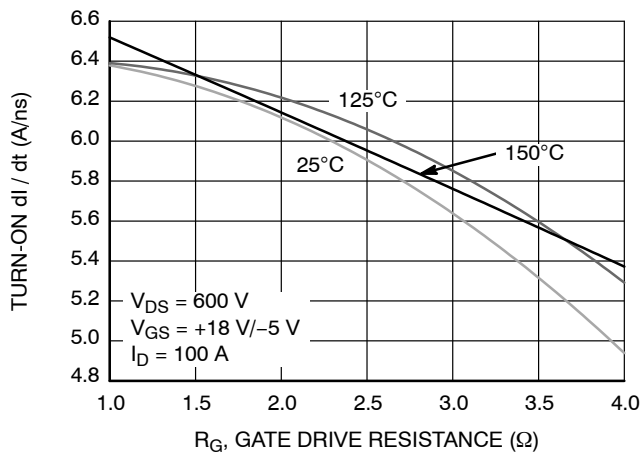


**Figure 17.  $E_{rr}$  vs.  $R_G$**

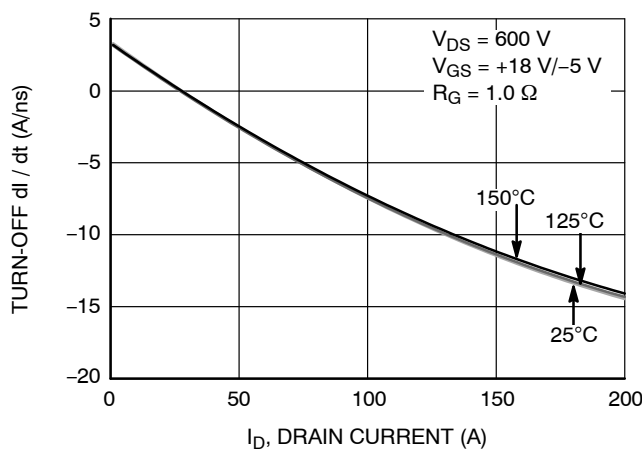
**TYPICAL CHARACTERISTIC**  
(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)



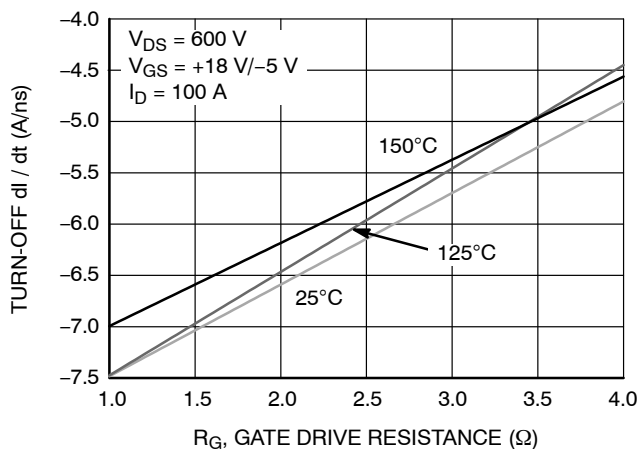
**Figure 18.  $di/dt$  ON vs.  $I_D$**



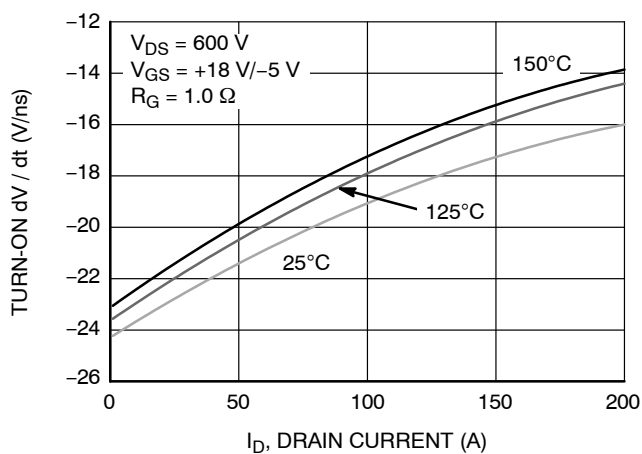
**Figure 19.  $di/dt$  ON vs.  $I_D$  vs.  $R_G$**



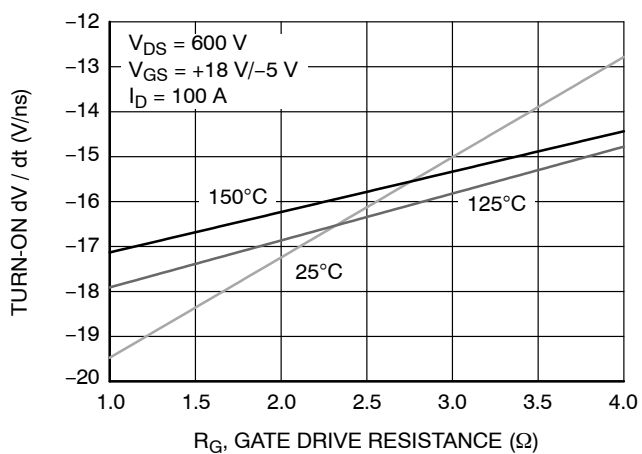
**Figure 20.  $di/dt$  OFF vs.  $I_D$**



**Figure 21.  $di/dt$  OFF vs.  $R_G$**



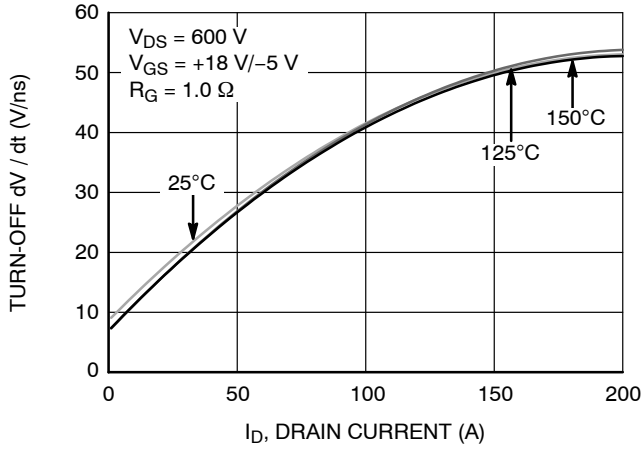
**Figure 22.  $dv/dt$  ON vs.  $I_D$**



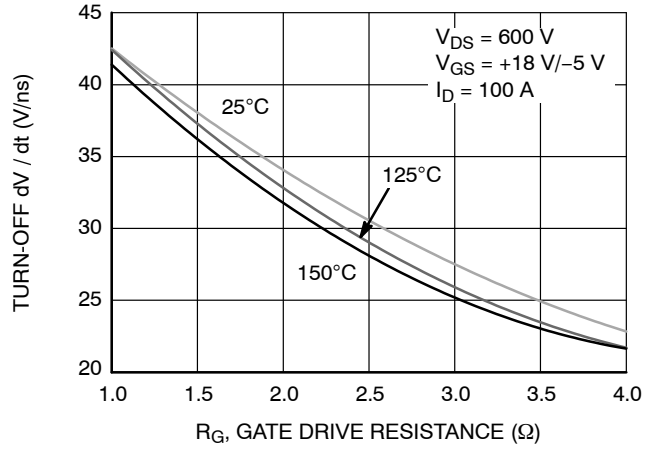
**Figure 23.  $dv/dt$  ON vs.  $R_G$**



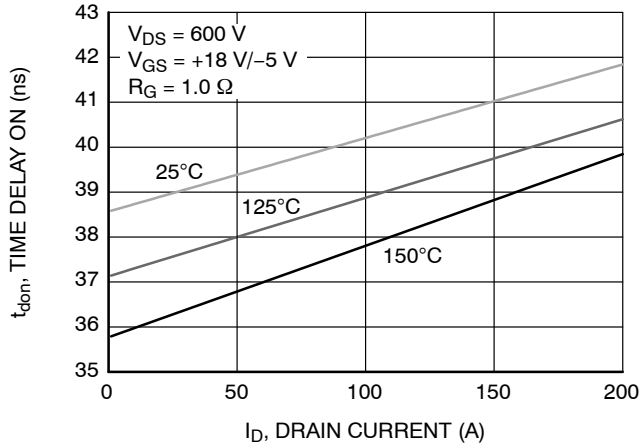
**TYPICAL CHARACTERISTIC**  
(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)



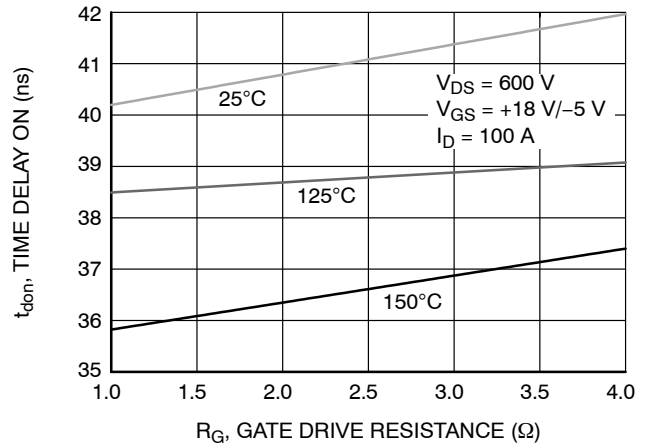
**Figure 24. dv/dt OFF vs.  $I_D$  vs.  $I_D$**



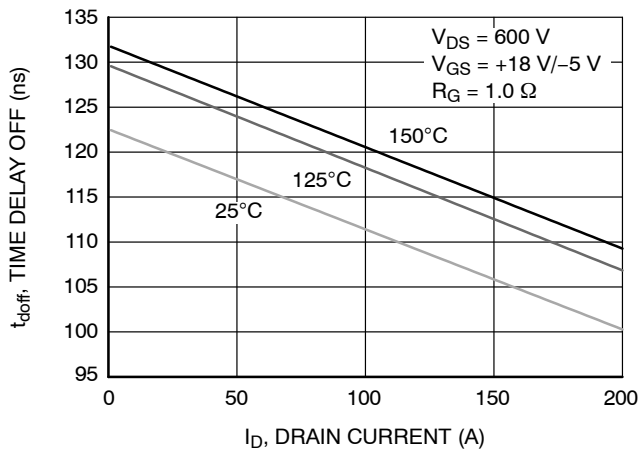
**Figure 25. dv/dt OFF vs.  $I_D$  vs.  $R_G$**



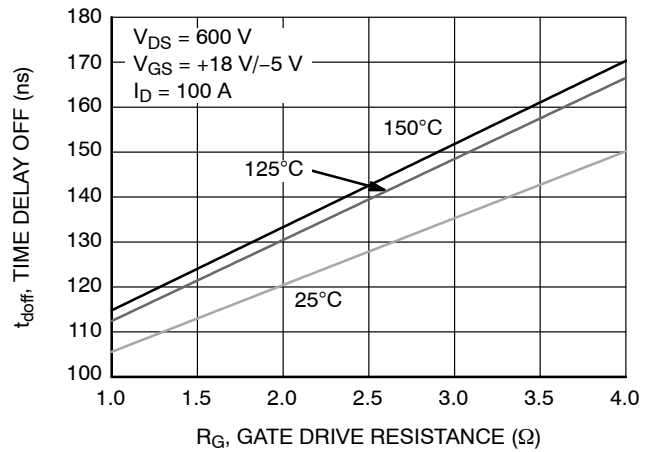
**Figure 26. Typical Switching Loss  $t_{don}$  vs.  $I_D$**



**Figure 27. Typical Switching Loss  $t_{don}$  vs.  $R_G$**

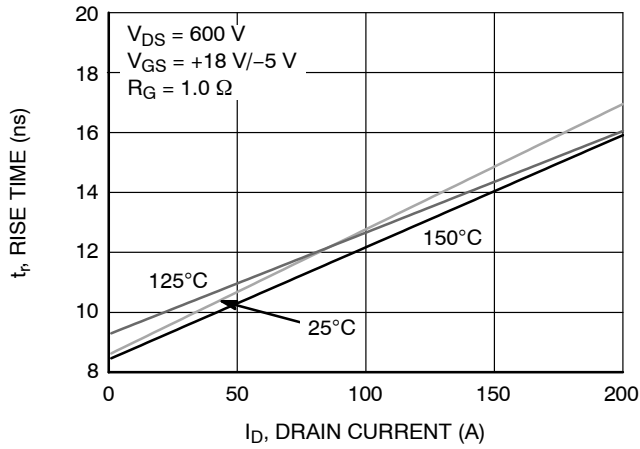


**Figure 28. Typical Switching Loss  $t_{doff}$  vs.  $I_D$**

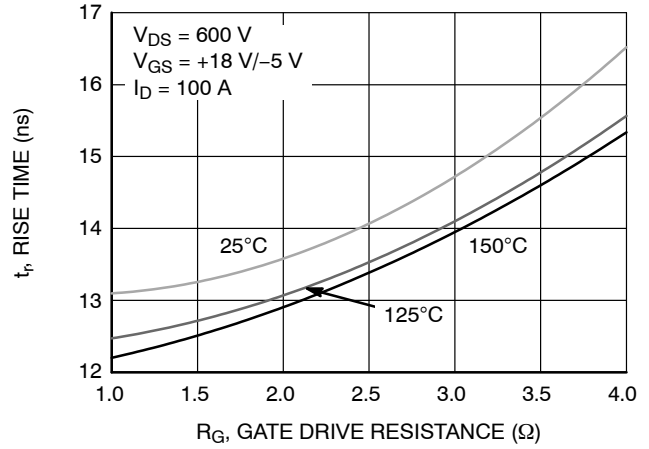


**Figure 29. Typical Switching Loss  $t_{doff}$  vs.  $R_G$**

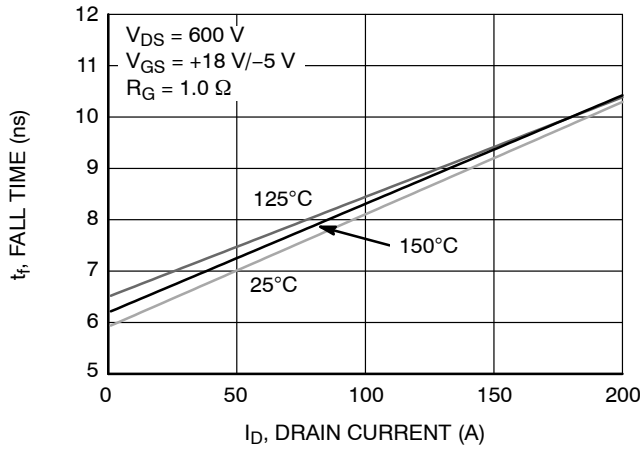
**TYPICAL CHARACTERISTIC**  
(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)



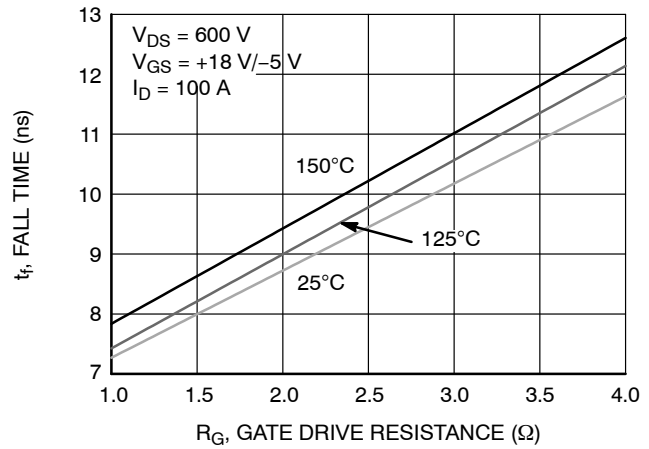
**Figure 30. Typical Switching Loss  $t_r$  vs.  $I_D$**



**Figure 31. Typical Switching Loss  $t_r$  vs.  $R_G$**



**Figure 32. Typical Switching Loss  $t_f$  vs.  $I_D$**



**Figure 33. Typical Switching Loss  $t_f$  vs.  $R_G$**

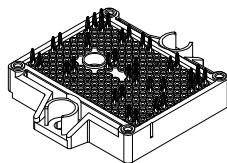
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**Table 1. FOSTER NETWORKS – M1, M2**

Foster Element #	M1		M2	
	Rth (K/W)	Cth (Ws/K)	Rth (K/W)	Cth (Ws/K)
1	0.007128913	0.014726553	0.007362625	0.014806718
2	0.012161919	0.065733420	0.012250209	0.068123520
3	0.007181004	0.193791778	0.008111627	0.172318664
4	0.016285510	0.295329029	0.015759800	0.310819905
5	0.129692183	0.184203426	0.130218477	0.185033159

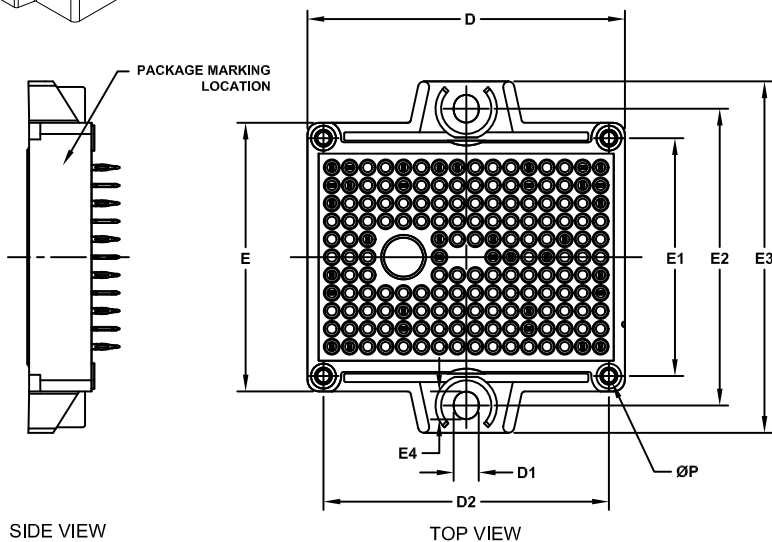
**Table 2. CAUER NETWORKS – M1, M2**

Cauer Element #	M1		M2	
	Rth (K/W)	Cth (Ws/K)	Rth (K/W)	Cth (Ws/K)
1	0.014060112	0.010299454	0.014544451	0.010347568
2	0.031541811	0.030614887	0.032745986	0.030654208
3	0.047951752	0.086377861	0.047636505	0.089568373
4	0.041739058	0.071218233	0.042559339	0.069836041
5	0.037156796	0.209773695	0.036216457	0.216319284



**PIM36 56.70x42.50x12.00**  
CASE 180BY  
ISSUE E

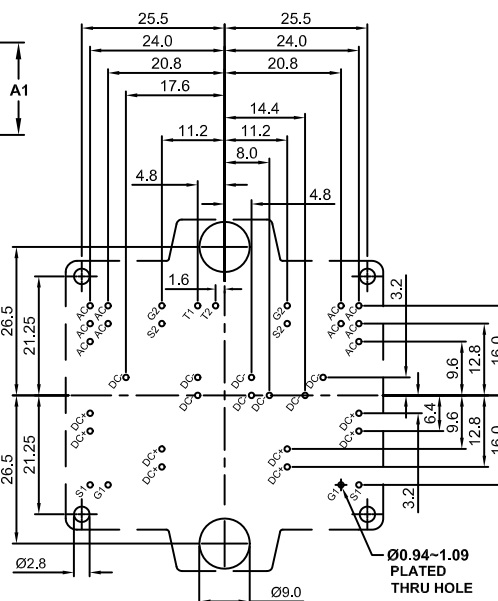
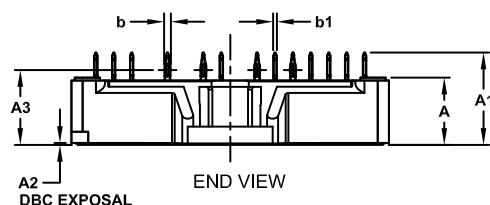
DATE 20 DEC 2023



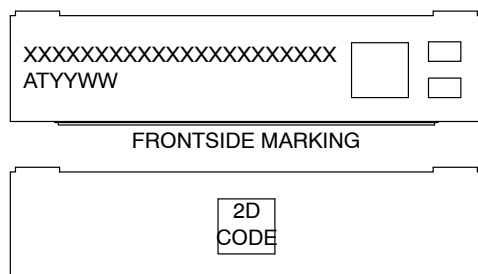
**NOTES:**

1. CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCE IS  $\pm 0.4\text{mm}$
3. PRESS FIT PIN

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	16.10	16.50	16.90
A2	0.00	0.35	0.60
A3	12.95	13.35	13.75
b	1.15	1.20	1.25
b1	0.59	0.64	0.69
D	56.40	56.70	57.00
D1	4.40	4.50	4.60
D2	50.85	51.00	51.15
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40



### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
AT = Assembly & Test Site Code  
YYWW = Year and Work Week Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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