DATA SHEET
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Si/SiC Hybrid Module – EliteSiC™, 3-channel Boost, Q1 Package

NXH240B120H3Q1P1G, NXH240B120H3Q1S1G

The NXH240B120H3Q1 is a case power module containing a three channel BOOST stage. The integrated field stop trench IGBTs and SiC Diodes provide lower conduction losses and switching losses, enabling designers to achieve high efficiency and superior reliability.

Features

- 1200 V Ultra Field Stop IGBTs
- Low Reverse Recovery and Fast Switching SiC Diodes
- Low Inductive Layout
- Press−fit Pins / Solder Pins
- Thermistor

Typical Applications

- Solar Inverters
- ESS

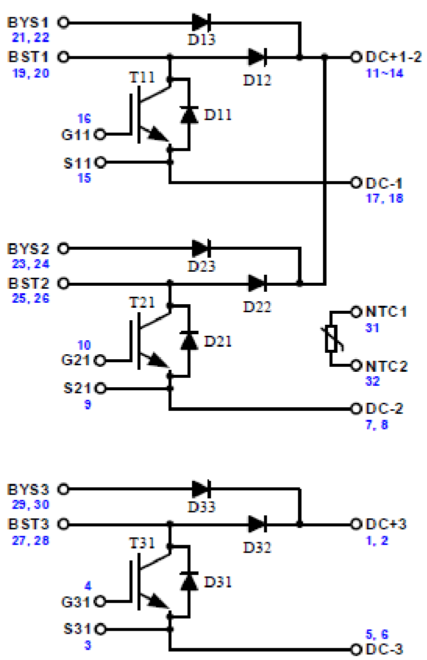
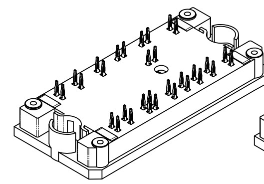
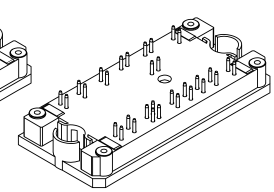


Figure 1. NXH240B120H3Q1 Schematic Diagram

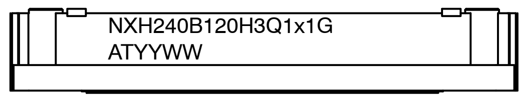




PIM32 (PRESS−FIT) CASE 180AX

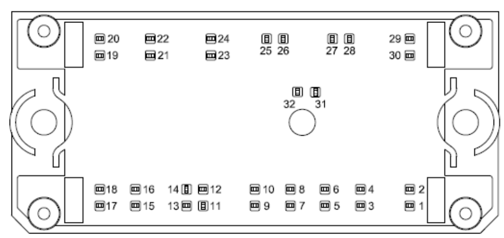
PIM32 (SOLDER−PINS) CASE 180BQ

MARKING DIAGRAM



NXH240B120H3Q1x1G = Specific Device Code
x = P or S
G = Pb−Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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Table 1. MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
IGBT (T11, T21, T31)			
Collector–Emitter Voltage	V_{CES}	1200	V
Gate–Emitter Voltage	V_{GE}	±20	V
Continuous Collector Current @ T_C = 80°C (T_J = 150°C)	I_C	92	A
Pulsed Collector Current (T_J = 150°C)	I_{Cpulse}	276	A
Maximum Power Dissipation (T_J = 150°C)	P_{tot}	266	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	150	°C
PROTECTION DIODE (D11, D21, D31)			
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Continuous Forward Current @ T_C = 80°C (T_J = 150°C)	I_F	41	A
Repetitive Peak Forward Current (T_J = 150°C)	I_{FRM}	123	A
Maximum Power Dissipation (T_J = 150°C)	P_{tot}	54	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	150	°C
SILICON CARBIDE BOOST DIODE (D12, D22, D32)			
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Continuous Forward Current @ T_C = 80°C (T_J = 175°C)	I_F	37	A
Repetitive Peak Forward Current (T_J = 175°C)	I_{FRM}	111	A
Maximum Power Dissipation (T_J = 175°C)	P_{tot}	99	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	175	°C
BYPASS DIODE (D13, D23, D33)			
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Continuous Forward Current @ T_C = 80°C (T_J = 150°C)	I_F	54	A
Repetitive Peak Forward Current (T_J = 150°C)	I_{FRM}	162	A
Maximum Power Dissipation (T_J = 150°C)	P_{tot}	64	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	150	°C
THERMAL PROPERTIES			
Storage Temperature range	T_{stg}	−40 to 150	°C
INSULATION PROPERTIES			
Isolation test voltage, t = 1 sec, 60 Hz	V_{is}	3000	V_{RMS}
Creepage distance		12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

Table 2. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
IGBT (T11, T21, T31)						
Collector−Emitter Cutoff Current	V_{GE} = 0 V, V_{CE} = 1200 V	I_{CES}	–	–	150	μA
Collector−Emitter Saturation Voltage	V_{GE} = 15 V, I_C = 80 A, T_J = 25°C	$V_{CE(sat)}$	–	2	2.7	V
	V_{GE} = 15 V, I_C = 80 A, T_J = 150°C		–	2.05	–	
Gate−Emitter Threshold Voltage	V_{GE} = V_{CE}, I_C = 80 μA	$V_{GE(TH)}$	4.2	5.2	6	V
Gate Leakage Current	V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	–	–	450	nA
Turn−on Delay Time	T_J = 25°C V_{CE} = 800 V, I_C = 50 A V_{GE} = +15 V, −9 V, R_G = 6 Ω	$t_{d(on)}$	–	100.51	–	ns
Rise Time		t_r	–	31.95	–	
Turn−off Delay Time		$t_{d(off)}$	–	377.15	–	
Fall Time		t_f	–	38.27	–	
Turn−on Switching Loss per Pulse		E_{on}	–	1660	–	μJ
Turn off Switching Loss per Pulse		E_{off}	–	2470	–	
Turn−on Delay Time	T_J = 125°C V_{CE} = 800 V, I_C = 50 A V_{GE} = +15 V, −9 V, R_G = 6 Ω	$t_{d(on)}$	–	89.65	–	ns
Rise Time		t_r	–	32	–	
Turn−off Delay Time		$t_{d(off)}$	–	440.78	–	
Fall Time		t_f	–	169.39	–	
Turn−on Switching Loss per Pulse		E_{on}	–	1660	–	μJ
Turn off Switching Loss per Pulse		E_{off}	–	5220	–	
Input Capacitance	V_{CE} = 20 V, V_{GE} = 0 V, f = 10 kHz	C_{ies}	–	19082	–	pF
Output Capacitance		C_{oes}	–	541	–	
Reverse Transfer Capacitance		C_{res}	–	387	–	
Total Gate Charge	V_{CE} = 600 V, I_C = 25 A, V_{GE} = ±15 V	Q_g	–	1320	–	nC
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 2 Mil ±2%, λ = 2.87 W/mK	R_{thJH}	–	0.464	–	°C/W
Thermal Resistance − chip−to−case		R_{thJC}	–	0.263	–	°C/W
PROTECTION DIODE (D11, D21, D31)						
Diode Forward Voltage	I_F = 30 A, T_J = 25°C	V_F	0.8	1.0	1.3	V
	I_F = 30 A, T_J = 150°C		–	0.98	–	
Thermal Resistance − chip−to−heatsink	Thermal grease, Thickness = 2 Mil ±2%, λ = 2.87 W/mK	R_{thJH}	–	1.303	–	°C/W
Thermal Resistance − chip−to−case		R_{thJC}	–	0.968	–	°C/W
SILICON CARBIDE BOOST DIODE (D12, D22, D32)						
Diode Forward Voltage	I_F = 30 A, T_J = 25°C	V_F	–	1.46	1.7	V
	I_F = 30 A, T_J = 175°C		–	2.12	–	
Reverse Recovery Time	T_J = 25°C V_{CE} = 800 V, I_C = 50 A V_{GE} = +15 V, −9 V, R_G = 6 Ω	t_{rr}	–	21.5	–	ns
Reverse Recovery Charge		Q_{rr}	–	87.82	–	μC
Peak Reverse Recovery Current		I_{RRM}	–	7.21	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	1282.75	–	A/μs
Reverse Recovery Energy		E_{rr}	–	23.61	–	μJ
Reverse Recovery Time	T_J = 125°C V_{CE} = 800 V, I_C = 50 A V_{GE} = +15 V, −9 V, R_G = 6 Ω	t_{rr}	–	25.73	–	ns
Reverse Recovery Charge		Q_{rr}	–	108.23	–	μC
Peak Reverse Recovery Current		I_{RRM}	–	7.6	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	1275.94	–	A/μs
Reverse Recovery Energy		E_{rr}	–	30.68	–	μJ

Table 3. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SILICON CARBIDE BOOST DIODE (D12, D22, D32)						
Thermal Resistance – chip–to–heatsink	Thermal grease, Thickness = 2 Mil ±2%, λ = 2.87 W/mK	R_{thJH}	–	0.958	–	°C/W
Thermal Resistance – chip–to–case		R_{thJC}	–	0.682	–	°C/W
BYPASS DIODE (D13, D23, D33)						
Diode Forward Voltage	I_F = 50 A, T_J = 25°C	V_F	–	1.1	1.3	V
	I_F = 50 A, T_J = 150°C		–	0.95	–	
Thermal Resistance – chip–to–heatsink	Thermal grease, Thickness = 2 Mil ±2%, λ = 2.87 W/mK	R_{thJH}	–	1.095	–	°C/W
Thermal Resistance – chip–to–case		R_{thJC}	–	0.767	–	°C/W
THERMISTOR CHARACTERISTICS						
Nominal resistance	T = 25°C	R_{25}	–	5	–	kΩ
Nominal resistance	T = 100°C	R_{100}	–	490.6	–	Ω
Deviation of R25		ΔR/R	–1	–	1	%
Power dissipation		P_D	–	5	–	mW
Power dissipation constant			–	1.3	–	mW/K
B–value	B(25/85), tolerance ±1%		–	3435	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH240B120H3Q1P1G	NXH240B120H3Q1P1G	Q1 BOOST, Case 180AX Press–fit Pins (Pb–Free)	21 Units / Blister Tray
NXH240B120H3Q1S1G	NXH240B120H3Q1S1G	Q1 BOOST, Case 180BQ Solder Pins (Pb–Free)	21 Units / Blister Tray

TYPICAL CHARACTERISTICS – IGBT (T1, T2, T3) AND SILICON CARBIDE SCHOTTKY DIODE (D12, D22, D32)

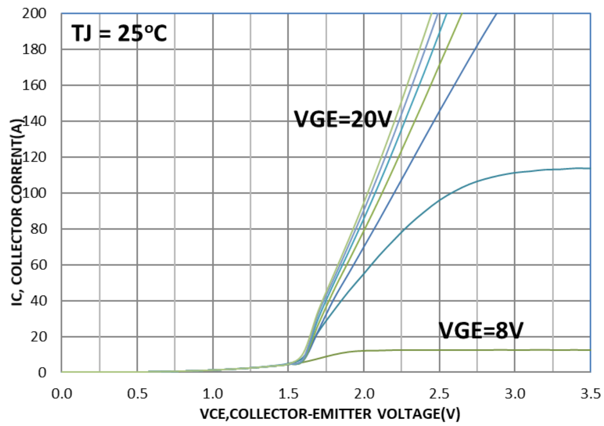

Figure 2. Typical Output Characteristics

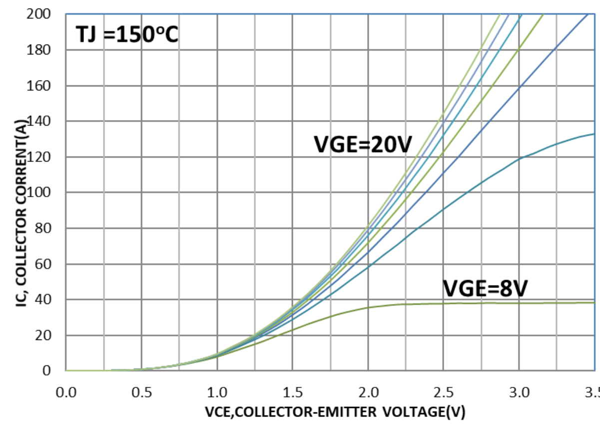

Figure 3. Typical Output Characteristics

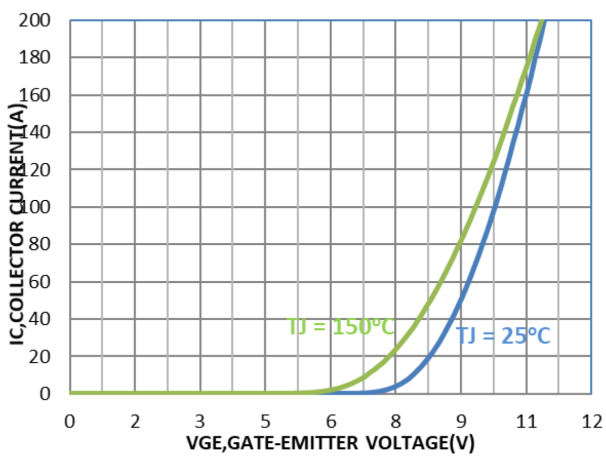

Figure 4. Typical Transfer Characteristics

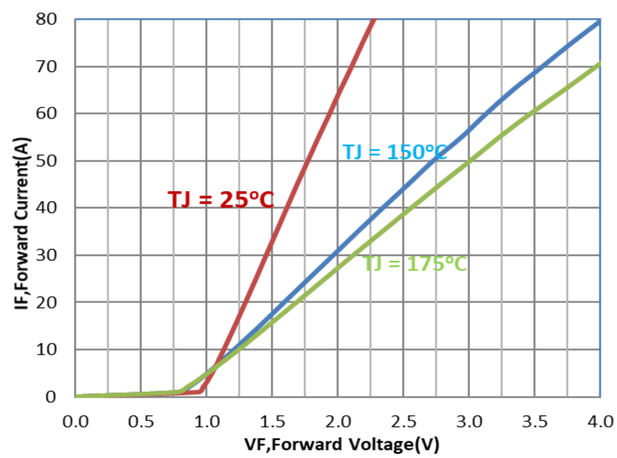

Figure 5. Diode Forward Characteristics

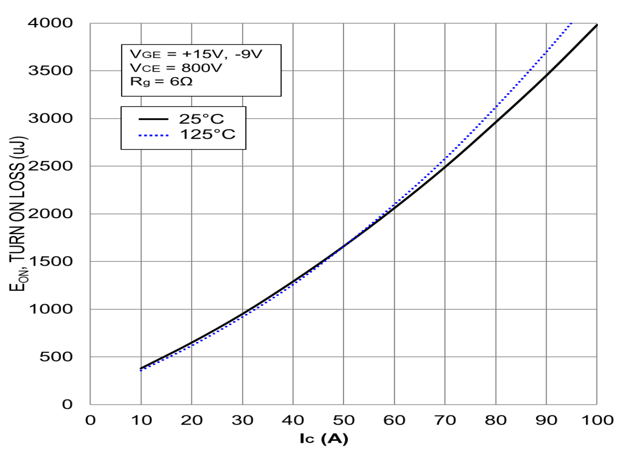

Figure 6. Typical Turn ON Loss vs. I_C

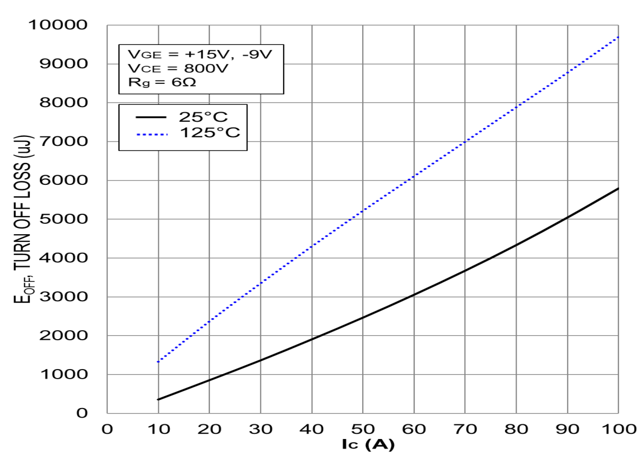

Figure 7. Typical Turn OFF Loss vs. I_C

TYPICAL CHARACTERISTICS – IGBT (T1, T2, T3) AND SILICON CARBIDE SCHOTTKY DIODE (D12, D22, D32)

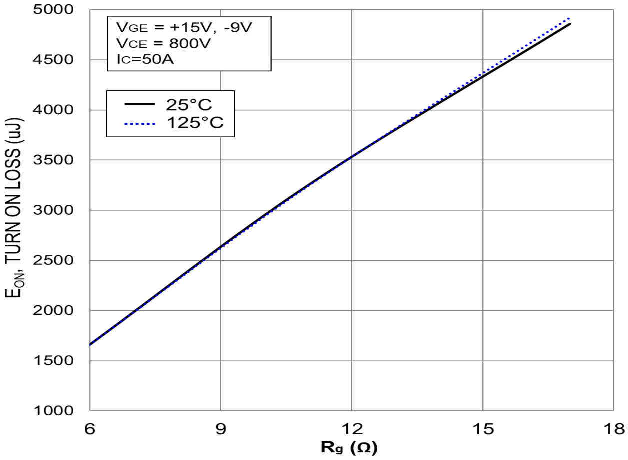

Figure 8. Typical Turn ON Loss vs. R_G

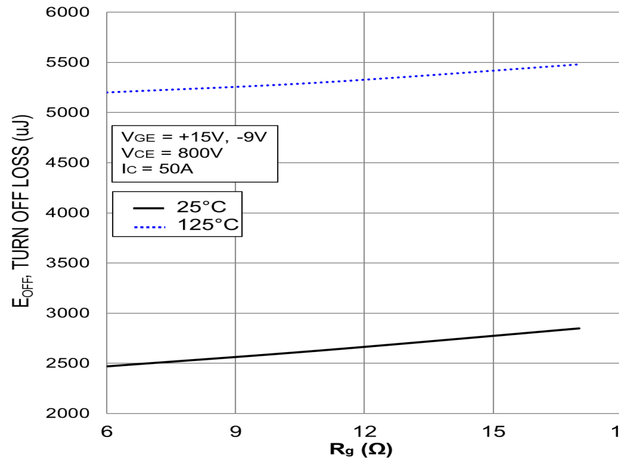

Figure 9. Typical Turn OFF Loss vs. R_G

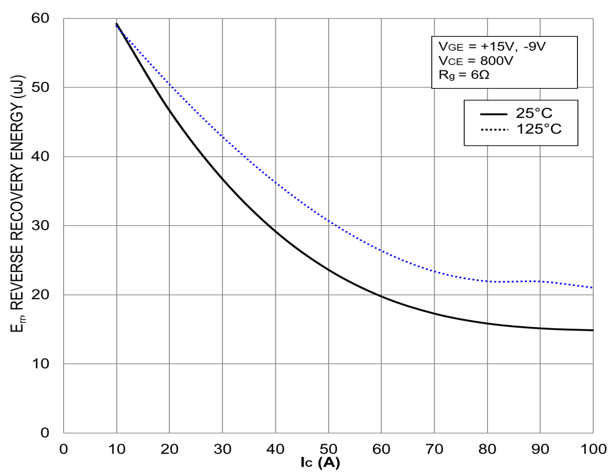

Figure 10. Typical Reverse Recovery Time vs. I_C

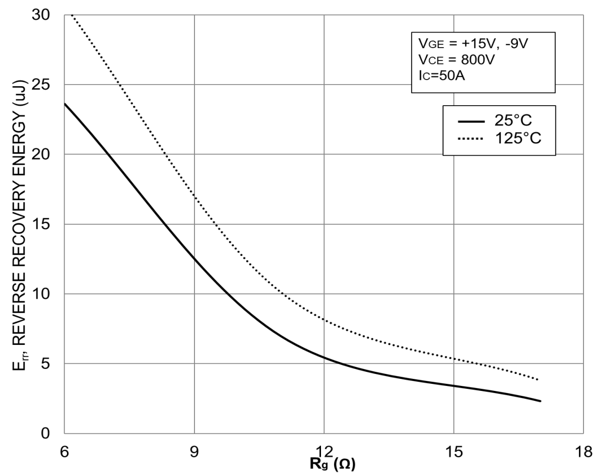

Figure 11. Typical Reverse Recovery Time vs. R_G

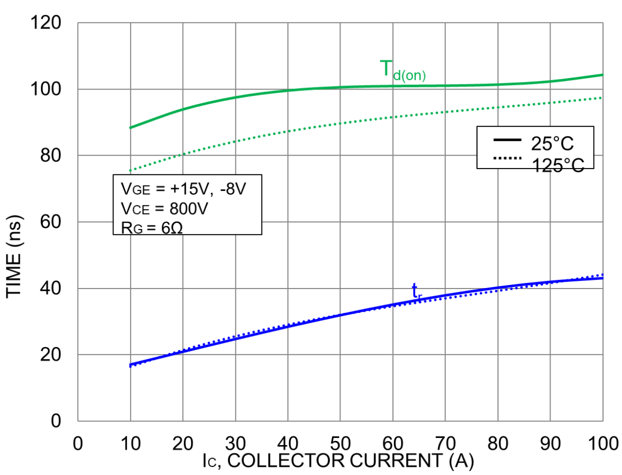

Figure 12. Typical Turn−On Switching Time vs. I_C

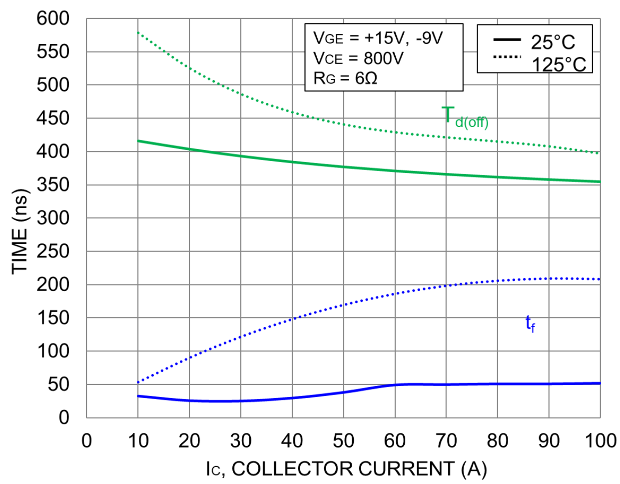

Figure 13. Typical Turn−Off Switching Time vs. I_C

TYPICAL CHARACTERISTICS – IGBT (T1, T2, T3) AND SILICON CARBIDE SCHOTTKY DIODE (D12, D22, D32)

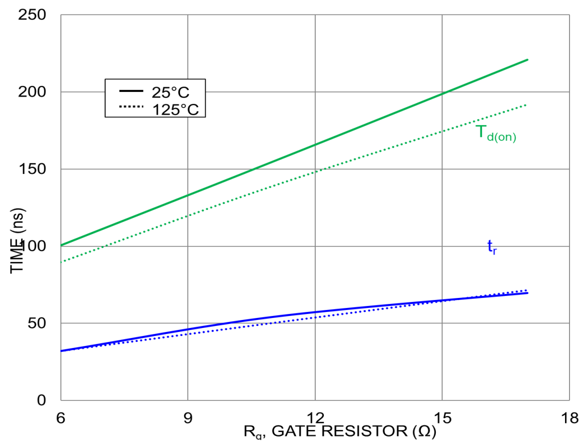

Figure 14. Typical Turn−On Switching Time vs. R_G

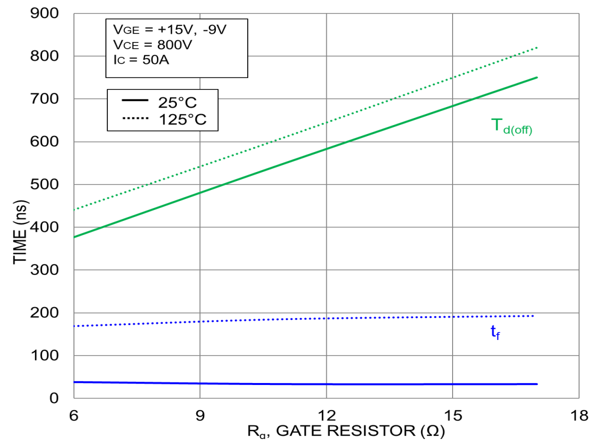

Figure 15. Typical Turn−Off Switching Time vs. R_G

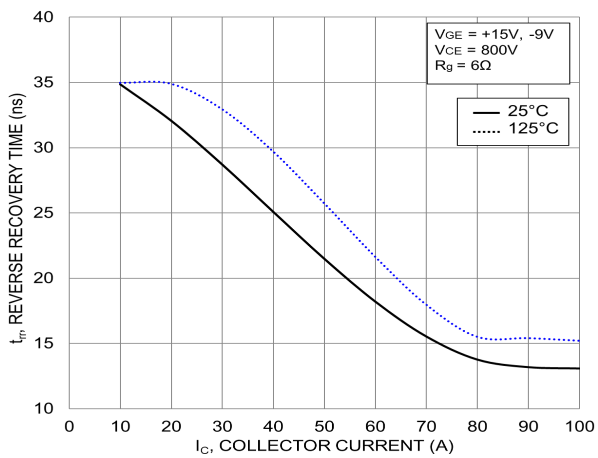

Figure 16. Typical Reverse Recovery Time vs. I_C

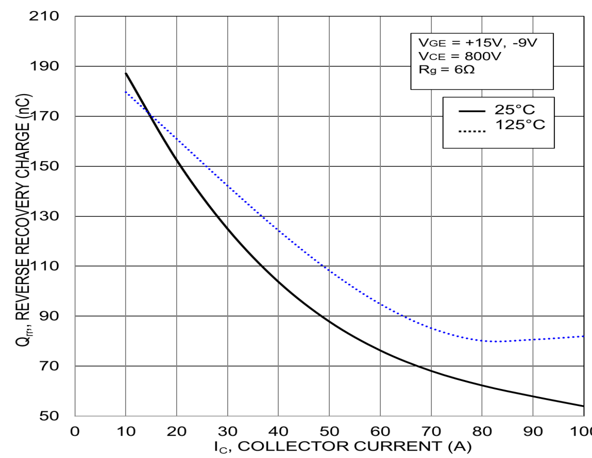

Figure 17. Typical Reverse Recovery Charge vs. I_C

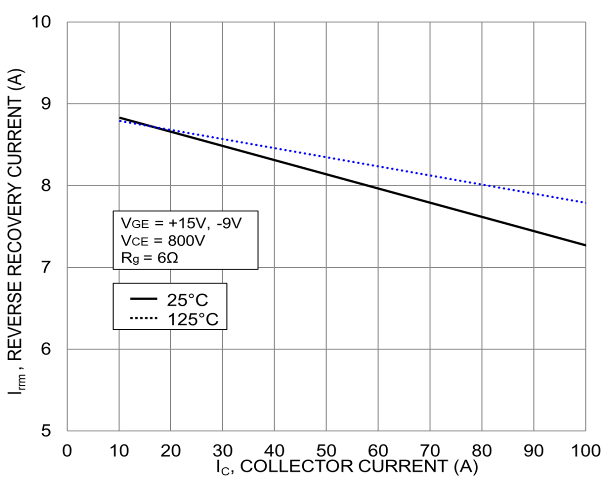

Figure 18. Typical Reverse Recovery Peak Current vs. I_C

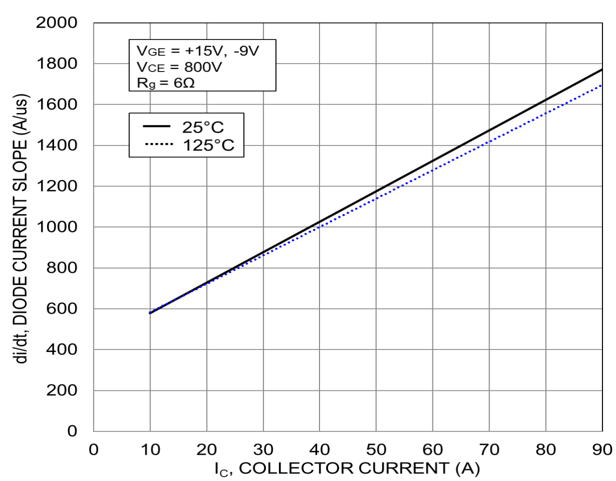

Figure 19. Typical di/dt vs. I_C

TYPICAL CHARACTERISTICS – IGBT (T1, T2, T3) AND SILICON CARBIDE SCHOTTKY DIODE (D12, D22, D32)

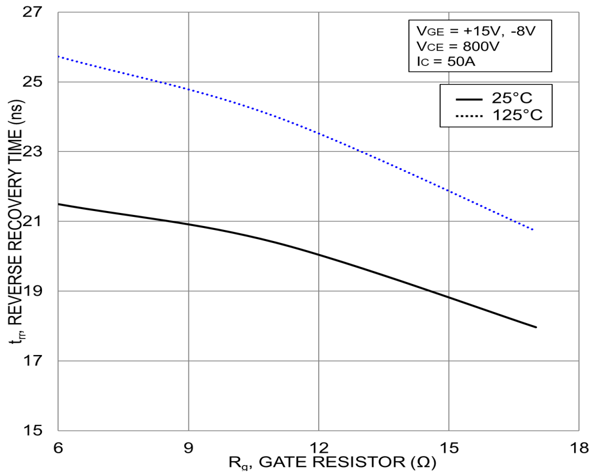

Figure 20. Typical Reverse Recovery Time vs. R_G

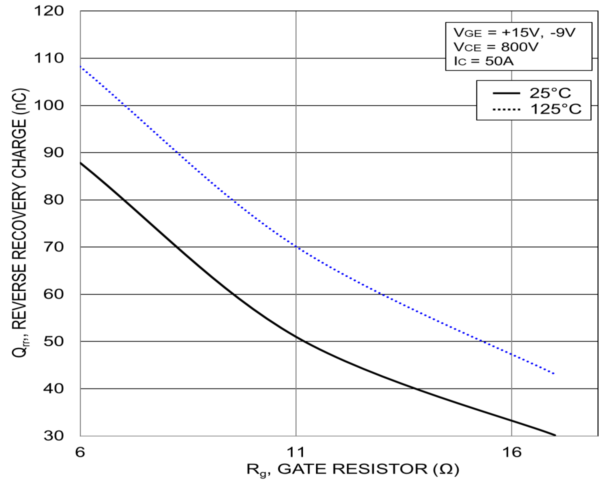

Figure 21. Typical Reverse Recovery Charge vs. R_G

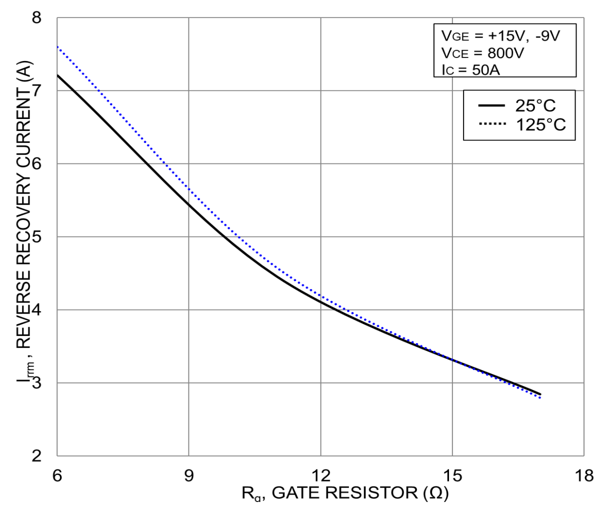

Figure 22. Typical Reverse Recovery Current vs. R_G

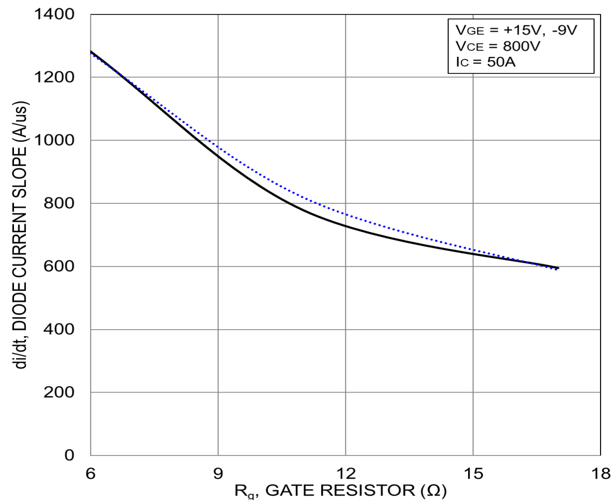

Figure 23. Typical di/dt Current Slope vs. R_G

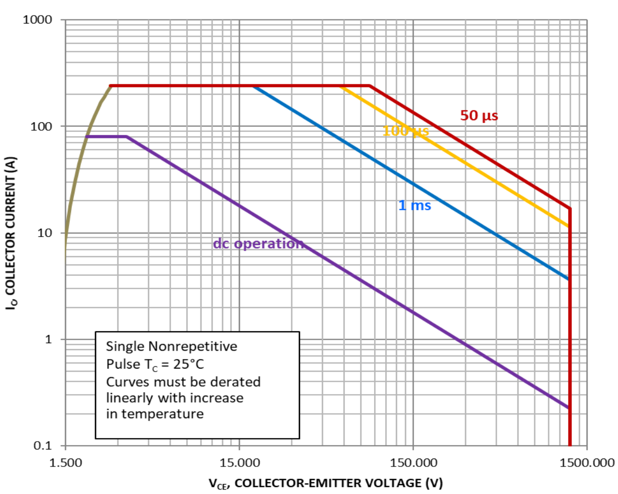

Figure 24. FBSOA

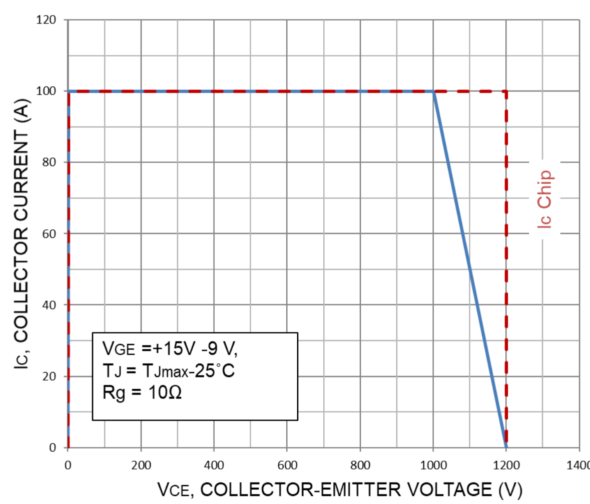

Figure 25. RBSOA

TYPICAL CHARACTERISTICS – IGBT (T1, T2, T3) AND SILICON CARBIDE SCHOTTKY DIODE (D12, D22, D32)

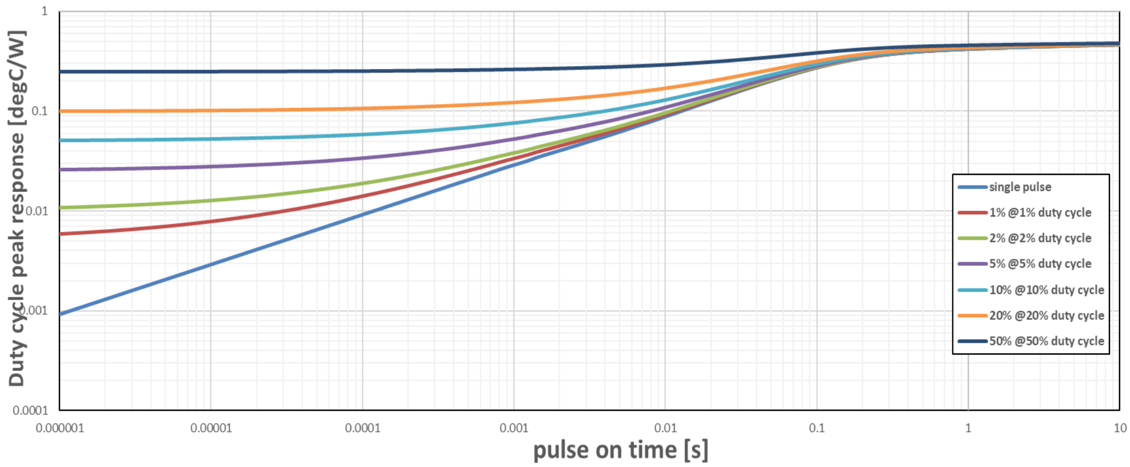

Figure 26. Transient Thermal Impedance (T1, T2, T3)

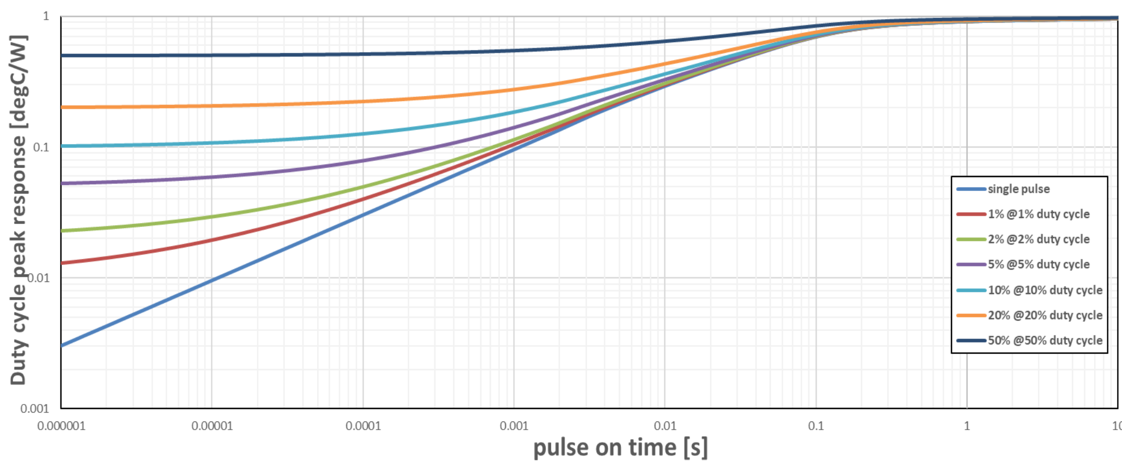

Figure 27. Transient Thermal Impedance (D12, D22, D32)

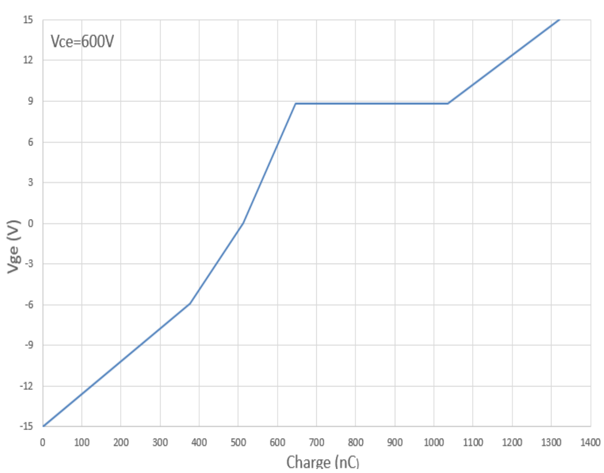

Figure 28. Gate Voltage vs. Gate Charge

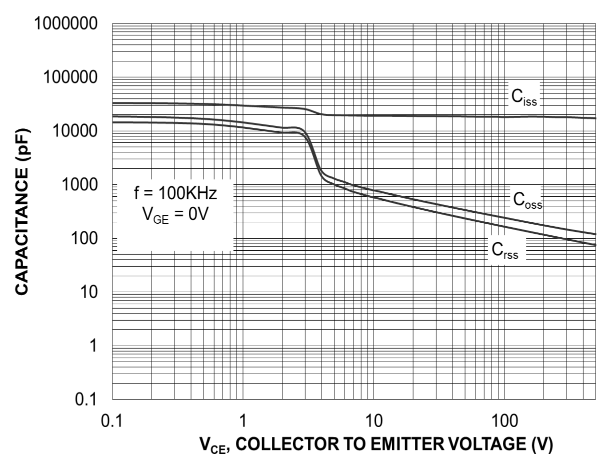

Figure 29. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – DIODE (D13, D23, D33)

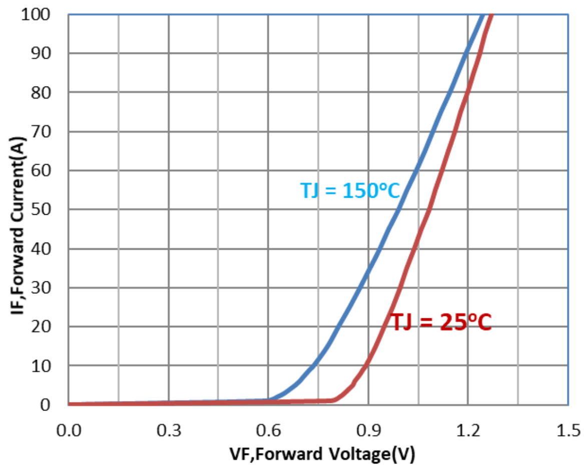

Figure 30. Diode Forward Characteristics

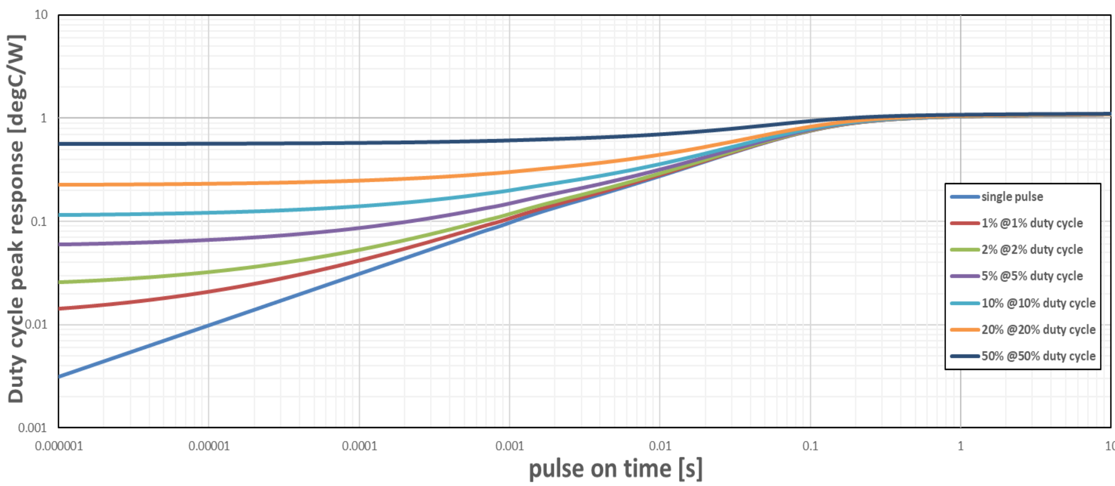

Figure 31. Transient Thermal Impedance

TYPICAL CHARACTERISTICS – DIODE (D11, D21, D31)

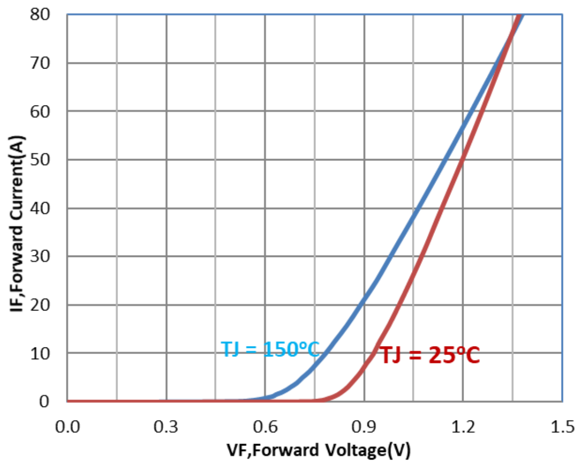

Figure 32. Diode Forward Characteristics

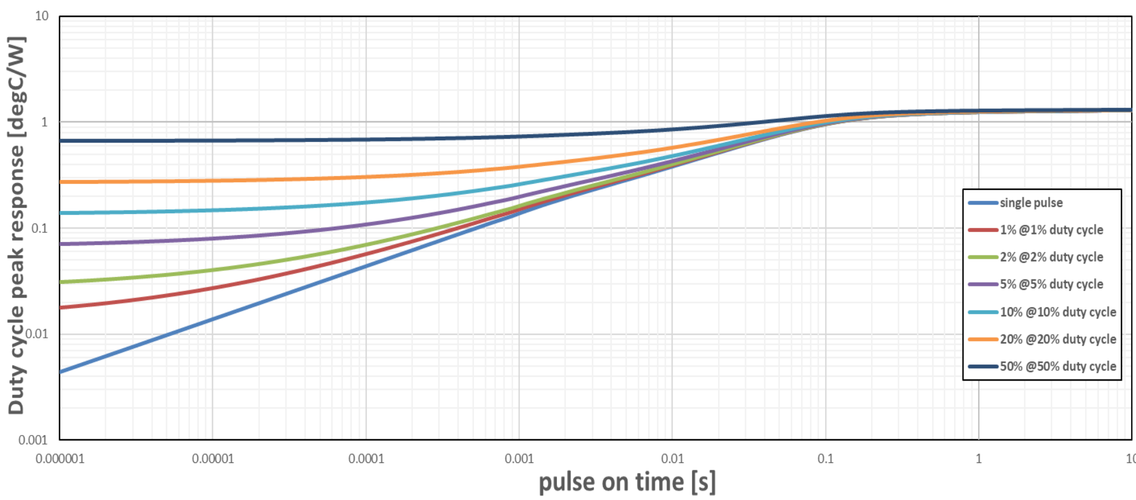

Figure 33. Transient Thermal Impedance

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PIM41, 93x47 (PRESS FIT)

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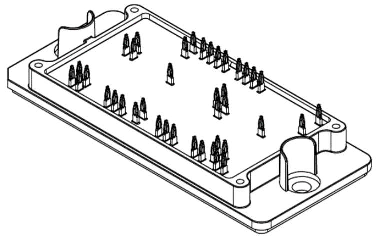
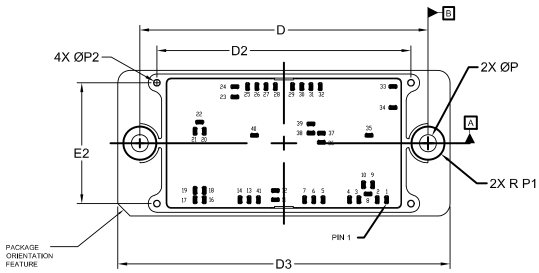
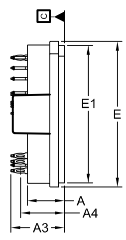
DATE 19 MAR 2019





TOP VIEW

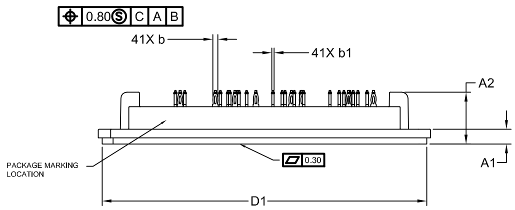


END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.60	12.00	12.40
A1	4.40	4.70	5.00
A2	16.30	16.70	17.10
A3	16.90	17.30	17.70
A4	13.97	14.18	14.39
b	1.61	1.66	1.71
b1	0.75	0.80	0.85
D	92.90	93.00	93.10
D1	104.45	104.75	105.05
D2	81.80	82.00	82.20
D3	106.90	107.20	107.50
E	46.70	47.00	47.30
E1	44.10	44.40	44.70
E2	38.80	39.00	39.20
P	5.40	5.50	5.60
P1	5.15	5.35	5.55
P2	2.00	2.20	2.40

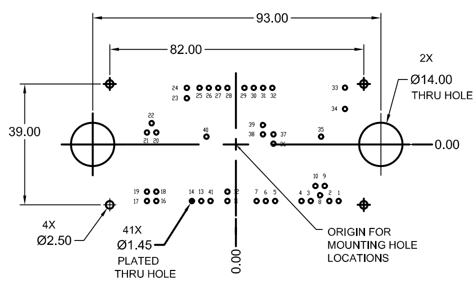
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED AT DIMENSION A4.
4. POSITION OF THE CENTER OF THE TERMINALS AND MOUNTING HOLES IS DETERMINED FROM DATUM B THE CENTER OF DIMENSION D, X DIRECTION, AND FROM DATUM A, Y DIRECTION. POSITIONAL TOLERANCE AS NOTED IN DRAWING, APPLIES TO BOTH TERMINALS AND MOUNTING HOLES IN BOTH DIRECTIONS.
5. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.
6. MOUNTING RECOMMENDATION IS SHOWN AS VIEWED FROM THE PCB TOP LAYER LOOKING DOWN TO SUBSEQUENT LAYERS.



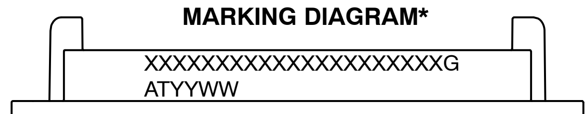
SIDE VIEW

PIN	PIN POSITION		PIN	PIN POSITION	
	X	Y		X	Y
1	33.15	-18.25	23	-15.85	14.90
2	30.15	-18.25	24	-15.85	18.25
3	24.15	-18.25	25	-11.75	18.25
4	21.15	-18.25	26	-8.75	18.25
5	12.65	-18.25	27	-5.75	18.25
6	9.65	-18.25	28	-2.75	18.25
7	6.65	-18.25	29	2.75	18.25
8	27.15	-16.40	30	5.75	18.25
9	28.65	-13.40	31	8.75	18.25
10	25.65	-13.40	32	11.75	18.25
11	-2.75	-18.25	33	35.20	18.30
12	-2.75	-15.25	34	35.20	11.45
13	-11.20	-18.25	35	27.50	2.50
14	-14.20	-18.25	36	12.10	0.25
15	n/a	n/a	37	12.10	3.25
16	-25.70	-18.25	38	8.70	3.25
17	-28.70	-18.25	39	8.70	6.25
18	-25.70	-15.25	40	-9.50	2.50
19	-28.70	-15.25	41	-8.20	-18.25
20	-25.70	3.85			
21	-28.70	3.85			
22	-27.20	6.85			



RECOMMENDED
MOUNTING PATTERN

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
G = Pb−Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	PIM41, 93x47 (PRESS FIT)	PAGE 1 OF 1

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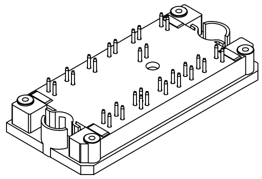
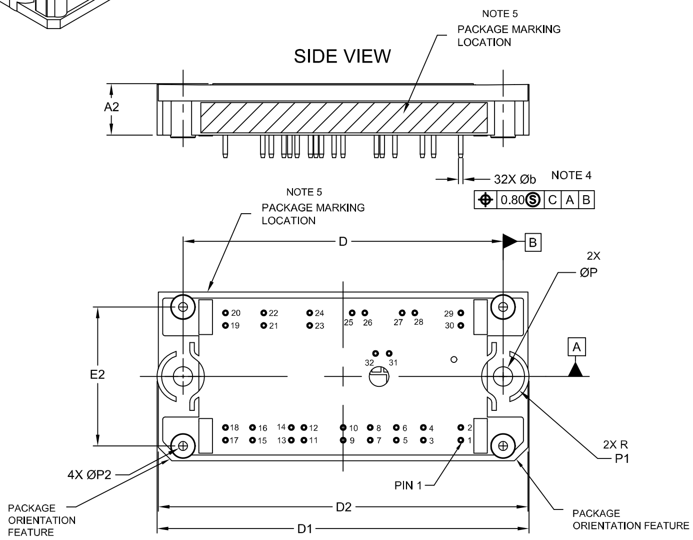
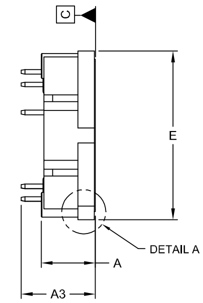


PIM32, 71x37.4 (SOLDER PIN)

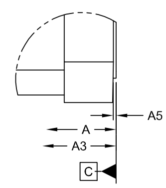
CASE 180BQ
ISSUE A

DATE 23 JUL 2021



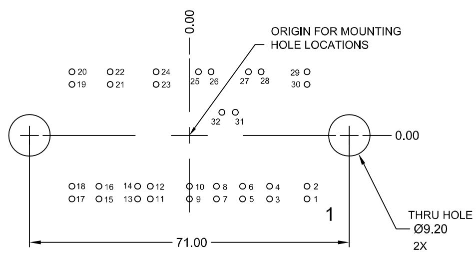


DIM	MILLIMETERS MIN.	NOM.	MAX.
A	11.70	12.00	12.30
A2	10.90	11.40	11.90
A3	15.90	16.40	16.90
A5	0.00	-	0.45
b	0.90	1.00	1.10
D	70.50	71.00	71.50
D1	82.00	82.50	83.00
D2	81.50	82.00	82.50
E	36.90	37.40	37.90
E2	30.30	30.80	31.30
P	4.30	4.40	4.50
P1	4.55	4.75	4.95
P2	2.00 REF		



NOTE 4

PIN	PIN POSITION X	Y	PIN	PIN POSITION X	Y
1	26.10	-14.10	17	-26.10	-14.10
2	26.10	-11.30	18	-26.10	-11.30
3	17.80	-14.10	19	-26.10	11.30
4	17.80	-11.30	20	-26.10	14.10
5	11.80	-14.10	21	-17.60	11.30
6	11.80	-11.30	22	-17.60	14.10
7	6.00	-14.10	23	-7.40	11.30
8	6.00	-11.30	24	-7.40	14.10
9	0.00	-14.10	25	2.00	14.10
10	0.00	-11.30	26	4.80	14.10
11	-8.70	-14.10	27	13.10	14.10
12	-8.70	-11.30	28	15.90	14.10
13	-11.50	-14.10	29	26.10	14.10
14	-11.50	-11.30	30	26.10	11.30
15	-20.10	-14.10	31	10.20	5.10
16	-20.10	-11.30	32	7.20	5.10

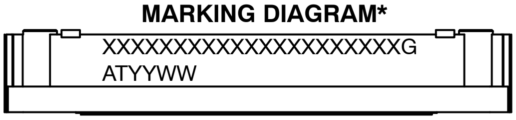


RECOMMENDED MOUNTING PATTERN*
For additional information on our Pb-Free strategy and soldering details, please download the On Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

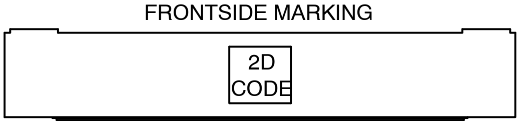
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 1.00 AND 3.00 FROM THE TERMINAL TIP.
4. POSITION OF THE CENTER OF THE TERMINALS AND MOUNTING HOLES IS DETERMINED FROM DATUM B THE CENTER OF DIMENSION D, X DIRECTION, AND FROM DATUM A, Y DIRECTION. POSITIONAL TOLERANCE, AS NOTED IN DRAWING, APPLIES TO BOTH TERMINALS AND MOUNTING HOLES IN BOTH DIRECTIONS.
5. PACKAGE MARKING IS LOCATED, AS SHOWN, ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES.
6. MOUNTING RECOMMENDATION IS SHOWN AS VIEWED FROM THE PCB TOP LAYER LOOKING DOWN TO SUBSEQUENT LAYERS.

GENERIC MARKING DIAGRAM*



FRONTSIDE MARKING



BACKSIDE MARKING

XXXXX = Specific Device Code
G = Pb−Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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