3-Level ANPC Inverter Module

Preliminary Document

NXH270A120M3F5PHG

The NXH270A120M3F5PHG is a power module in F5BP containing an A-type neutral point clamped three-level inverter. The integrated field stop trench IGBTs and FRDs and SiC MOSFET provide lower conduction and switching losses, enabling designers to achieve high efficiency, higher power and superior reliability.

Features

- A-type Neutral Point Clamped Three-level Inverter Module
- 1200 V SiC MOSFETs
- 1200 V Field Stop 7 IGBTs
- Low Inductive layout
- Press Fit Pins
- Integrated NTC Thermistor
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Typical Applications

- Energy Storage System
- Solar Inverters

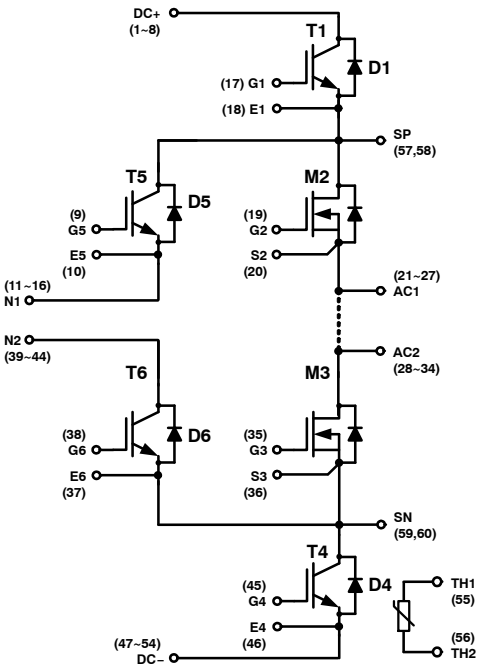
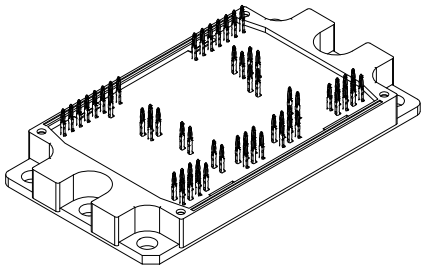


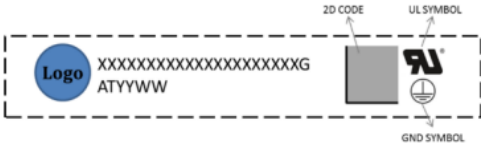
Figure 1. NXH270A120M3F5PHG Schematic Diagram

This Preliminary document is for informational purposes only. **onsemi** may update or withdraw it without notice. Content and referenced products are under development and subject to change.



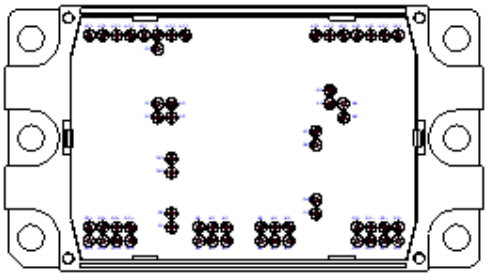
PIM-60 112x62 (PRESS FIT PIN)
CASE 180DR

MARKING DIAGRAM



XXXXX = Device Code
G = Pb-Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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MODULE CHARACTERISTICS

Operating Temperature under Switching Condition	T_{VJOP}	−40 to 175	°C
Storage Temperature Range	T_{stg}	−40 to 125	°C
Isolation Test Voltage, t = 60 s, 50 Hz	V_{is}	4000	V_{RMS}
Stray Inductance	L_{sCE}	10	nH
Terminal Connection Torque (M5, Screw)	M	3−5	Nm
Weight	G	260	g
Creepage Distance (Terminal to Heatsink)		17.4	mm
Creepage Distance (Terminal to Terminal)		7.0	mm
Clearance Distance (Terminal to Heatsink)		15.6	mm
Clearance Distance (Terminal to Terminal)		6.0	mm
Comparative Tracking Index	CTI	>600	

ABSOLUTE MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter	Symbol	Value	Unit
SiC MOSFET (M2, M3)			
Drain-Source Voltage	V_{DSS}	1200	V
Gate-Source Voltage	V_{GS}	+22/−10	V
Recommended Operating Gate−Source Voltage	V_{GS_OP}	+18/−3~−5	V
Continuous Drain Current @ T_C = 80 °C, (T_{VJ} = 175 °C)	I_D	463	A
Pulsed Peak Drain Current @ T_C = 80 °C (T_{VJ} = 175 °C), T_{pulse} = 1 ms	I_{Dpulse}	1200	A
Power Dissipation (T_{VJ} = 175 °C, T_C = 80 °C)	Pt_{ot}	826	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	175	°C
OUTER and NEUTRAL POINT IGBTs (T1, T4, T5, T6)			
Collector-Emitter Voltage	V_{CES}	1200	V
Gate-Emitter Voltage Positive Transient Gate-emitter Voltage (T_{pulse} = 5 μs, D < 0.10)	V_{GE}	±20 30	V
Continuous Collector Current @ T_C = 80 °C (T_{VJ} = 175 °C)	I_C	299	A
Pulsed Peak Collector Current @ T_C = 80 °C (T_{VJ} = 175 °C), T_{pulse} = 1 ms	I_{Cpulse}	800	A
Power Dissipation (T_{VJ} = 175 °C, T_C = 80 °C)	P_{tot}	742	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	175	°C
OUTER and NEUTRAL POINT DIODES (D1, D4, D5, D6)			
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Continuous Forward Current @ T_C = 80 °C (T_{VJ} = 175 °C)	I_F	260	A
Repetitive Peak Forward Current (T_{VJ} = 175 °C), T_{pulse} = 1 ms	I_{FRM}	800	A
Maximum Power Dissipation @ T_C = 80 °C (T_{VJ} = 175 °C)	P_{tot}	463	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. For optimum lifetime and reliability, **onsemi** recommends continuous V_{CE} (Half DC link voltage) operating conditions do not exceed 80% of the maximum ratings.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SIC MOSFET (M2, M3)						
Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 1200 V	I_{DSS}	–	–	1	mA
Drain-Source On Resistance	V_{GS} = 18 V, I_D = 450 A, T_{VJ} = 25 °C	$R_{DS(ON)}$	–	1.8	2.35	mΩ
	V_{GS} = 18 V, I_D = 450 A, T_{VJ} = 150 °C		–	3.5	–	
	V_{GS} = 18 V, I_D = 450 A, T_{VJ} = 175 °C		–	3.9	–	
Gate-Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 198 mA, T_{VJ} = 25 °C (tested after I_{GSS} @ = +22 V)	$V_{GS(TH)}$	2.3	3.0	4.5	V
	V_{GS} = V_{DS}, I_D = 198 mA, T_{VJ} = 175 °C (tested after I_{GSS} @ = +22 V)		–	2.3	–	
Gate Leakage Current	V_{GS} = 22 V, V_{DS} = 0 V	I_{GSS}	–	–	1	μA
	V_{GS} = −10 V, V_{DS} = 0 V		−1	–	–	
Internal Gate Resistor	F = 1 MHz	R_{GINT}	–	1.5	–	Ω
Turn-on Delay Time	T_J = 25 °C V_{DS} = 800 V, I_D = 300 A V_{GS} = −5 V to +18 V, R_G = 4 Ω	$t_{d(on)}$	–	118.02	–	ns
Rise Time		t_r	–	77.26	–	
Turn-off Delay Time		$t_{d(off)}$	–	328.55	–	
Fall Time		t_f	–	38.25	–	
Turn-on Switching Loss per Pulse		E_{ON}	–	6.13	–	mJ
Turn off Switching Loss per Pulse		E_{OFF}	–	10.24	–	
Turn-on Delay Time	T_J = 150 °C V_{DS} = 800 V, I_D = 300 A V_{GS} = −5 V to +18 V, R_G = 4 Ω	td(on)	–	110.48	–	ns
Rise Time		t_r	–	73.8	–	
Turn-off Delay Time		td(off)	–	380.85	–	
Fall Time		t_f	–	39.05	–	
Turn-on Switching Loss per Pulse		E_{ON}	–	6.24	–	mJ
Turn off Switching Loss per Pulse		E_{OFF}	–	10.33	–	
Total Gate Charge	V_{DS} = 800 V, V_{GS} = −10/18 V, I_D = 225 A	$Q_{G(TOTAL)}$		1512		nC
Gate-Source Charge		Q_{GS}		272		
Gate-Drain Charge		Q_{GD}		336		
Input Capacitance	V_{DS} = 800 V, V_{GS} = 0 V, f = 1 MHz	C_{ISS}	–	37647.4	–	pF
Output Capacitance		C_{OSS}	–	1705.48	–	
Reverse Transfer Capacitance		C_{RSS}	–	35.58	–	
Diode Forward Voltage	V_{GS} = −5 V, I_D = 300 A, T_J = 25 °C	V_{SD}	3.5	4.44	5.5	V
	V_{GS} = −5 V, I_D = 300 A, T_J = 150 °C		–	4.06	–	
Thermal Resistance – Chip-to-heatsink	Thermal grease, Thickness < 100 μm Thermal conductivity= 3.3 W/mK	R_{thJH}		0.159		°C/W
Thermal Resistance – Chip-to-case		R_{thJC}		0.115		°C/W
OUTER and NEUTRAL POINT IGBTs (T1, T4, T5, T6)						
Collector-Emitter Cutoff Current	V_{GE} = 0 V, V_{CE} = 1200 V	I_{CES}	–	–	1	mA
Collector-Emitter Saturation Voltage	V_{GE} = 15 V, I_C = 270 A, T_J = 25 °C	$V_{CE(sat)}$	–	1.50	2.0	V
	V_{GE} = 15 V, I_C = 270 A, T_J = 175 °C		–	1.75	–	
Gate-Emitter Threshold Voltage	V_{GE} = V_{CE}, I_C = 270 mA	$V_{GE(TH)}$	5.0	6.0	7.0	V
Gate Leakage Current	V_{GE} = ±20 V, V_{CE} = 0 V	I_{GES}	–	–	300	nA
Internal Gate Resistor	F = 1 MHz	R_{GINT}	–	4.25	–	Ω

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
OUTER and NEUTRAL POINT IGBTs (T1, T4, T5, T6)						
Turn-off Safe Operating Area	V_{CC} =800V, Vce< 1200V at Chip Level, T_{VJ} < 175 °C		–	–	540	A
Total Gate Charge	V_{CE} = 800 V, V_{GE} = −15/15 V, I_C = 135 A	$Q_{G(TOTAL)}$	–	1904	–	nC
Gate-Emitter Charge		Q_{GE}	–	256	–	
Gate-Collector Charge		Q_{GC}	–	408	–	
Input Capacitance	V_{CE} = 20 V. V_{GE} = 0 V. f = 100 kHz	C_{IES}	–	35151.5	–	pF
Output Capacitance		C_{OES}	–	1420.23	–	
Reverse Transfer Capacitance		C_{RES}	–	188.56	–	
Thermal Resistance – Chip-to-heatsink	Thermal grease, Thickness < 100 μm Thermal conductivity = 3.3 W/mK	R_{thJH}	–	0.196	–	°C/W
Thermal Resistance – Chip-to-case		R_{thJC}	–	0.128	–	°C/W
OUTER and NEUTRAL POINT DIODEs (D1, D4, D5, D6)						
Diode Forward Voltage	I_F = 340 A, T_{VJ} = 25 °C	V_F	–	2.03	2.3	V
	I_F = 340 A, T_{VJ} = 175 °C		–	2.09	–	
Surge Forward Current	tp = 10 ms, T_{VJ} = 150 °C	I_{FSM}	–	–	1000	A
I^2t	tp = 10 ms, T_{VJ} = 150 °C	I^2t	–	–	5000	A^2s
Thermal Resistance – Chip-to-heatsink	Thermal grease, Thickness < 100 μm Thermal conductivity= 3.3 W/mK	R_{thJH}	–	0.287	–	°C/W
Thermal Resistance – Chip-to-case		R_{thJC}	–	0.205	–	°C/W
THERMISTOR CHARACTERISTICS						
Nominal Resistance	T = 25 °C	R25	–	5	–	k
Nominal Resistance	T = 100 °C	R100	–	492.2	–	
Deviation of R25		R/R	–1	–	1	%
Power Dissipation		P_D	–	5	–	mW
Power Dissipation Constant			–	1.3	–	mW/K
B-value	B(25/85), tolerance ±1%		–	3430	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Device	Marking	Package	Shipping
NXH270A120M3F5PHG	NXH270A120M3F5PHG	F5 – PIM-60 112x62 (Press-fit PIN) (Pb-Free / Halide Free)	8 Units / Blister Tray

TYPICAL CHARACTERISTICS – T1, T4, T5, T6 (OUTER AND NEUTRAL POINT IGBTs)

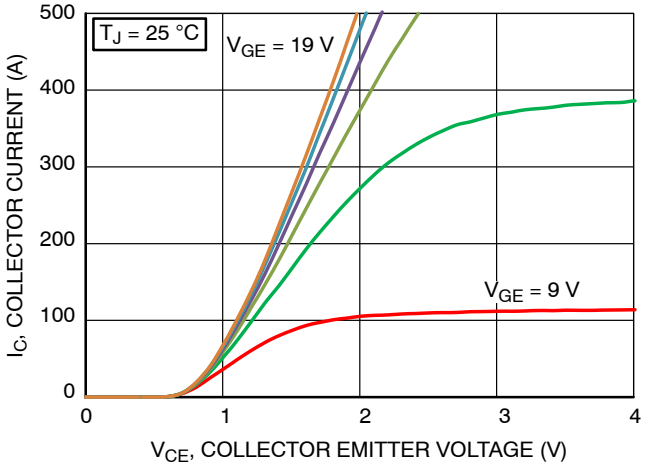


Figure 2. Typical Output Characteristics – IGBT

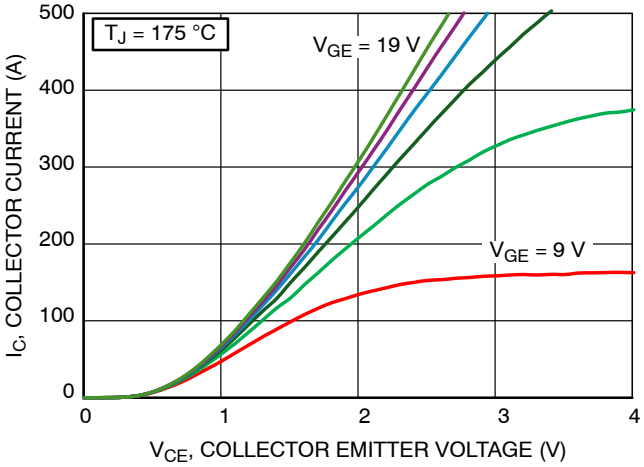


Figure 3. Typical Output Characteristics – IGBT

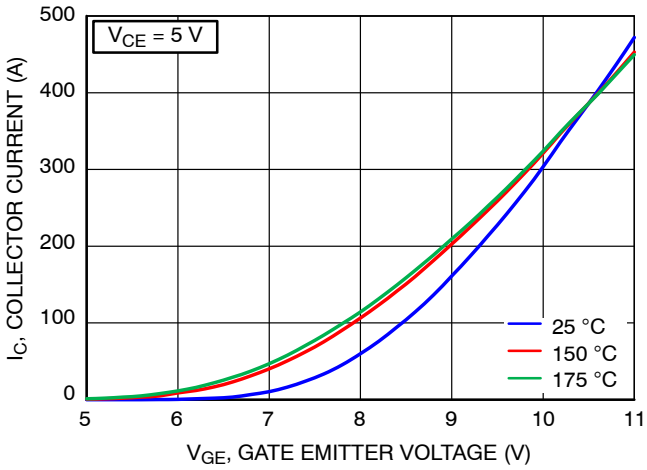


Figure 4. Transfer Characteristics – IGBT

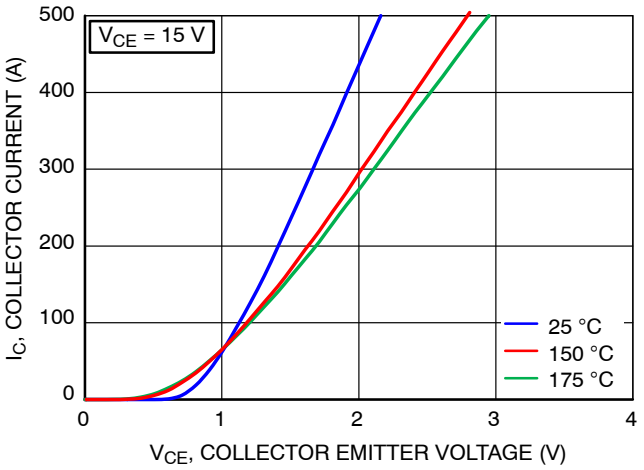


Figure 5. Saturation Voltage Characteristic – IGBT

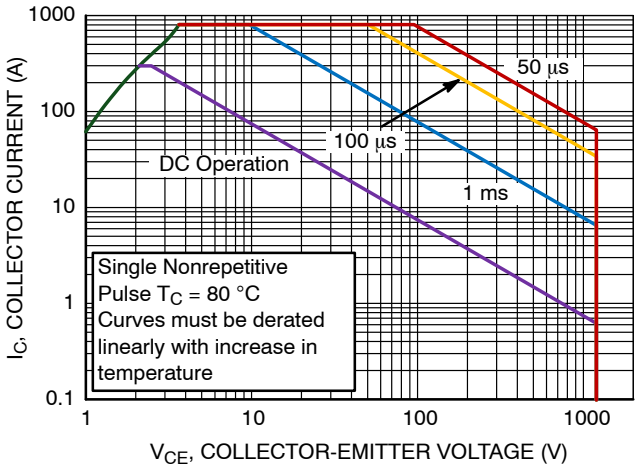


Figure 6. FBSOA

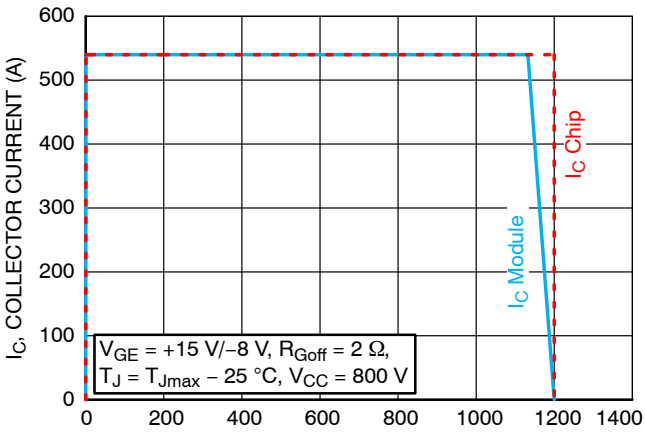


Figure 7. RBSOA

TYPICAL CHARACTERISTICS – T1, T4 , T5, T6 (OUTER AND NEUTRAL POINT IGBTs)

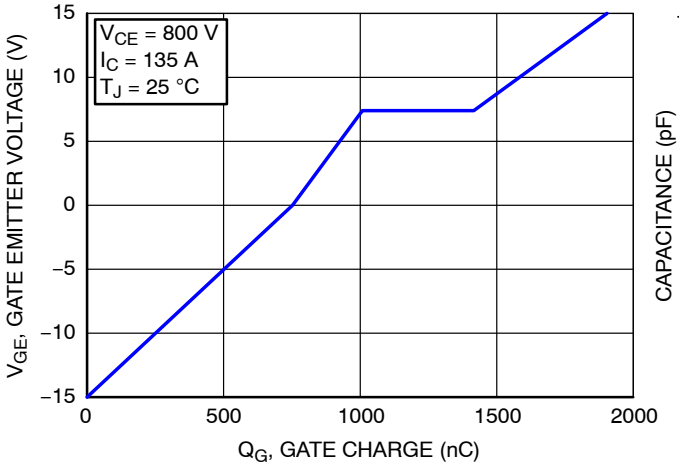


Figure 8. Gate Voltage vs. Gate Charge

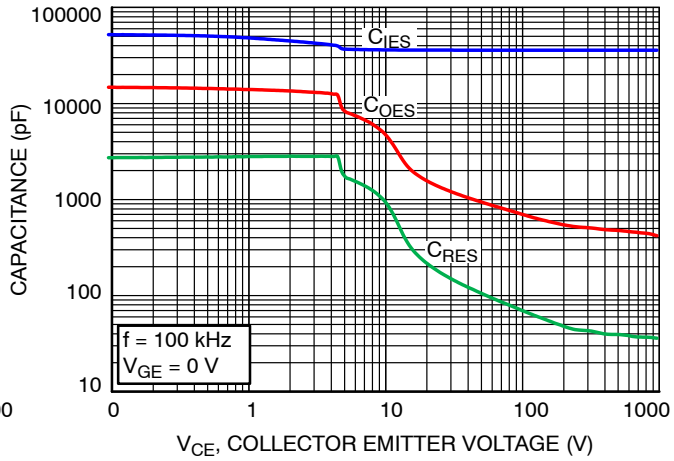


Figure 9. Capacitance Characteristics

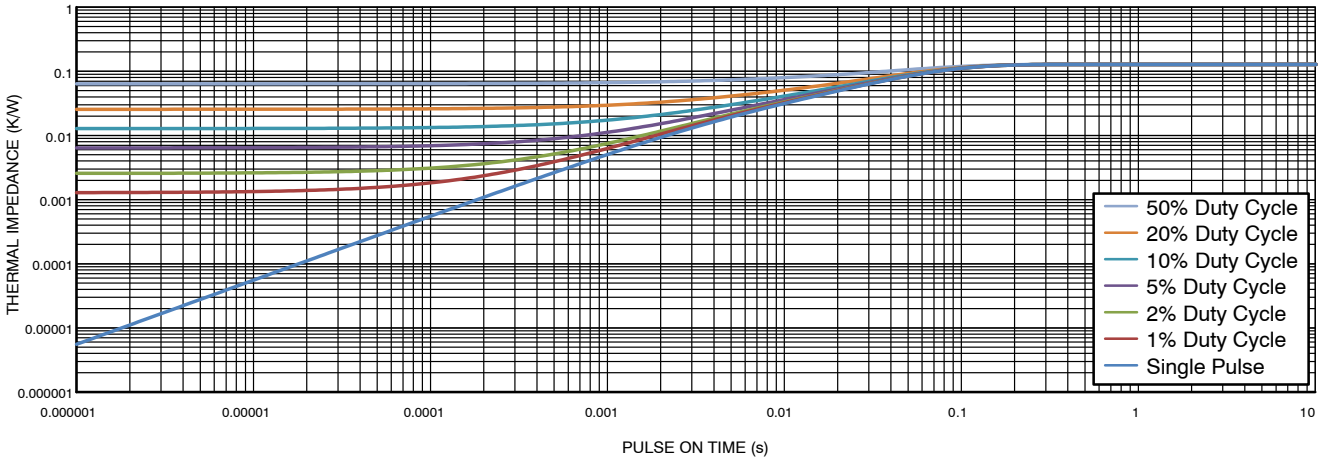


Figure 10. Transient Thermal Impedance (IGBT Z_{thjc})

TYPICAL CHARACTERISTIC – M2, M3 (SIC MOSFET)

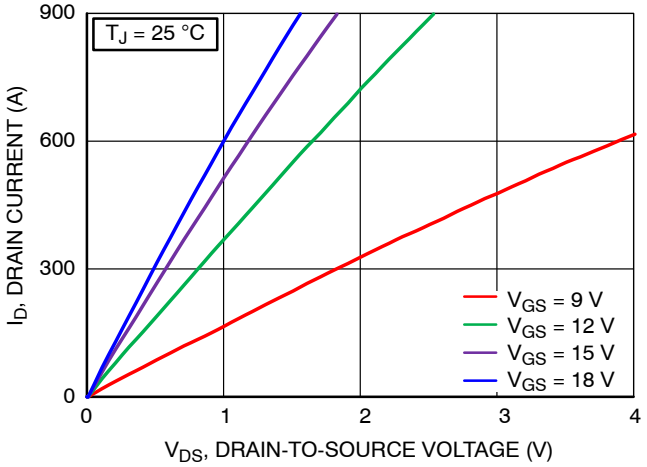


Figure 11. Typical Output Characteristics – SIC MOSFET

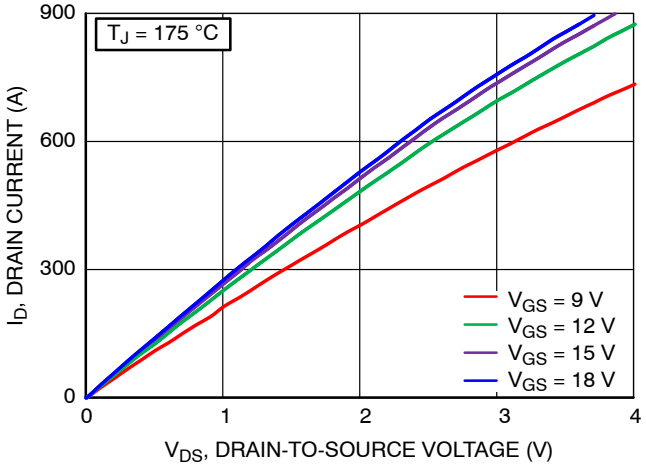


Figure 12. Typical Output Characteristics – SIC MOSFET

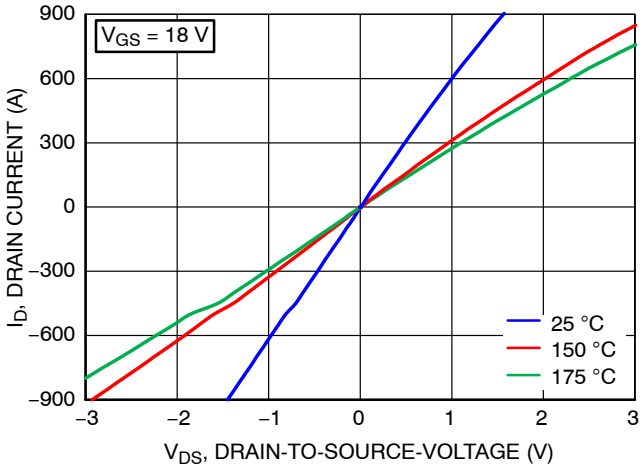


Figure 13. Typical Output Characteristics – SIC MOSFET

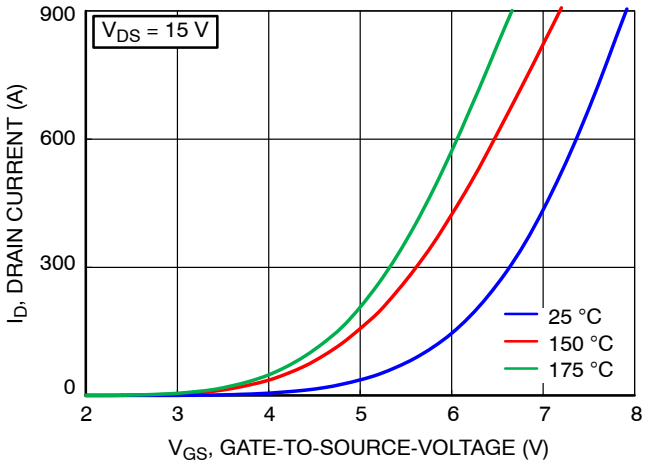


Figure 14. Typical Transfer Characteristics – SIC MOSFET

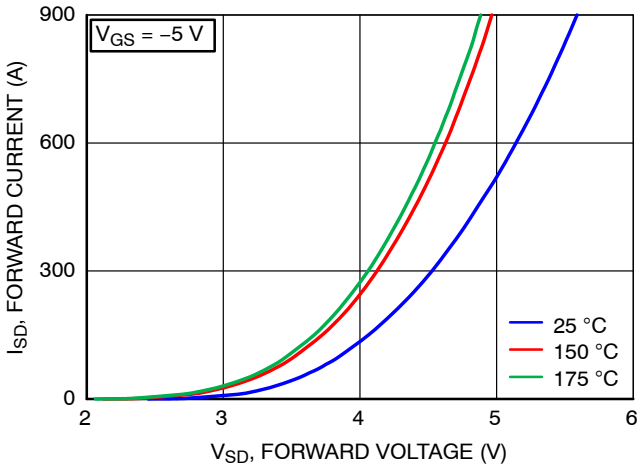


Figure 15. Typical Forward Characteristics – Body Diode

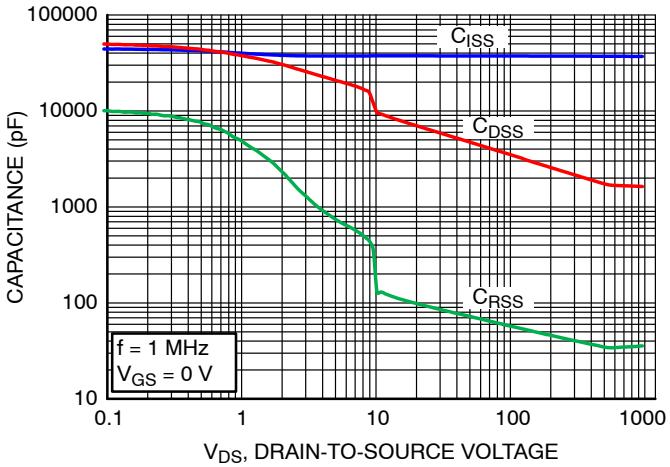


Figure 16. Capacitance Characteristics

TYPICAL CHARACTERISTIC – M2, M3 (SIC MOSFET)

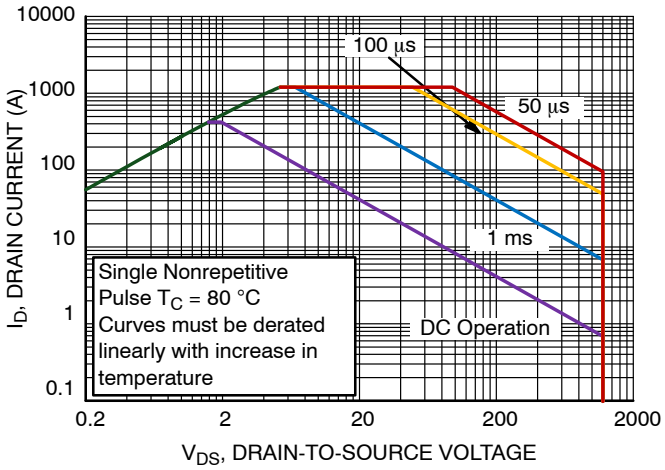


Figure 17. FBSOA

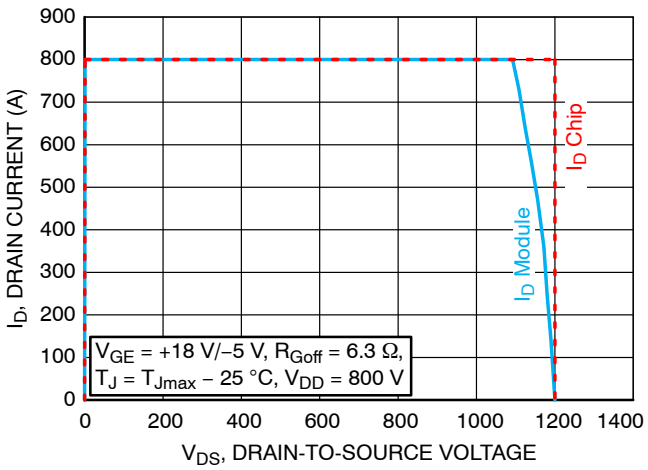


Figure 18. RBSOA

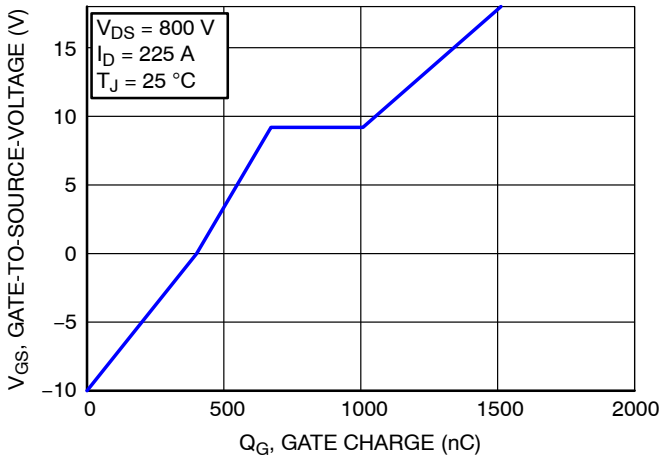


Figure 19. Gate Charge Characteristics

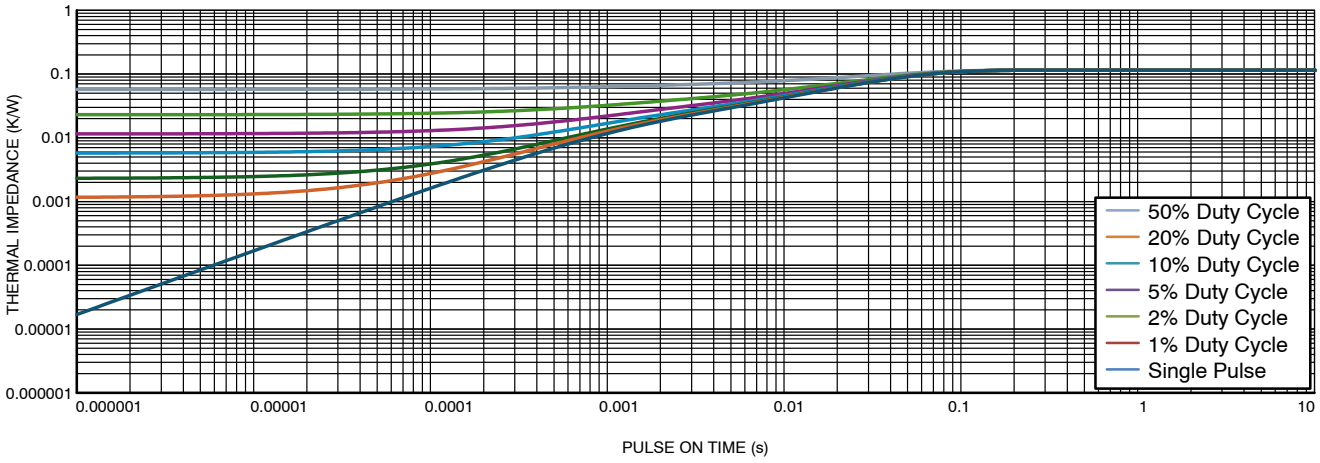


Figure 20. Transient Thermal Impedance (SIC MOSFET)

TYPICAL CHARACTERISTIC – M2, M3 (SIC MOSFET)

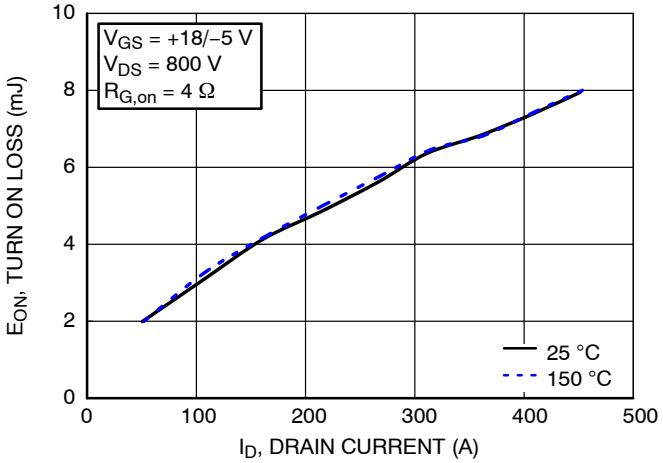


Figure 21. Typical Switching Turn on Loss vs Drain Current

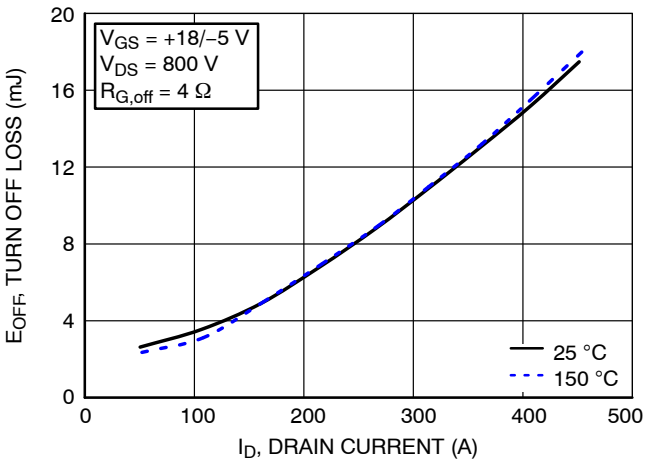


Figure 22. Typical Switching Turn off Loss vs Drain Current

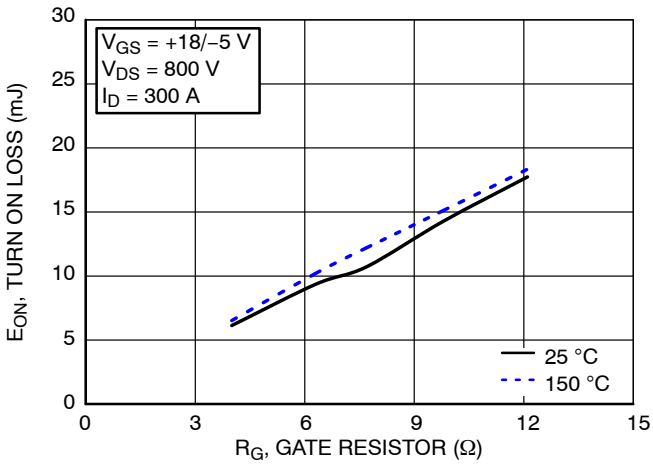


Figure 23. Typical Switching Turn on Loss vs Gate Resistance

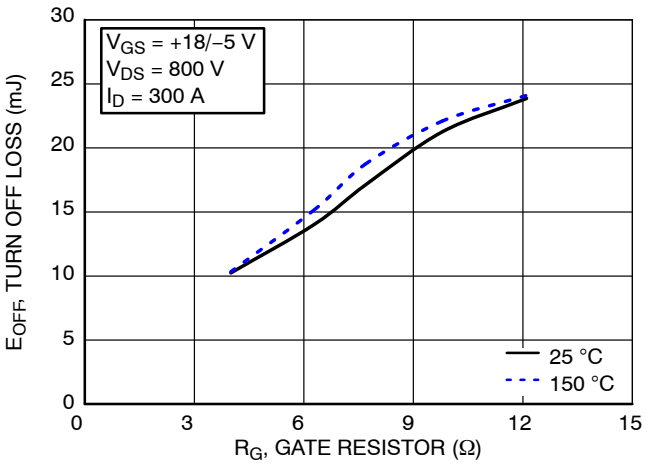


Figure 24. Typical Switching Turn off Loss vs Gate Resistance

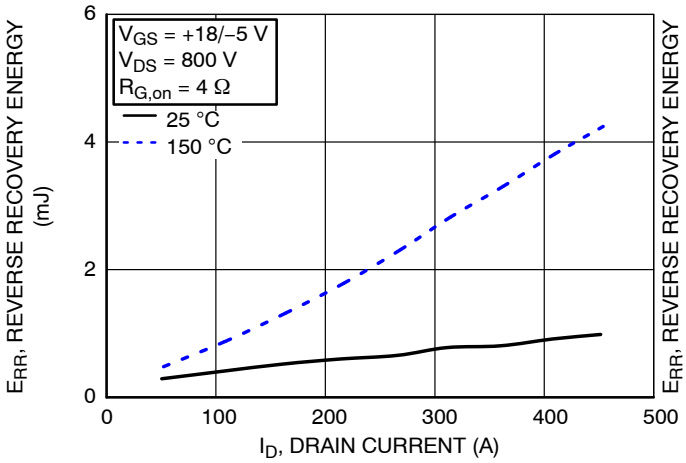


Figure 25. Typical Reverse Recovery Energy vs Drain Current

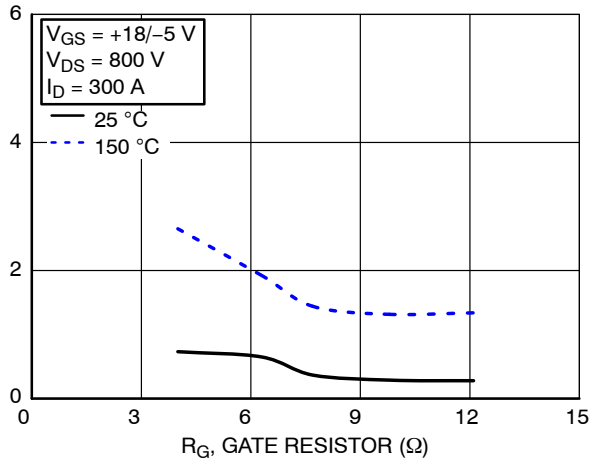


Figure 26. Typical Reverse Recovery Energy vs Gate Resistance

TYPICAL CHARACTERISTIC – M2, M3 (SIC MOSFET)

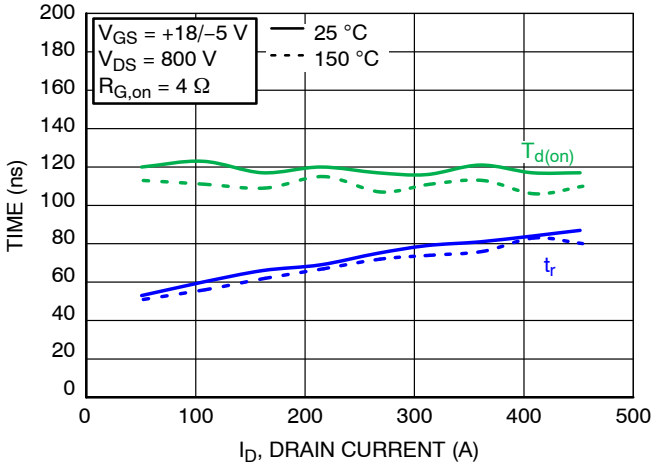


Figure 27. Typical Turn On Switching Time vs Drain Current

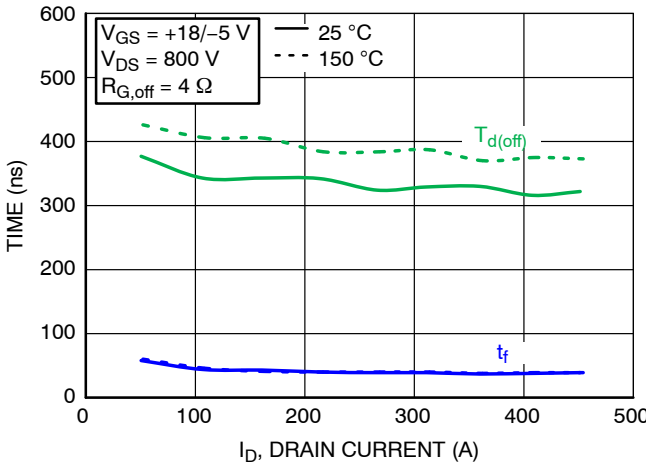


Figure 28. Typical Turn Off Switching Tim vs Drain Current

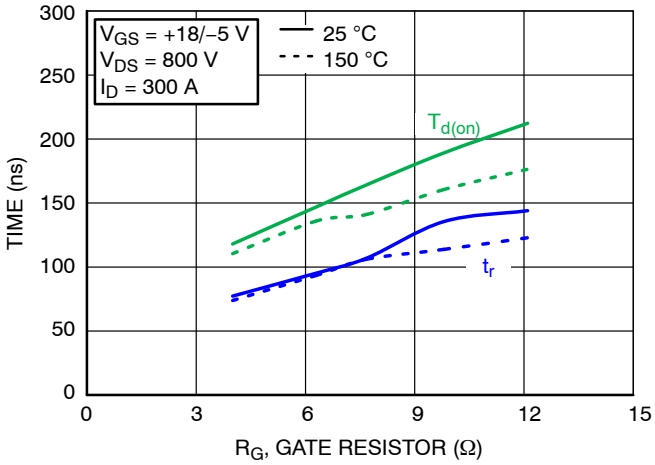


Figure 29. Typical Turn On Switching Time vs Gate Resistance

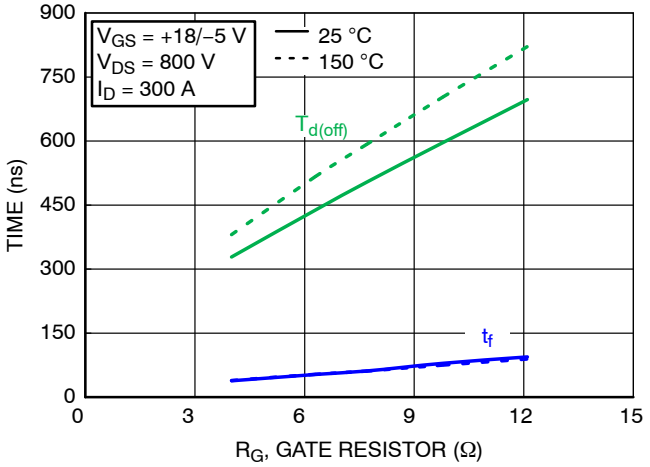


Figure 30. Typical Turn Off Switching Time vs Gate Resistance

TYPICAL CHARACTERISTIC – D1, D4, D5, D6 (OUTER AND NEUTRAL POINT DIODES)

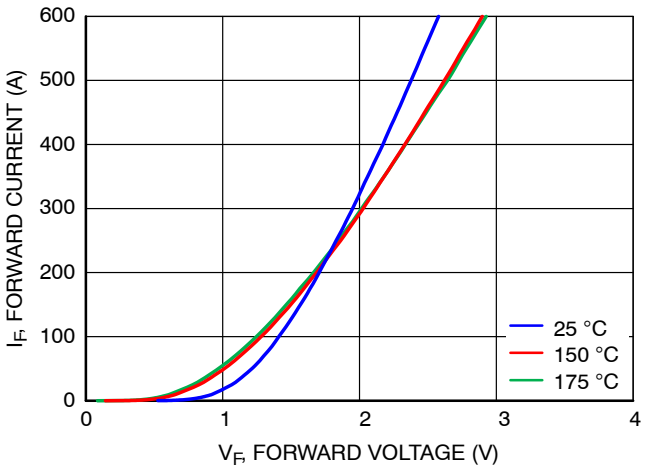


Figure 31. Typical Outer and Neutral Point Diodes Forward Characteristics

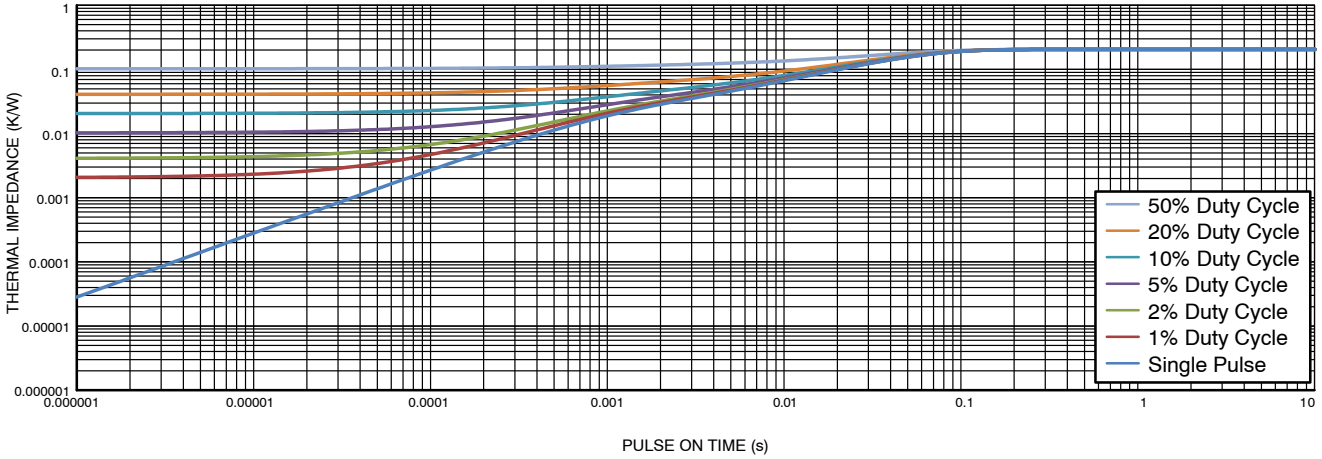


Figure 32. Transient Thermal Impedance (Outer and Neutral Point Diodes)

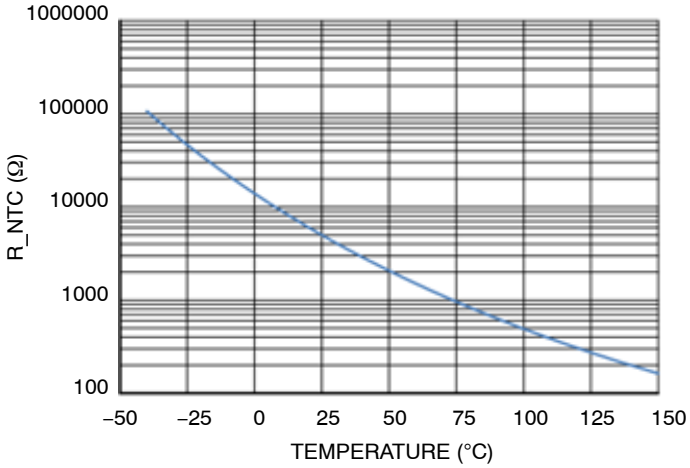
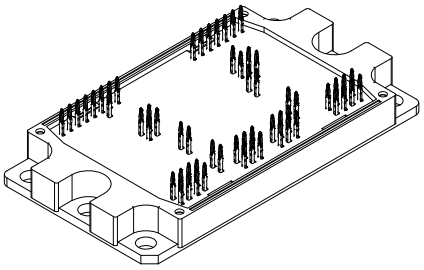


Figure 33. Temperature vs. NTC Value

REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary document release.	5/12/2026
P1	P1: Change the I_D and I_{dpulse} of SiC MOSFET and IC and I_{cpulse} of IGBT and add V_{GS} = 18 V, I_D = 198 mA, T_{vj} = 25 °C, (tested after I_{GSS} @ = +22 V) for $V_{GS(TH)}$ of SiC MOSFET P2: Add Recommended Operating Gate-Source Voltage, V_{GS_OP}, +18/−3~−5 V P3: Change the description from $R_{G,on}$ to R_G in switching test condition P4: Change the unit from μA to mA of I_{DSS} P5: Change the description from Gate-Emitter Threshold Voltage to Gate-Source Threshold Voltage for SiC MOSFET and from 322 A to 299 A for I_C of IGBT P6: Change thermal conductivity from 2.87 W/mK to 3.3 W/mK P7: Change the description from $R_{G,on}$ to $R_{G,off}$ in the plot and remove Gate-Emitter Threshold Voltage for SiC MOSFET P8: Change the description from V_{GS} = 15 V to V_{GS} = V_{DS}	6/17/2026

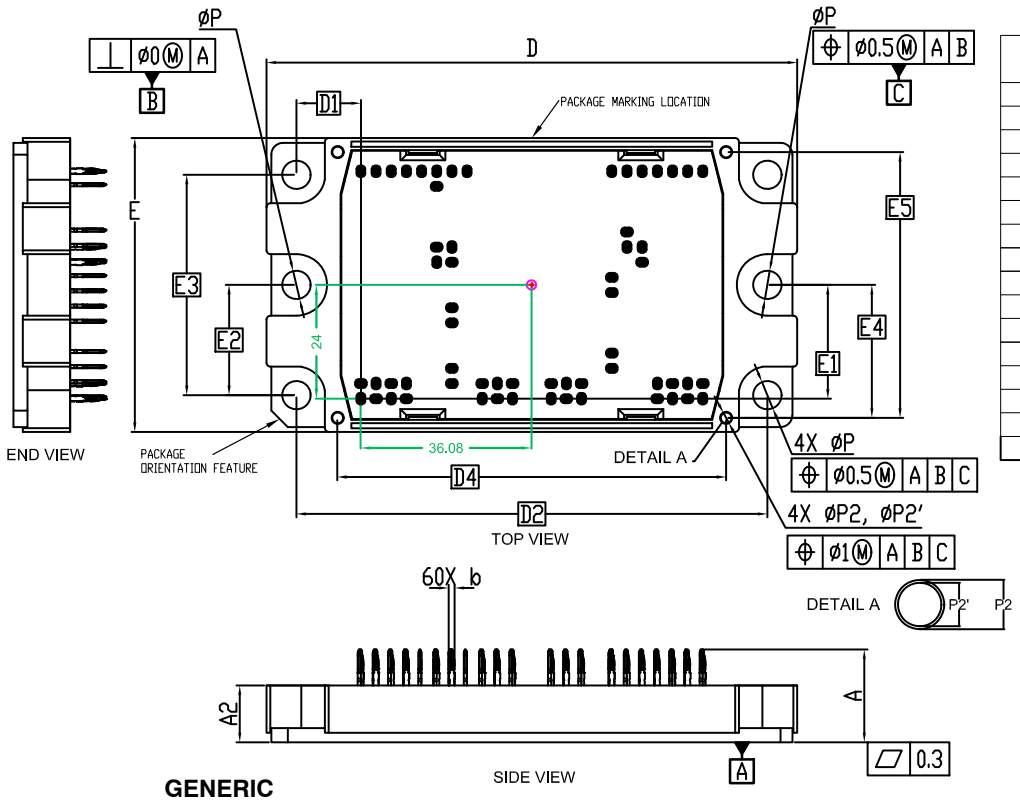
PACKAGE DIMENSIONS



PIM−60 112.00x62.00x12.00
CASE 180DR
ISSUE O

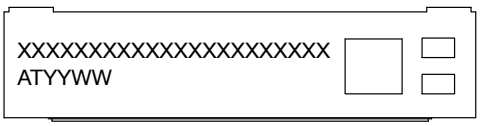
DATE 25 MAR 2026

NOTES:
1. Dimensioning and tolerancing conform to ASME Y14.5 - 2018
2. All dimensions are in millimeters.
3. Pin-grid is 3.2mm.
4. Package marking is located on the side opposite the package orientation feature.
5. The pins are press fit pin (1.2mm)
6. Pin Position tolerance is ±.04mm

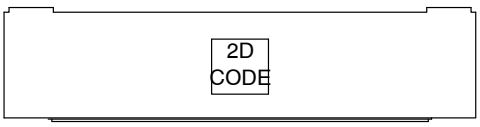


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	19.20	19.60	20.00
A2	11.70	12.00	12.30
b	1.15	1.20	1.25
D	111.60	112.00	112.40
D1	13.62 BSC		
D2	99.40 BSC		
D4	82.00 BSC		
E	61.60	62.00	62.40
E1	24.00 BSC		
E2	23.25 BSC		
E3	46.50 BSC		
E4	28.05 BSC		
E5	56.10 BSC		
P	5.90	6.00	6.10
P2	2.50	2.60	2.70
P2′	2.30	2.40	2.50

GENERIC MARKING DIAGRAM*



FRONTSIDE MARKING



BACKSIDE MARKING

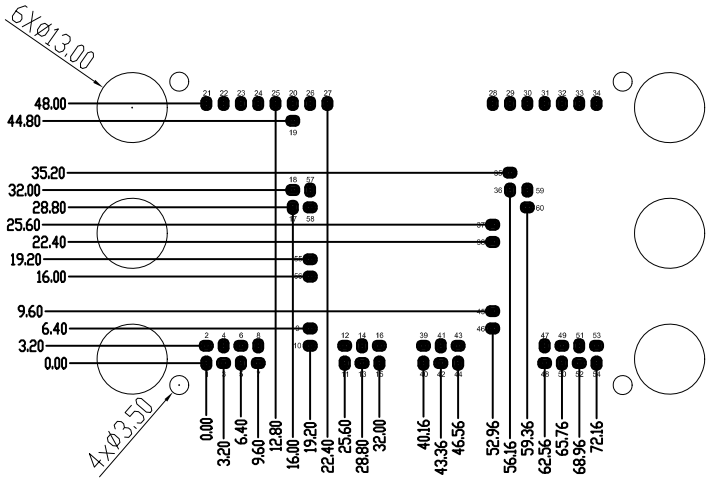
XXXXX = Specific Device Code
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

PACKAGE DIMENSIONS

PIM−60 112.00x62.00x12.00
CASE 180DR
ISSUE O

DATE 25 MAR 2026



RECOMMENDED
MOUNTING PATTERN

* For additional Information on our Pb−Free strategy and soldering details, please download the Onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTE 2:

Pin table								
Pin	X	Y	Pin	X	Y	Pin	X	Y
1	0	0	23	6.4	48	45	52.96	9.6
2	0	3.2	24	9.6	48	46	52.96	6.4
3	3.2	0	25	12.8	48	47	62.56	3.2
4	3.2	3.2	26	19.2	48	48	62.56	0
5	6.4	0	27	22.4	48	49	65.76	3.2
6	6.4	3.2	28	52.96	48	50	65.76	0
7	9.6	0	29	56.16	48	51	68.96	3.2
8	9.6	3.2	30	59.36	48	52	68.96	0
9	19.2	6.4	31	62.56	48	53	72.16	3.2
10	19.2	3.2	32	65.76	48	54	72.16	0
11	25.6	0	33	68.96	48	55	19.2	19.2
12	25.6	3.2	34	72.16	48	56	19.2	16
13	28.8	0	35	56.16	35.2	57	19.2	32
14	28.8	3.2	36	56.16	32	58	19.2	28.8
15	32	0	37	52.96	25.6	59	59.36	32
16	32	3.2	38	52.96	22.4	60	59.36	28.8
17	16	28.8	39	40.16	3.2			
18	16	32	40	40.16	0			
19	16	44.8	41	43.36	3.2			
20	16	48	42	43.36	0			
21	0	48	43	46.56	3.2			
22	3.2	48	44	46.56	0			

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