

PNP Low-Saturation Transistor

NZT660, NZT660A

Description

These devices are designed with high-current gain and low saturation voltage with collector currents up to 3 A continuous.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted.) (Notes 1, 2)

Symbol	Parameter	Value	Unit
V _{CEO}	Collector-Emitter Voltage	-60	V
V _{CBO}	Collector-Base Voltage NZT660 NZT660A	-80 -60	V
V _{EBO}	Emitter-Base Voltage	-5	V
I _C	Collector Current – Continuous	-3	A
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

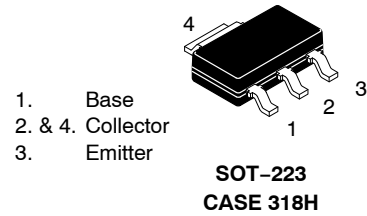
- These ratings are based on a maximum junction temperature of 150°C.
- These are steady limits. onsemi should be consulted on application involving pulsed or low-duty-cycle operations.

THERMAL CHARACTERISTICS

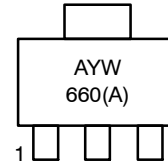
(T_A = 25°C unless otherwise noted.) (Note 3)

Symbol	Parameter	Max	Unit
P _D	Total Device Dissipation	2	W
R _{θJA}	Thermal Resistance, Junction to Ambient	62.5	°C/W

- PCB size: FR-4, 76 mm × 114 mm × 1.57 mm (3.0 inch × 4.5 inch × 0.062 inch) with minimum land pattern size.



MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
660(A) = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NZT660	SOT-223 (Pb-Free)	4,000 / Tape & Reel
NZT660A	SOT-223 (Pb-Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NZT660, NZT660A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Max	Unit	
BV _{CEO}	Collector-Emitter Breakdown Voltage	I _C = -10 mA	-60	-	V	
BV _{CBO}	Collector-Base Breakdown Voltage	I _C = -100 μA	NZT660	-80	-	V
			NZT660A	-60	-	
BV _{EBO}	Emitter-Base Breakdown Voltage	I _E = -100 μA	-5	-	V	
I _{CBO}	Collector-Base Cut-Off Current	V _{CB} = -30 V	-	-100	nA	
		V _{CB} = -30 V, T _A = 100°C	-	-10	μA	
I _{EBO}	Emitter-Base Cut-Off Current	V _{EB} = -4 V	-	-100	nA	
h _{FE}	DC Current Gain (Note 4)	I _C = -100 mA, V _{CE} = -2 V	70	-		
		I _C = -500 mA, V _{CE} = -2 V	NZT660	100		300
			NZT660A	250		550
		I _C = -1 A, V _{CE} = -2 V	80	-		
V _{CE(sat)}	Collector-Emitter Saturation Voltage (Note 4)	I _C = -1 A, I _B = -100 mV	-	-300	mV	
		I _C = -3 A, I _B = -300 mV	NZT660	-		-550
			NZT660A	-		-500
V _{BE(sat)}	Base-Emitter Saturation Voltage (Note 4)	I _C = -1 A, I _B = -100 mV	-	-1.25	V	
V _{BE(on)}	Base-Emitter On Voltage (Note 4)	I _C = -1 A, V _{CE} = -2 V	-	-1	V	
C _{ob}	Output Capacitance	V _{CB} = -10 V, I _E = 0, f = 1 MHz	-	45	pF	
f _T	Transition Frequency	I _C = -100 mA, V _{CE} = -5 V, f = 100 MHz	75	-	MHz	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2.0%.

TYPICAL PERFORMANCE CHARACTERISTICS

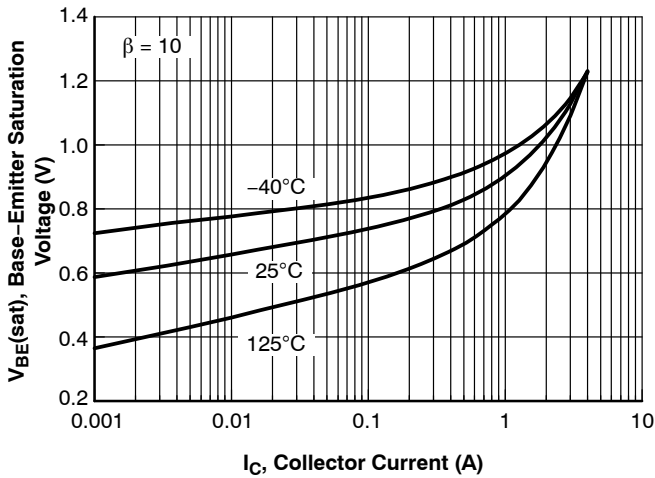


Figure 1. Base-Emitter Saturation Voltage vs. Collector Current

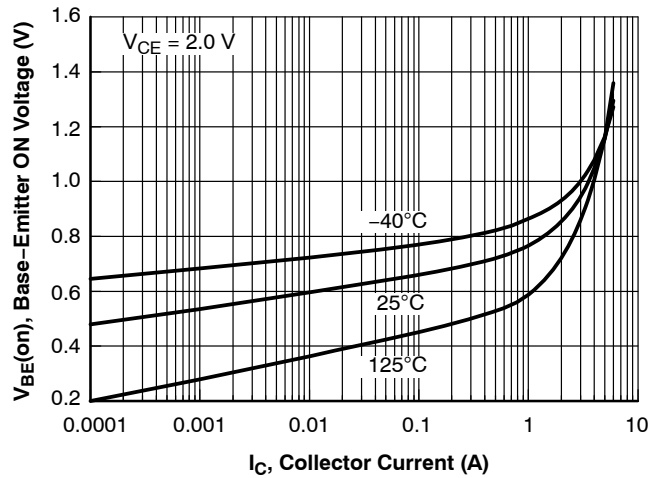


Figure 2. Base-Emitter On Voltage vs. Collector Current

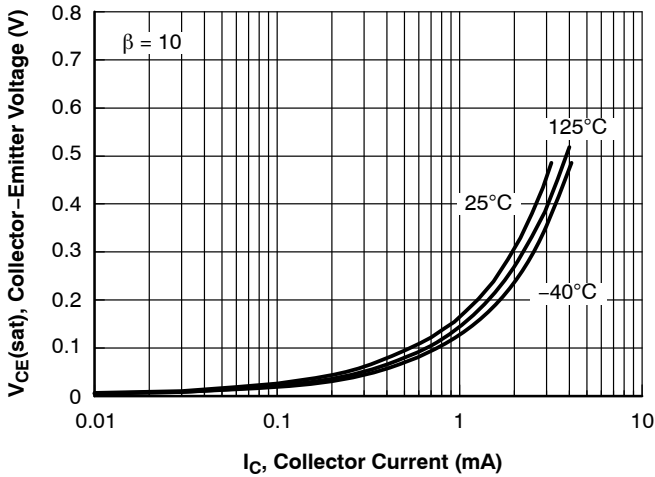


Figure 3. Collector-Emitter Saturation Voltage vs. Collector Current

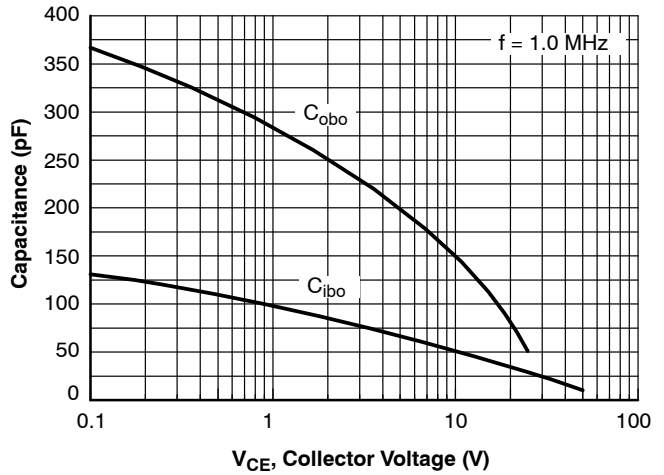


Figure 4. Input/Output Capacitance vs. Reverse Bias Voltage

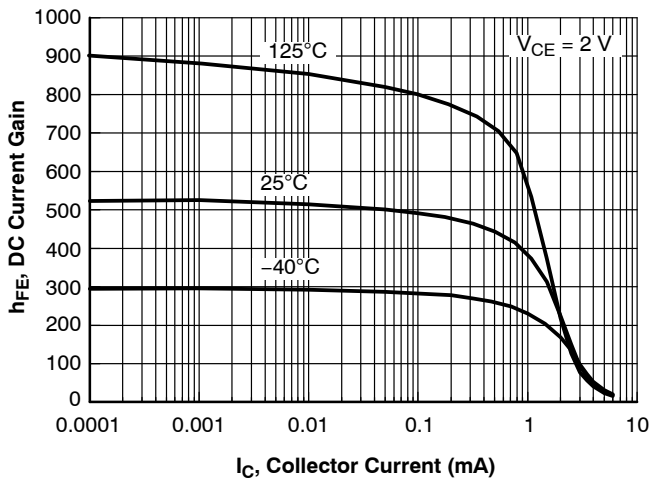
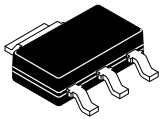


Figure 5. Current Gain vs. Collector Current

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

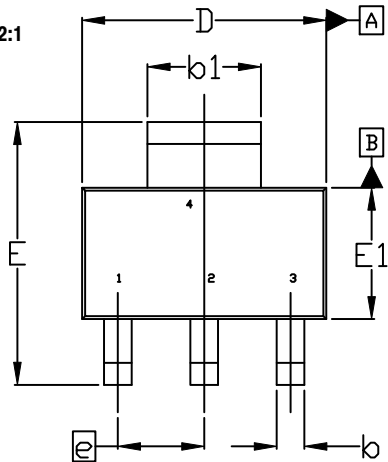
ON Semiconductor®



SOT-223
CASE 318H
ISSUE B

DATE 13 MAY 2020

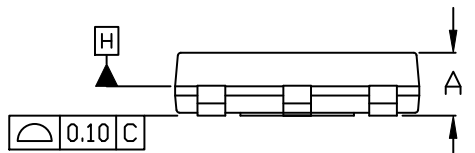
SCALE 2:1



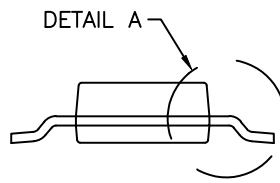
TOP VIEW

$\text{Ø} 0.10 \text{ (M) C A B}$

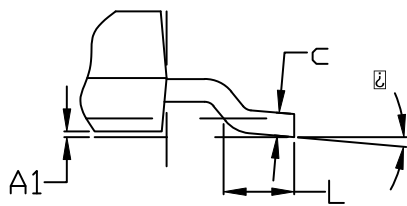
NOTE 7



SIDE VIEW



END VIEW

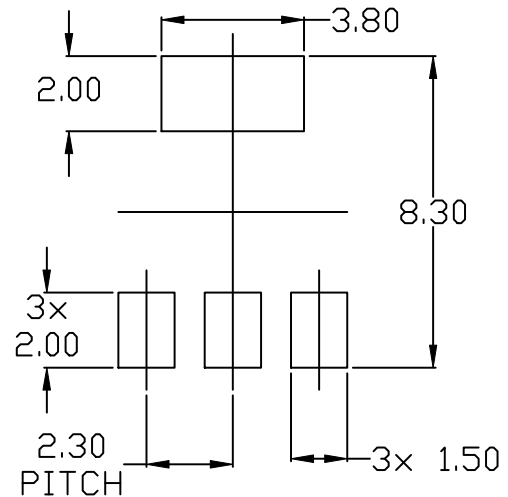


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

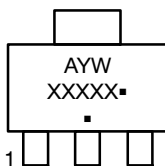
DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
Ø	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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