

MOSFET – Power, N-Channel

60 V, 50 A, 22 mΩ

RFP50N06

These N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developed type TA49018.

Features

- 50 A, 60 V
- $r_{DS(ON)} = 0.022 \Omega$
- Temperature Compensating PSpice™ Model
- Peak Current vs. Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- This Device is Pb-Free and is RoHS Compliant

Specifications

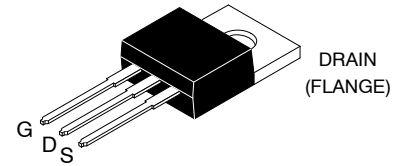
ABSOLUTE MAXIMUM RATINGS

($T_C = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter		Rating	Unit
V_{DSS}	Drain to Source Voltage (Note 1)		60	V
V_{DGR}	Drain to Gate Voltage ($R_{GS} = 20 \text{ k}\Omega$) (Note 1)		60	V
V_{GS}	Gate to Source Voltage		± 20	V
I_D	Drain Current	Continuous (Figure 2)	50	A
		Pulsed (Figure 5)		
E_{AS}	Pulsed Avalanche Rating		(Figure 6)	
P_D	Power Dissipation		131	W
	Linear Derating Factor		0.877	
T_J, T_{STG}	Operating and Storage Temperature		-55 to 175	$^\circ\text{C}$
T_L	Maximum Temperature for Soldering Leads at 0.063 inch (1.6 mm) from Case for 10 s		300	$^\circ\text{C}$
T_{pkg}	Maximum Temperature for Soldering Package Body for 10 s, see Techbrief 334		260	$^\circ\text{C}$

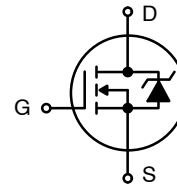
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $T_J = 25^\circ\text{C}$ to 150°C

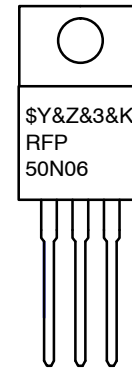


TO-220-3LD
CASE 340AT

SYMBOL



MARKING DIAGRAM



- \$Y = onsemi Logo
- &Z = Assembly Plant Code
- &3 = Date Code (Year & Week)
- &K = Lot
- RFP50N06 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
RFP50N06	TO-220-3LD (Pb-Free)	800 units / Tube

RFP50N06

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250 μA, V _{GS} = 0 V (Figure 11)	60	–	–	V	
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA (Figure 10)	2	–	4	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	T _C = 25°C	–	–	1	μA
			T _C = 150°C	–	–	50	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V	–	–	±100	nA	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 50 A, V _{GS} = 10 V (Figure 9)	–	–	0.022	Ω	
Turn-On Time	t _{ON}	V _{DD} = 30 V, I _D = 50 A R _L = 0.6 Ω, V _{GS} = 10 V R _{GS} = 3.6 Ω (Figure 13)	–	–	95	ns	
Turn-On Delay Time	t _{d(ON)}		–	12	–	ns	
Rise Time	t _r		–	55	–	ns	
Turn-Off Delay Time	t _{d(OFF)}		–	37	–	ns	
Fall Time	t _f		–	13	–	ns	
Turn-Off Time	t _{OFF}		–	–	75	ns	
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0 to 20 V	–	125	150	nC	
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0 to 10 V					
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0 to 2 V					
		V _{DD} = 48 V, I _D = 50 A, R _L = 0.96 Ω I _{g(REF)} = 1.45 mA (Figure 13)					
Input Capacitance	C _{ISS}	V _{DS} = 25 V, V _{GS} = 0 V	–	2020	–	pF	
Output Capacitance	C _{OSS}	f = 1 MHz	–	600	–	pF	
Reverse Transfer Capacitance	C _{RSS}	(Figure 12)	–	200	–	pF	
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)	–	–	1.14	°C/W	
Thermal Resistance Junction to Ambient	R _{θJA}	TO-220	–	–	62	°C/W	

SOURCE TO DRAIN DIODE CHARACTERISTICS

Source to Drain Diode Voltage	V _{SD}	I _{SD} = 50 A	–	–	1.5	V
Output Capacitance	t _{rr}	I _{SD} = 50 A, dI _{SD} /dt = 100 A/μs	–	–	125	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified)

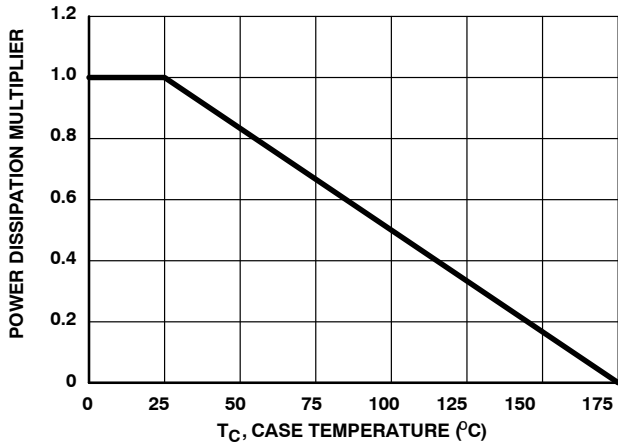


Figure 1. Normalized Power Dissipation vs. Case Temperature

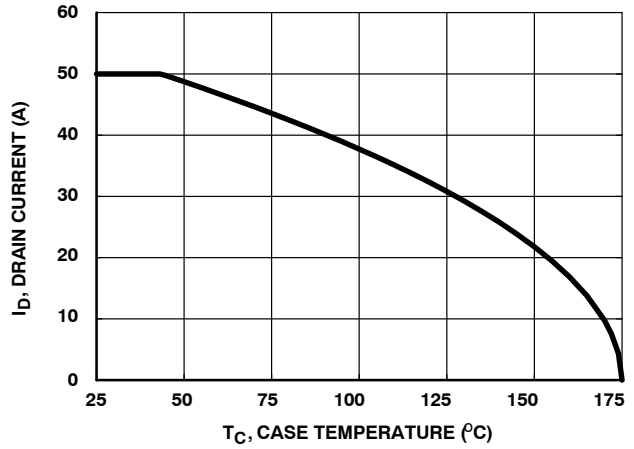


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

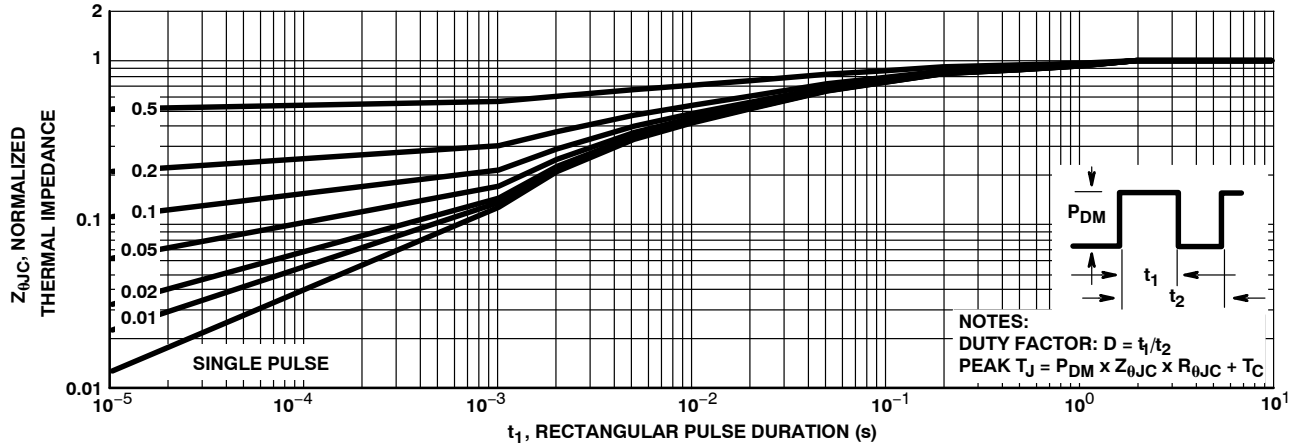


Figure 3. Normalized Maximum Transient Thermal Impedance

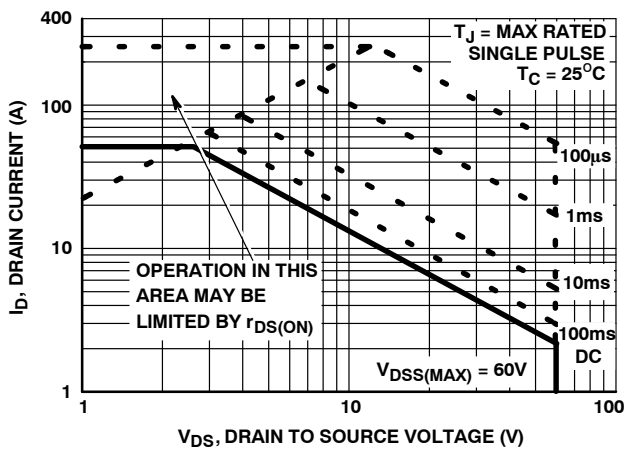


Figure 4. Forward Bias Safe Operating Area

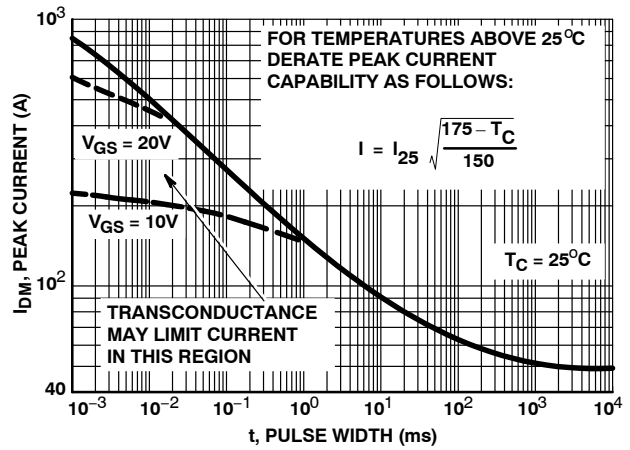


Figure 5. Peak Current Capability

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified) (continued)

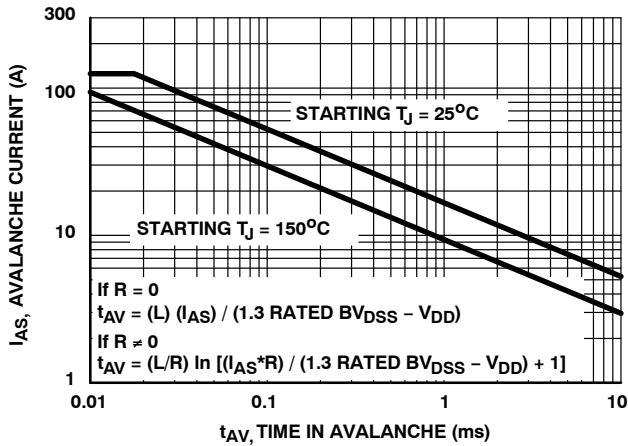


Figure 6. Unclamped Inductive Switching Capability

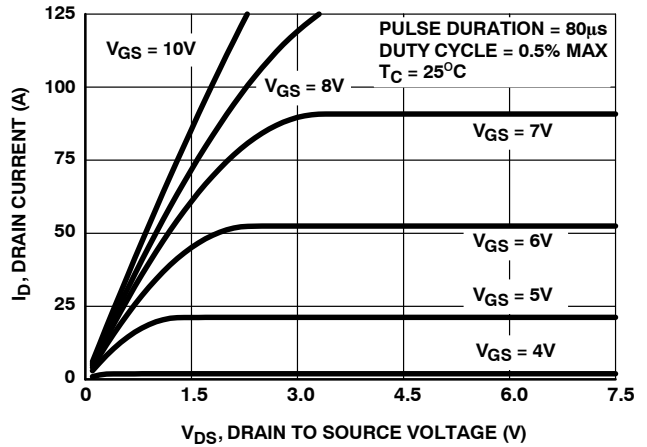


Figure 7. Saturation Characteristics

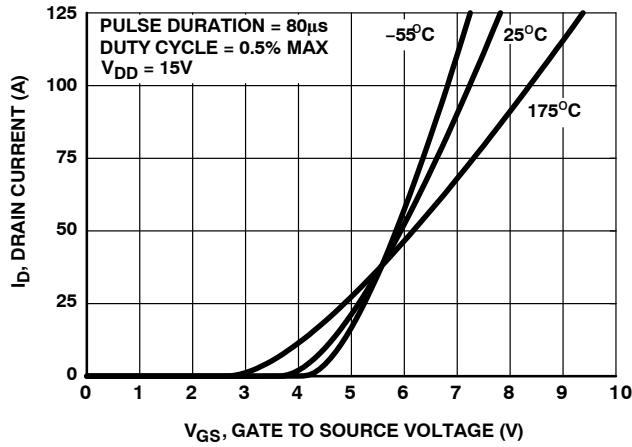


Figure 8. Transfer Characteristics

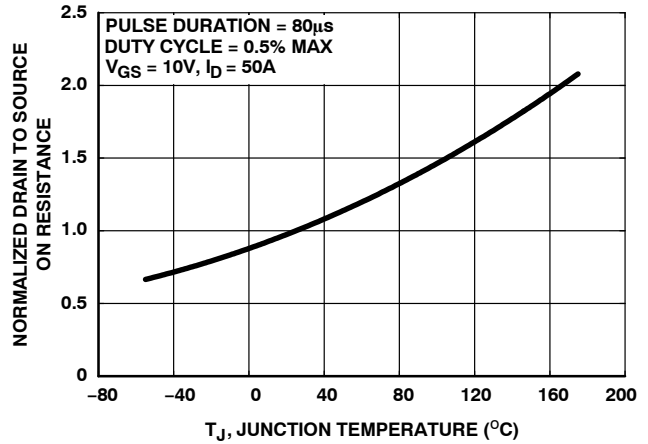


Figure 9. Normalized Drain to Source On Resistance vs. Junction Temperature

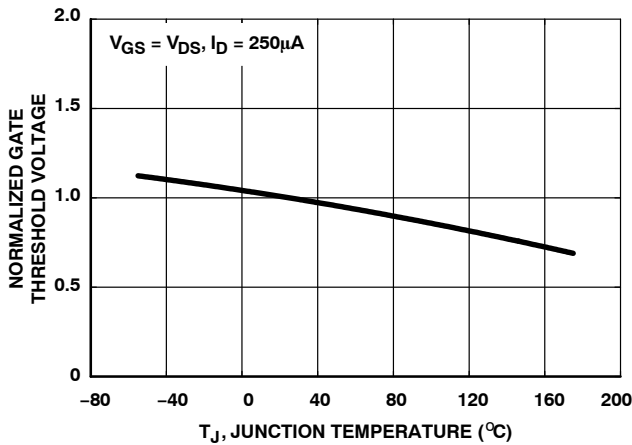


Figure 10. Normalized Gate Threshold Voltage vs. Junction Temperature

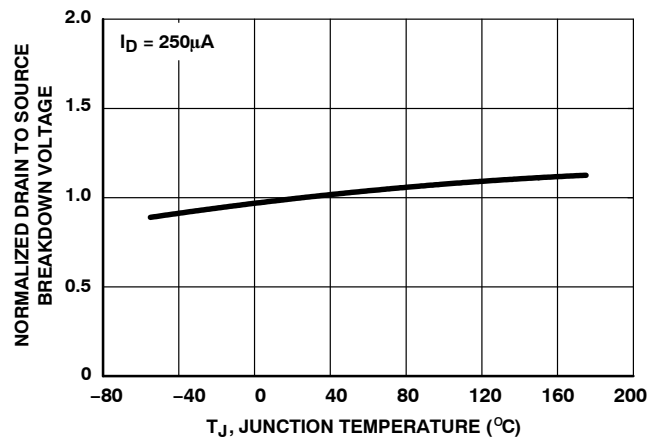


Figure 11. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified) (continued)

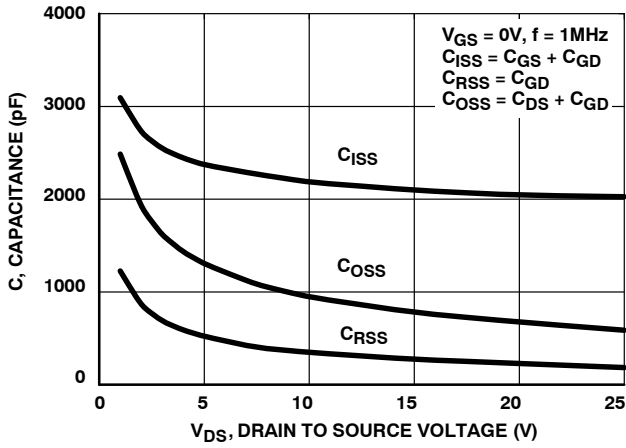


Figure 12. Capacitance vs. Drain to Source Voltage

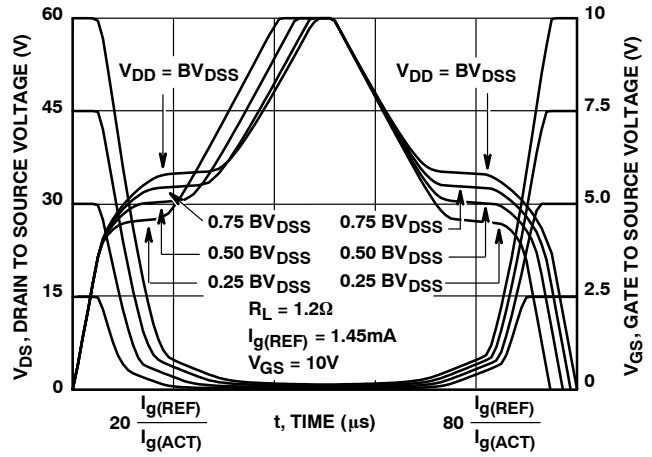


Figure 13. Normalized Switching Waveforms for Constant Gate Current

TEST CIRCUITS AND WAVEFORMS

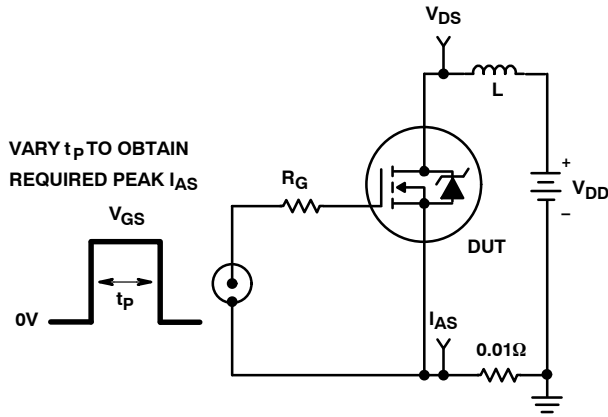


Figure 14. Unclamped Energy Test Circuit

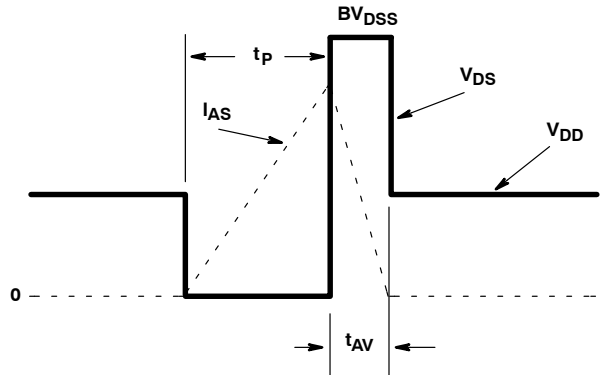


Figure 15. Unclamped Energy Waveforms

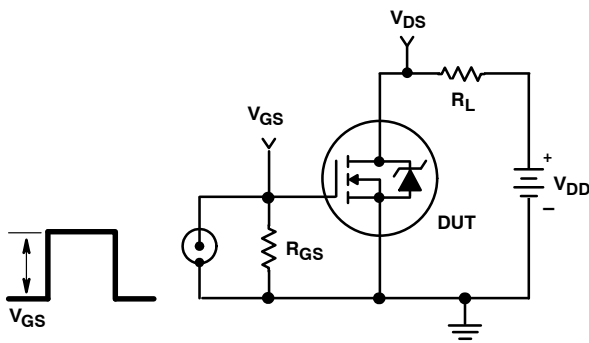


Figure 16. Switching Time Test Circuit

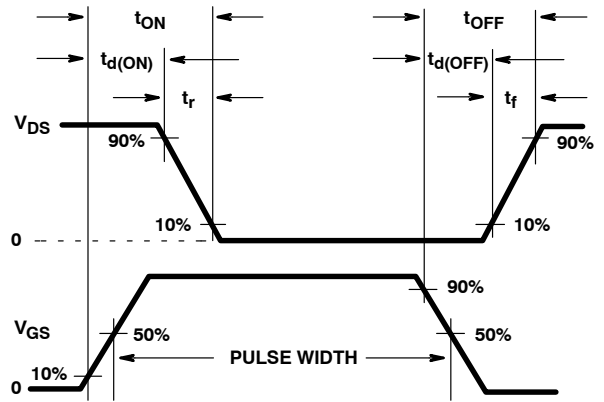


Figure 17. Switching Waveforms

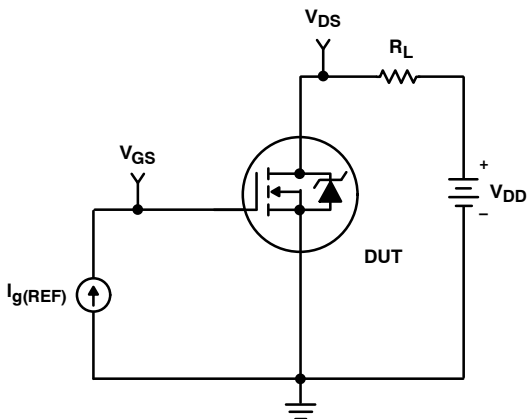


Figure 18. Gate Charge Test Circuit

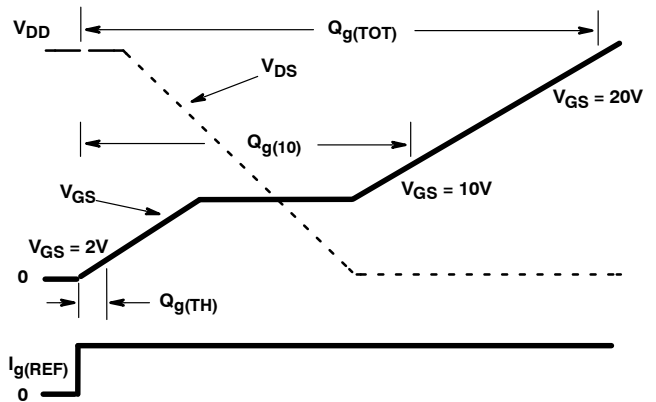


Figure 19. Gate Charge Waveforms

RFP50N06

PSPICE ELECTRICAL MODEL

.SUBCKT RFP50N06213

REV 2/22/93

*NOM TEMP = 25°C

CA 12 8 3.68e-9
 CB 15 14 3.625e-9
 CIN 6 8 1.98e-9

DBODY 7 5 DBDMOD
 DBREAK 5 11 DBKMOD
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 64.59
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 6 8 1
 EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
 LGATE 1 9 5.65e-9
 LSOURCE 3 7 4.13e-9

MOS1 16 6 8 8 MOSMOD M=0.99
 MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
 RDRAIN 5 16 RDSMOD 1e-4
 RGATE 9 20 0.690
 RIN 6 8 1e9
 RSOURCE 8 7 RDSMOD 12e-3
 RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

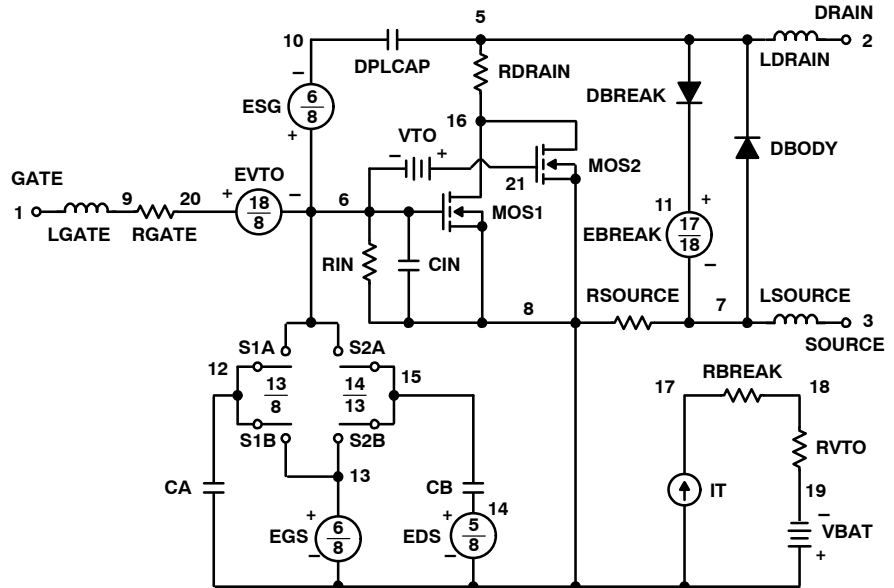
VBAT 8 19 DC 1
 VTO 21 6 0.678

.MODEL DBDMOD D (IS=9.85e-13 RS=4.91e-3 TRS1=2.07e-3 TRS2=2.51e-7 CJO=2.05e-9 TT=4.33e-8)
 .MODEL DBKMOD D (RS=1.98e-1 TRS1=2.35e-4 TRS2=-3.83e-6)
 .MODEL DPLCAPMOD D (CJO=1.42e-9 IS=1e-30 N=10)
 .MODEL MOSMOD NMOS (VTO=3.65 KP=35 IS=1e-30 N=10 TOX=1 L=1u W=1u)
 .MODEL RBKMOD RES (TC1=1.23e-3 TC2=-2.34e-7)
 .MODEL RDSMOD RES (TC1=5.01e-3 TC2=1.49e-5)
 .MODEL RVTOMOD RES (TC1=-5.03e-3 TC2=-5.16e-6)
 .MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.75 VOFF=-2.5)
 .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.5 VOFF=-6.75)
 .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.7 VOFF=2.3)
 .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.3 VOFF=-2.7)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; authors, William J. Hepp and C. Frank Wheatley.

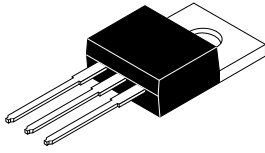
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

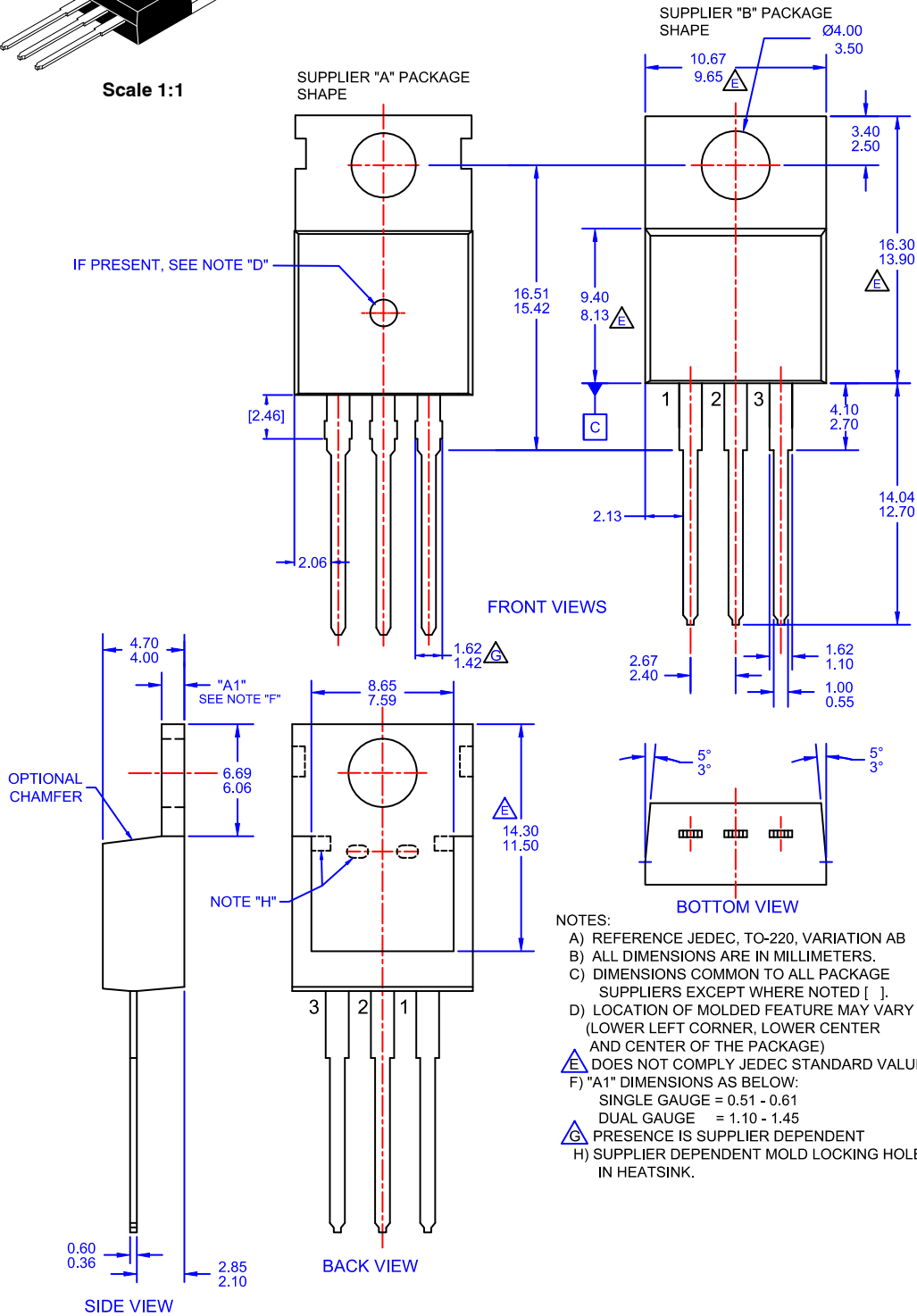
ON Semiconductor®



Scale 1:1

TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017



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