4-Bit Dual-Supply Level Translator

Product Preview

T30LMXT3V4T244, T30LMXT3V4T240, T30LMXT3V4T3144

The T30LMXT3V4T244 / T30LMXT3V4T240 / T30LMXT3V4T3144 are 4−bit configurable dual−supply level translators with 3−state outputs. The A− and B− ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both supply rails are configurable from 0.9 V to 3.6 V allowing universal voltage level translation between the A− to B− ports.

The T30LMXT3V4T244 is a 4−bit level translator that allows non−inverting translations from A to B ports. The T30LMXT3V4T240 is a 4−bit level translator that allows inverting translations from A to B ports. The T30LMXT3V4T3144 is a 4−bit level translator that allows 3−bits of non−inverting translations from A to B ports and 1 bit of non−inverting translation from B to A.

The output enable pin ($\overline{OE}$), when High, disables all the output ports by putting them in 3−state. The $\overline{OE}$ pin is designed to track V_{CCA}.

Features

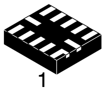
- Wide V_{CCA} and V_{CCB} Operating Range: 0.9 V to 3.6 V
- Balanced Output Drive: ±24 mA @ 3.0 V
- High−Speed w/ Balanced Propagation Delay: 2.8 ns max at 3.0 to 3.6 V
- Input/Output Pins OVT to 3.6 V
- Non−preferential V_{CC} Sequencing
- Outputs at 3−State until Active V_{CC} is Reached
- Partial Power−Off Protection
- Outputs Switch to 3−State with either V_{CC} at GND
- Typical Max Data Rates:
    - 400 Mbps (≥1.8−V to 3.3−V Translation)
    - 200 Mbps (≥1.1−V to [1.8−V, 2.5−V, 3.3−V] Translation)
    - 150 Mbps (≥1.1−V to 1.5−V Translation)
    - 100 Mbps (≥1.1−V to 1.2−V Translation)
- Small Pb−Free Packaging: TSSOP−14, SOIC−14, UQFN12
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

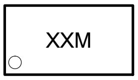
- Mobile Phones, PDAs, Other Portable Devices
- Automotive
- Industrial

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

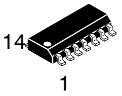
MARKING DIAGRAMS



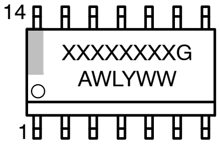
UQFN12
MU SUFFIX
CASE 523AE

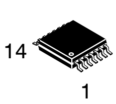


XX = Specific Device Code
M = Date Code

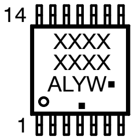


SOIC−14
D SUFFIX
CASE 751A





TSSOP−14
DT SUFFIX
CASE 948G

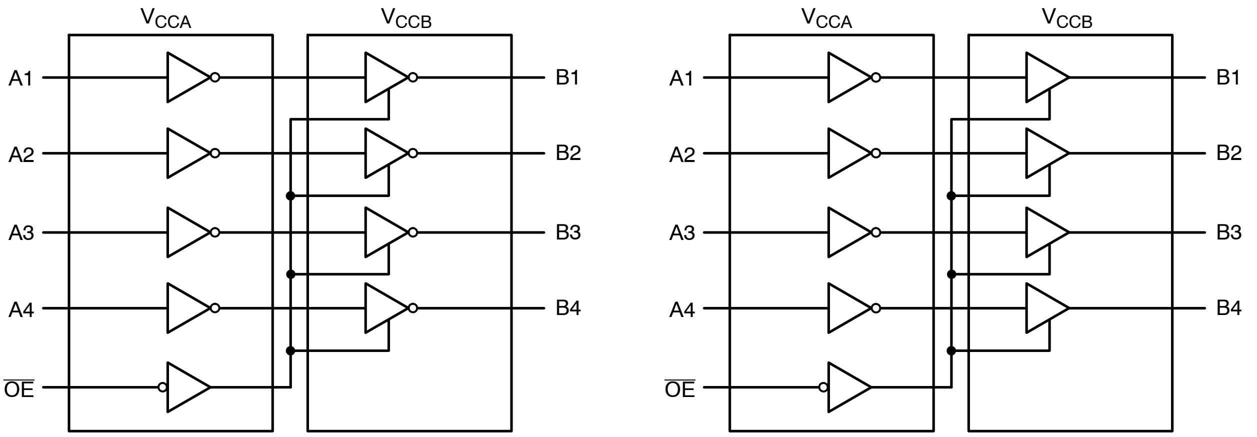


A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

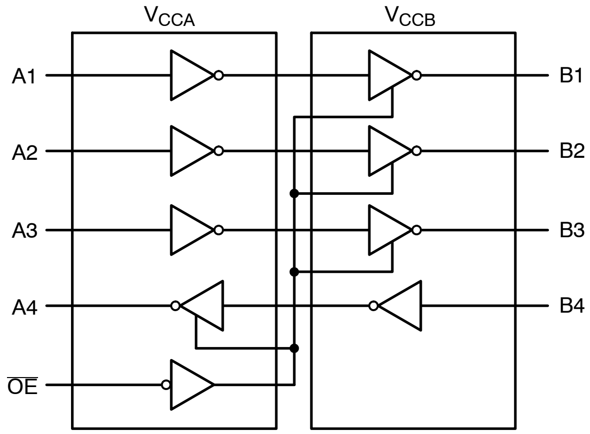
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

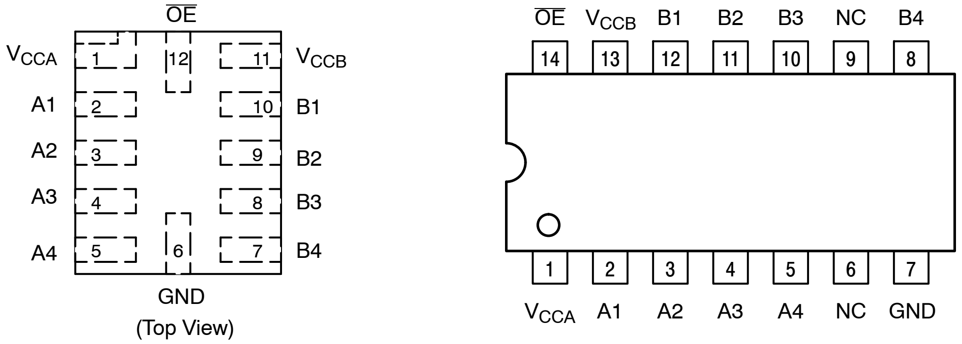


T30LMXT3V4T244 **T30LMXT3V4T240**



T30LMXT3V4T3144

Figure 1. Logic Diagrams



UQFN12 **SOIC−14/TSSOP−14**

Figure 2. Pin Assignments (Top View)

FUNCTION TABLE – T30LMXT3V4T244

Inputs		Output
$\overline{OE}$	A_n	B_n
L	L	L
L	H	H
H	X	3–State

FUNCTION TABLE – T30LMXT3V4T240

Inputs		Output
$\overline{OE}$	A_n	B_n
L	L	H
L	H	L
H	X	3–State

FUNCTION TABLE – T30LMXT3V4T3144

Inputs		Output
$\overline{OE}$	A1,A2,A3,B4	B1,B2,B3,A4
L	L	L
L	H	H
H	X	3–State

PIN ASSIGNMENT – T30LMXT3V4T244, T30LMXT3V4T240

PIN	FUNCTION
V_{CCA}	A–Port DC Power Supply
V_{CCB}	B–Port DC Power Supply
GND	Ground
$\overline{OE}$	Output Enable
A1, A2, A3, A4	Input Ports
B1, B2, B3, B4	Output Ports

PIN ASSIGNMENT – T30LMXT3V4T3144

PIN	FUNCTION
V_{CCA}	A–Port DC Power Supply
V_{CCB}	B–Port DC Power Supply
GND	Ground
$\overline{OE}$	Output Enable
A1, A2, A3, B4	Input Ports
B1, B2, B3, A4	Output Ports

Application Recommendations

During power−up and power−down, it is recommended that the $\overline{OE}$ pin be connected to V_{CC} through pull−up resistors to ensure high impedance at the I/O ports.

MAXIMUM RATINGS

Symbol	Rating	Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage	−0.5 to +4.3		V
V_I	DC Input Voltage $\overline{OE}$, A, B	−0.5 to +4.3		V
V_O	DC Output Voltage (Power Down Mode) A, B	−0.5 to +4.3	$V_{CCA} = V_{CCB} = 0$	V
	(3−State Mode) A, B	−0.5 to +4.3		
	(Active Mode) A	−0.5 to V_{CCA}+0.5		
	(Active Mode) B	−0.5 to V_{CCB}+0.5		
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C
θ_{JA}	Thermal Resistance (Note 1) SOIC−14 TSSOP−14 UQFN12		116 150 143	°C/W
P_D	Power Dissipation in Still Air SOIC−14 TSSOP−14 UQFN12		1077 833 875	mW
MSL	Moisture Sensitivity Level		Level 1	−
F_R	Flammability Rating Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 2) Human Body Model Charged Device Model		2 1	kV
$I_{LATCHUP}$	Latchup Performance (Note 3)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm−by−114mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to EIA/JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued per JEDEC/JEP172A.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CCA}, V_{CCB}	Positive DC Supply Voltage	0.9	3.6	V
V_I	Input Voltage	GND	3.6	V
V_{IO}	Output Voltage (Power Down Mode) A, B	GND	3.6	V
	(3−State Mode) A, B	GND	3.6	
	(Active Mode) A	GND	V_{CCA}	
	(Active Mode) B	GND	V_{CCB}	
T_A	Operating Temperature Range	−40	+125	°C
$\Delta t / \Delta V$	Input Transition Rise or Rate	0	5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS – INPUT VOLTAGES

						T_A = –40°C to +85°C			T_A = –40°C to +125°C		
Symbol	**Parameter**	**Test Condi- tions**	**Port**	**V_{CCA} (V)**	**V_{CCB} (V)**	**Min**	**Typ** (Note 4)	**Max**	**Min**	**Max**	**Unit**
V_{IH}	Input HIGH Voltage		$\overline{OE}$, A	2.7 – 3.6	0.9 – 3.6	2.0	–	–	2.0	–	V
				2.3 – 2.7		1.6	–	–	1.6	–	
				0.9 – 1.95		0.65 V_{CCA}	–	–	0.65 V_{CCA}	–	
			B	0.9 – 3.6	2.7 – 3.6	2.0	–	–	2.0	–	
					2.3 – 2.7	1.6	–	–	1.6	–	
					0.9 – 1.95	0.65 V_{CCB}	–	–	0.65 V_{CCB}	–	
V_{IL}	Input LOW Voltage		$\overline{OE}$, A	2.7 – 3.6	0.9 – 3.6	–	–	0.8	–	0.8	V
				2.3 – 2.7		–	–	0.7	–	0.7	
				0.9 – 1.95		–	–	0.35 V_{CCA}	–	0.35 V_{CCA}	
			B	0.9 – 3.6	2.7 – 3.6	–	–	0.8	–	0.8	
					2.3 – 2.7	–	–	0.7	–	0.7	
					0.9 – 1.95	–	–	0.35 V_{CCB}	–	0.35 V_{CCB}	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. All typical values are at T_A = 25°C.

DC ELECTRICAL CHARACTERISTICS − OUTPUT VOLTAGES

Symbol	Parameter	Test Conditions	V_{CCA} (V)	V_{CCB} (V)	T_A = −40°C to +85°C			T_A = −40°C to +125°C		Unit
					Min	Typ (Note 4)	Max	Min	Max	
V_{OH}	Output HIGH Voltage	$V_I = V_{IH}$ or V_{IL}:								V
		I_{OH} = −100 µA A	0.9 – 3.6	0.9 – 3.6	V_{CCA} − 0.1	–	–	V_{CCA} − 0.1	–	
		B	0.9 – 3.6	0.9 – 3.6	V_{CCB} − 0.1	–	–	V_{CCB} − 0.1	–	
		I_{OH} = −0.5 mA	0.9	0.9	0.7	–	–	0.7	–	
		I_{OH} = −3 mA	1.1	1.1	0.85	–	–	0.85	–	
		I_{OH} = −6 mA	1.4	1.4	1.05	–	–	1.05	–	
		I_{OH} = −8 mA	1.65	1.65	1.2	–	–	1.2	–	
		I_{OH} = −12 mA	2.3	2.3	1.8	–	–	1.8	–	
			2.7	2.7	2.2	–	–	2.2	–	
		I_{OH} = −18 mA	2.3	2.3	1.7	–	–	1.7	–	
			3.0	3.0	2.4	–	–	2.4	–	
		I_{OH} = −24 mA	3.0	3.0	2.2	–	–	2.2	–	
V_{OL}	Output LOW Voltage	$V_I = V_{IH}$ or V_{IL}:								V
		I_{OL} = 100 µA	0.9 – 3.6	0.9 – 3.6	–	–	0.1	–	0.1	
		I_{OL} = 0.5 mA	0.9	0.9	–	–	0.2	–	0.2	
		I_{OL} = 3 mA	1.1	1.1	–	–	0.25	–	0.25	
		I_{OL} = 6 mA	1.4	1.4	–	–	0.35	–	0.35	
		I_{OL} = 8 mA	1.65	1.65	–	–	0.3	–	0.3	
		I_{OL} = 12 mA	2.3	2.3	–	–	0.4	–	0.4	
			2.7	2.7	–	–	0.4	–	0.4	
		I_{OL} = 18 mA	2.3	2.3	–	–	0.4	–	0.4	
			3.0	3.0	–	–	0.4	–	0.4	
		I_{OL} = 24 mA	3.0	3.0	–	–	0.55	–	0.55	

DC ELECTRICAL CHARACTERISTICS − LEAKAGE AND SUPPLY CURRENTS

Symbol	Parameter	Test Conditions	V_{CCA} (V)	V_{CCB} (V)	T_A = −40°C to +85°C		T_A = −40°C to +125°C		Unit
					Min	Max	Min	Max	
I_I	Input Leakage Current	V_I = 3.6 V or GND	0.9 – 3.6	0.9 – 3.6	–	±0.1	–	±1.0	µA
I_{OZ}	3−State Output Leakage	$\overline{OE} = V_{IH}$; V_I = 3.6 V or GND, V_O = GND to 3.6 V	3.6	3.6	–	±0.1	–	±1.0	µA
I_{OFF}	Power−Off Leakage Current	V_I or V_O = 0 to 3.6 V A	0	0.9 – 3.6	–	±0.1	–	±1.0	µA
		B	0.9 – 3.6	0	–	±0.1	–	±1.0	
I_{CCA}	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; I_O = 0	0.9 – 3.6	0.9 – 3.6	–	0.5	–	1.0	µA
			0	0.9 – 3.6	–	−0.1	–	−1	
			0.9 – 3.6	0	–	0.1	–	1.0	
I_{CCB}	Quiescent Supply Current	$V_I = V_{CCB}$ or GND; I_O = 0	0.9 – 3.6	0.9 – 3.6	–	0.5	–	1.0	µA
			0	0.9 – 3.6	–	0.1	–	1.0	
			0.9 – 3.6	0	–	−0.1	–	−1.0	

NOTE: Connect ground before applying supply voltage V_{CCA} or V_{CCB}. This device is designed with the feature that the power−up sequence of V_{CCA} and V_{CCB} will not damage the IC.

AC ELECTRICAL CHARACTERISTICS (Notes 5 and 6)

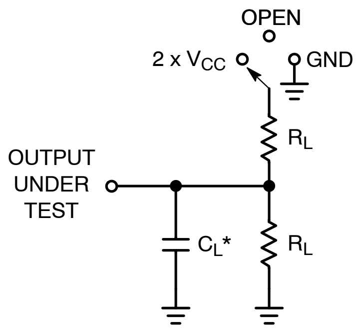
Symbol	Parameter	V_{CCA} (V)	T_A = −40°C to +85°C					T_A = −40°C to +125°C					Unit
			V_{CCB} (V)					V_{CCB} (V)					
			3.3	2.5	1.8	1.5	1.2	3.3	2.5	1.8	1.5	1.2	
			Max	Max	Max	Max	Max	Max	Max	Max	Max	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A to B	3.3	2.3	2.8	3.5	4.2	8.0	2.6	3.3	3.9	4.7	8.3	nS
		2.5	2.7	3.1	3.8	4.4	8.2	2.9	3.5	4.2	4.9	8.5	
		1.8	3.2	3.6	4.0	4.6	8.4	3.5	3.9	4.5	5.0	8.7	
		1.5	3.9	4.0	4.4	5.1	8.7	4.1	4.3	4.8	5.5	9.0	
		1.2	4.9	5.0	5.2	6.1	9.0	5.3	5.4	5.9	6.9	9.3	
	Propagation Delay, B to A	3.3	2.3	2.7	3.2	3.9	4.9	2.6	2.9	3.5	4.1	5.3	
		2.5	2.8	3.1	3.6	4.0	5.0	3.3	3.5	3.9	4.3	5.4	
		1.8	3.5	3.8	4.0	4.4	5.2	3.9	4.2	4.5	4.8	5.9	
		1.5	4.2	4.4	4.6	5.1	6.1	4.7	4.9	5.0	5.5	6.9	
		1.2	8.0	8.2	8.4	8.7	9.0	8.3	8.5	8.7	9.0	9.3	
t_{PZH}, t_{PZL}	Output Enable, $\overline{OE}$ to A	3.3	2.8	3.2	3.5	4.0	5.4	3.1	3.4	3.7	4.2	5.7	nS
		2.5	4.2	4.4	4.6	4.8	5.7	4.7	4.9	5.1	5.3	6.0	
		1.8	6.7	6.7	6.7	6.7	6.7	7.5	7.5	7.5	7.5	7.5	
		1.5	9.1	9.1	9.1	9.1	9.1	10	10	10	10	10	
		1.2	12.8	12.8	12.8	12.8	12.8	13.3	13.3	13.3	13.3	13.3	
	Output Enable, $\overline{OE}$ to B	3.3	3.5	4.2	5.8	8.0	11.3	4.2	4.9	6.7	8.4	11.9	
		2.5	4	4.8	6.3	8.3	11.3	4.4	5.3	7.0	8.7	11.9	
		1.8	4.6	5.3	7.0	8.6	11.3	5.1	5.9	7.5	9.0	11.9	
		1.5	5.6	5.8	7.5	8.9	11.3	6.2	6.4	8.0	9.3	11.9	
		1.2	8.7	8.8	9.1	9.8	12.3	8.9	9.0	9.3	10.0	12.5	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{OE}$ to A	3.3	5.6	5.6	5.6	5.6	5.6	6.1	6.1	6.1	6.1	6.1	nS
		2.5	6.2	6.2	6.2	6.2	6.2	6.7	6.7	6.7	6.7	6.7	
		1.8	6.9	6.9	6.9	6.9	6.9	7.4	7.4	7.4	7.4	7.4	
		1.5	7.6	7.6	7.6	7.6	7.6	8.2	8.2	8.2	8.2	8.2	
		1.2	9.5	9.5	9.5	9.5	9.5	10.5	10.5	10.5	10.5	10.5	
	Output Disable, $\overline{OE}$ to B	3.3	5.6	5.6	5.6	5.6	5.6	6.1	6.1	6.1	6.1	6.1	
		2.5	6.2	6.2	6.2	6.2	6.2	6.7	6.7	6.7	6.7	6.7	
		1.8	6.9	6.9	6.9	6.9	6.9	7.4	7.4	7.4	7.4	7.4	
		1.5	7.6	7.6	7.6	7.6	7.6	8.2	8.2	8.2	8.2	8.2	
		1.2	9.5	9.5	9.5	9.5	9.5	10.5	10.5	10.5	10.5	10.5	

5. Propagation delays defined per Figure 3.
6. These parameters are guaranteed by characterization and are not production tested.

CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 4)	Unit
C_{IN}	Control Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or V_{CCA}	2.5	pF
$C_{I/O}$	I/O Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or V_{CCA}	5.0	pF
C_{PD} (Note 7)	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or V_{CCA}, f = 10 MHz	12	pF

7. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: $I_{CC(operating)} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where $I_{CC} = I_{CCA} + I_{CCB}$ and N_{SW} = total number of outputs switching.



*C_L Includes probe and jig capacitance

Figure 3. AC Test Circuit

Test	Switch	C_L	R_L
t_{PLH}, t_{PHL}	OPEN	15 pF	2 kΩ
t_{PLZ}, t_{PZL}	2 x V_{CC}		
t_{PHZ}, t_{PZH}	GND		
C_L includes probe and jig capacitance Pulse generator Z_O = 50 Ω Input f = 1.0 MHz; t_W = 500 ns			

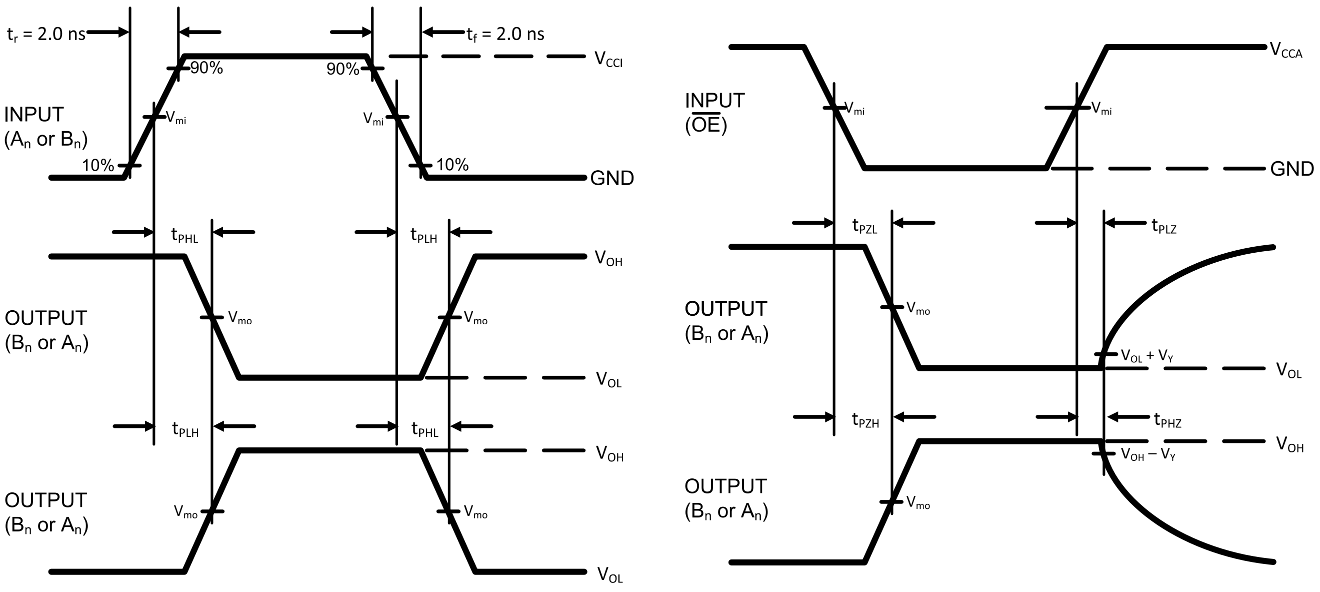


Figure 4. AC Waveforms

Symbol	V_{CC}				
	3.0 V – 3.6 V	2.3 V – 2.7 V	1.65 V – 1.95 V	1.4 V – 1.6 V	1.1 V – 1.3 V
V_{mi}	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$
V_{mo}	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$
V_Y	0.3 V	0.15 V	0.15 V	0.1 V	0.1 V

8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CCO} is the V_{CC} associated with the output port.

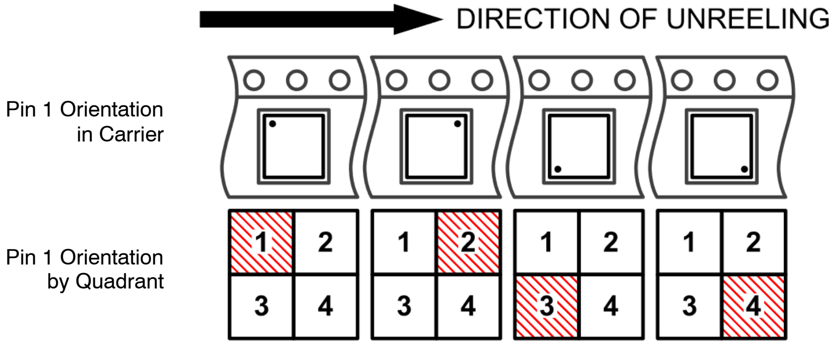
ORDERING INFORMATION

Device	Marking	Package	Pin 1 Quadrant	Shipping†
T30LMXT3V4T244MU2TAG	TBD	UQFN12	1	3000 Units / Tape & Reel
T30LAXT3V4T244MU2TAG*	TBD	UQFN12	1	3000 Units / Tape & Reel
T30LMXT3V4T244DR2G (Contact **onsemi** sales)	TBD	SOIC−14	TBD	2500 Units / Tape & Reel
T30LMXT3V4T244DTR2G (Contact **onsemi** sales)	TBD	TSSOP−14	TBD	2500 Units / Tape & Reel
T30LMXT3V4T240MU2TAG	TBD	UQFN12	1	3000 Units / Tape & Reel
T30LMXT3V4T240DR2G (Contact **onsemi** sales)	TBD	SOIC−14	TBD	2500 Units / Tape & Reel
T30LMXT3V4T240DTR2G (Contact **onsemi** sales)	TBD	TSSOP−14	TBD	2500 Units / Tape & Reel
T30LMXT3V4T3144MU2TAG	TBD	UQFN12	1	3000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

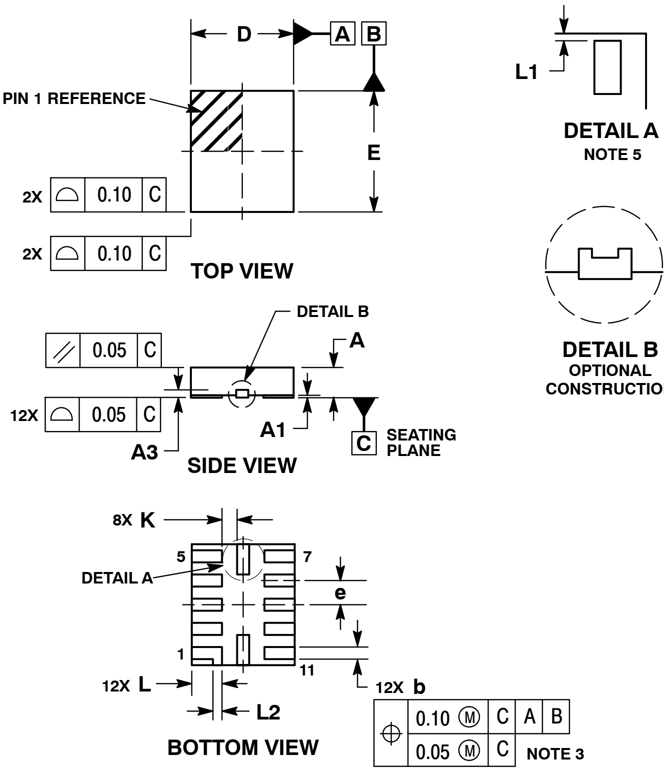
*For Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel



PACKAGE DIMENSIONS

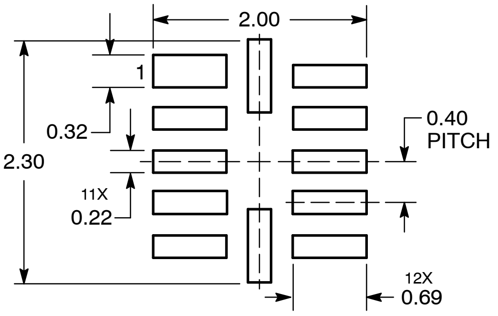
UQFN12 1.7x2.0, 0.4P
CASE 523AE
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	----
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

MOUNTING FOOTPRINT SOLDERMASK DEFINED

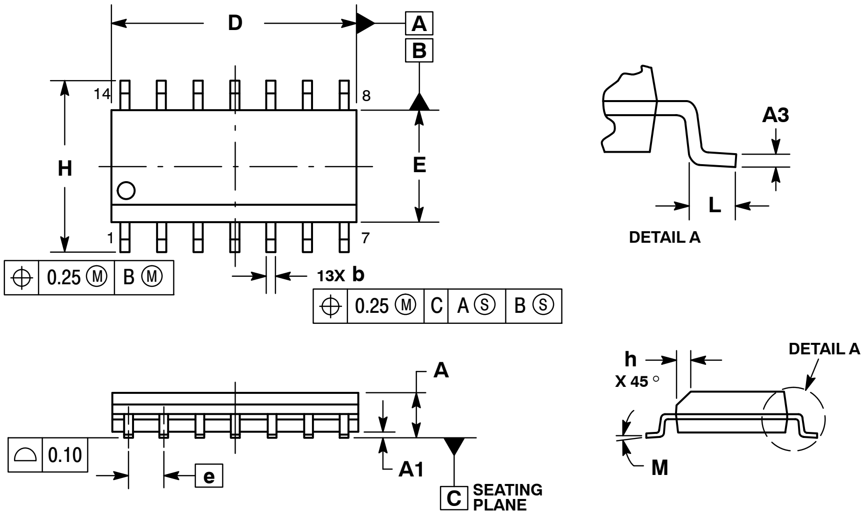


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

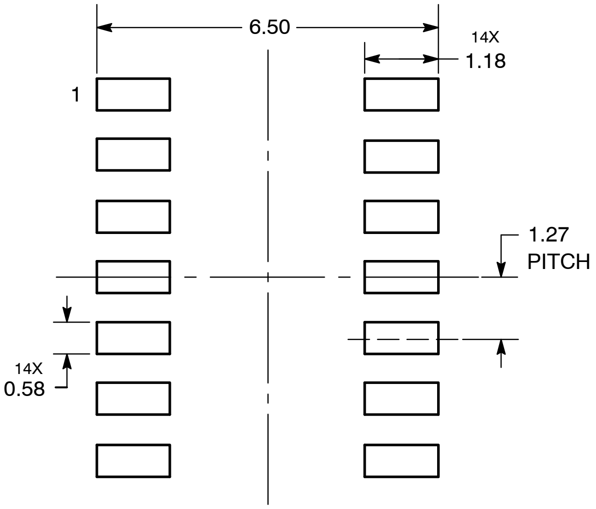
SOIC−14
D SUFFIX
CASE 751A−03
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*

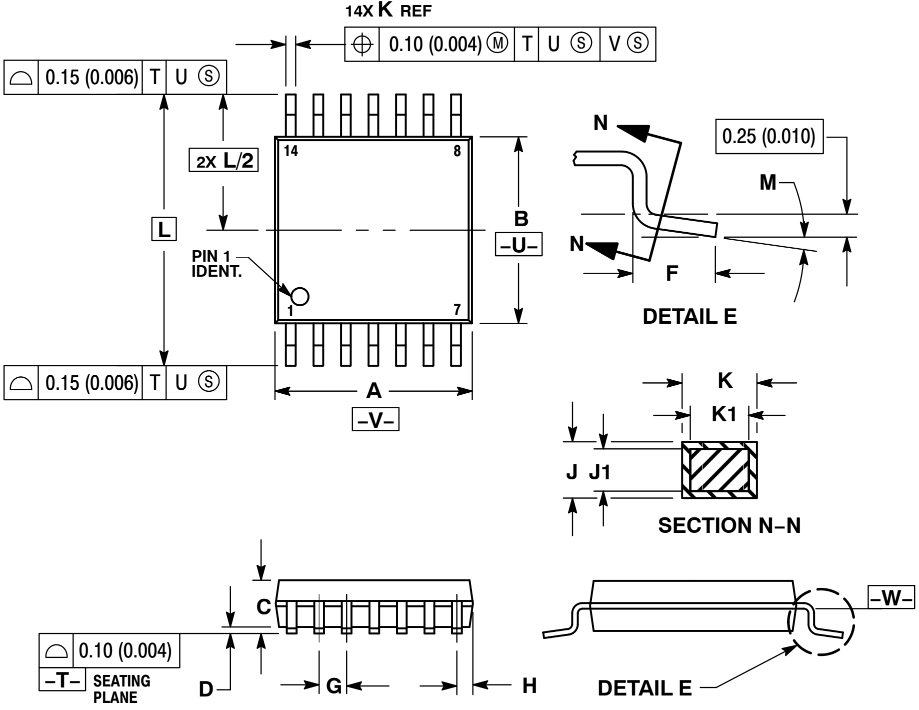


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

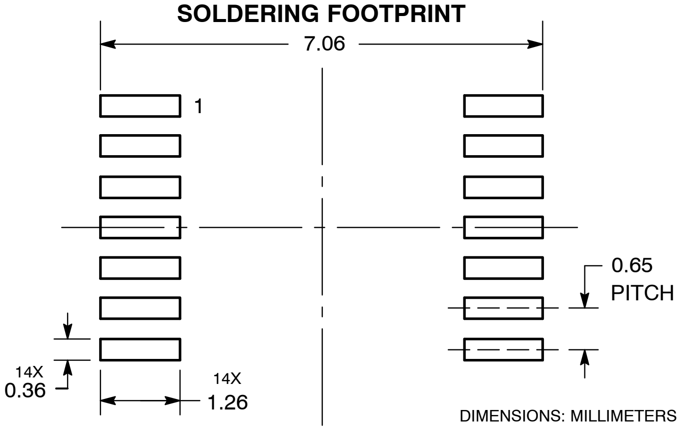
TSSOP−14
DT SUFFIX
CASE 948G
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



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