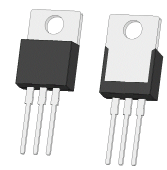
Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO220-3, 650 V, 80 mohm

UF3C065080T3S



TO220-3 10.16x15.37x4.19, 2.54P
CASE 221AL

Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO220-3 package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads when used with recommended RC-snubbers, and any application requiring standard gate drive.

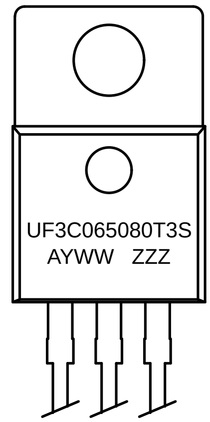
Features

- Typical On-resistance $R_{DS(on),typ}$ of 80 mΩ
- Maximum Operating Temperature of 175 °C
- Excellent Reverse Recovery
- Low Gate Charge
- Low Intrinsic Capacitance
- ESD Protected, HBM Class 2
- Very Low Switching Losses (Required RC-snubber Loss Negligible under Typical Operating Conditions)
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Typical Applications

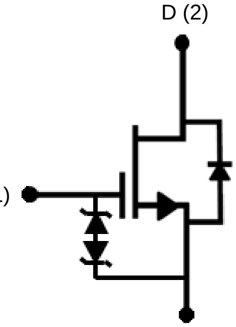
- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

MARKING DIAGRAM



UF3C065080T3S	= Specific Device Code
A	= Assembly Location
YY	= Year
WW	= Work Week
ZZZ	= Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

March, 2025 − Rev. 4
Publication Order Number:
UF3C065080T3S/D

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		650	V
Gate-source Voltage	V_{GS}	DC	−25 to +25	V
Continuous Drain Current (Note 1)	I_D	T_C = 25 °C	31	A
		T_C = 100 °C	23	A
Pulsed Drain Current (Note 2)	I_{DM}	T_C = 25 °C	65	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	L= 15 mH, I_{AS} = 2.1 A	33	mJ
Power Dissipation	P_{tot}	T_C = 25 °C	190	W
Maximum Junction Temperature	$T_{J,max}$		175	°C
Operating and Storage Temperature	T_J, T_{STG}		−55 to 175	°C
Max. Lead Temperature for Soldering, 1/8” from Case for 5 Seconds	T_L		250	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25 °C

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		−	0.61	0.79	°C/W

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE − STATIC						
Drain-source Breakdown Voltage	BV_{DS}	V_{GS} = 0 V, I_D = 1 mA	650	−	−	V
Total Drain Leakage Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 25 °C	−	6	100	μA
		V_{DS} = 650 V, V_{GS} = 0 V, T_J = 175 °C	−	40	−	
Total Gate Leakage Current	I_{GSS}	V_{DS} = 0 V, T_J = 25 °C, V_{GS} = −20 V / +20 V	−	6	±20	μA
Drain-source On-resistance	$R_{DS(on)}$	V_{GS} = 12 V, I_D = 20 A, T_J = 25 °C	−	80	100	mΩ
		V_{GS} = 12 V, I_D = 20 A, T_J = 125 °C	−	111	−	
		V_{GS} = 12 V, I_D = 20 A, T_J = 175 °C	−	141	−	
Gate Threshold Voltage	$V_{G(th)}$	V_{DS} = 5 V, I_D = 10 mA	4	5	6	V
Gate Resistance	R_G	f = 1 MHz, open drain	−	4.5	−	Ω
TYPICAL PERFORMANCE − REVERSE DIODE						
Diode Continuous Forward Current (Note 4)	I_S	T_C = 25 °C	−	−	31	A
Diode Pulse Current (Note 5)	$I_{S,pulse}$	T_C = 25 °C	−	−	65	A
Forward Voltage	V_{FSD}	V_{GS} = 0 V, I_S = 10 A, T_J = 25 °C	−	1.5	2	V
		V_{GS} = 0 V, I_S = 10 A, T_J = 175 °C	−	1.75	−	
Reverse Recovery Charge	Q_{rr}	V_{DS} = 400 V, I_S = 20 A, V_{GS} = −5 V, R_{G_EXT} = 10 Ω ,di/dt = 2200 A/μs, T_J = 25 °C	−	119	−	nC
Reverse Recovery Time	t_{rr}		−	16	−	ns
Reverse Recovery Charge	Q_{rr}	V_{DS} = 400 V, I_S = 20 A, V_{GS} = −5 V, R_{G_EXT} = 10 Ω, di/dt = 2200 A/μs, T_J = 150 °C	−	73	−	nC
Reverse Recovery Time	t_{rr}		−	11	−	ns

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE − DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 100 V, V_{GS} = 0 V, f = 100 kHz	−	1500	−	pF
Output Capacitance	C_{oss}		−	104	−	
Reverse Transfer Capacitance	C_{rss}		−	2.6	−	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	−	77	−	pF
Effective Output Capacitance, Time Related	$C_{oss(tr)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	−	176	−	pF
C_{OSS} Stored Energy	E_{oss}	V_{DS} = 400 V, V_{GS} = 0 V	−	6.2	−	μJ
Total Gate Charge	Q_G	V_{DS} = 400 V, I_D = 20 A, V_{GS} = −5 V to15 V	−	51	−	nC
Gate-drain Charge	Q_{GD}		−	11	−	
Gate-source Charge	Q_{GS}		−	19	−	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 400 V, I_D = 20 A, Gate Driver = −5 V to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 22 Ω Inductive Load, FWD: same device with V_{GS} = −5 V and R_G = 22 Ω, RC snubber: R_S = 5 Ω and C_S = 100 pF, T_J = 25 °C	−	25	−	ns
Rise Time	t_r		−	14	−	
Turn-off Delay Time	$t_{d(off)}$		−	54	−	
Fall Time	t_f		−	11	−	
Turn-on Energy Including R_S Energy (Note 6)	E_{ON}		−	182	−	μJ
Turn-off Energy Including R_S Energy (Note 6)	E_{OFF}		−	24	−	
Total Switching Energy Including R_S Energy (Note 6)	E_{TOTAL}		−	206	−	
Snubber R_S Energy During Turn-on	E_{RS_ON}		−	0.6	−	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		−	1.1	−	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 400 V, I_D = 20 A, Gate Driver = −5 V to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 22 Ω Inductive Load, FWD: same device with V_{GS} = −5 V and R_G = 22 Ω, RC snubber: R_S = 5 Ω and C_S = 100 pF, T_J = 150 °C	−	22	−	ns
Rise Time	t_r		−	14	−	
Turn-off Delay Time	$t_{d(off)}$		−	55	−	
Fall Time	t_f		−	12	−	
Turn-on Energy Including R_S Energy (Note 6)	E_{ON}		−	156	−	μJ
Turn-off Energy Including R_S Energy (Note 6)	E_{OFF}		−	25	−	
Total Switching Energy Including R_S Energy (Note 6)	E_{TOTAL}		−	181	−	
Snubber R_S Energy During Turn-on	E_{RS_ON}		−	0.6	−	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		−	1.2	−	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Limited by $T_{J,max}$
5. Pulse width t_p limited by $T_{J,max}$
6. The switching performance are evaluated with a RC snubber circuit as shown in Figure 24.

TYPICAL PERFORMANCE DIAGRAMS

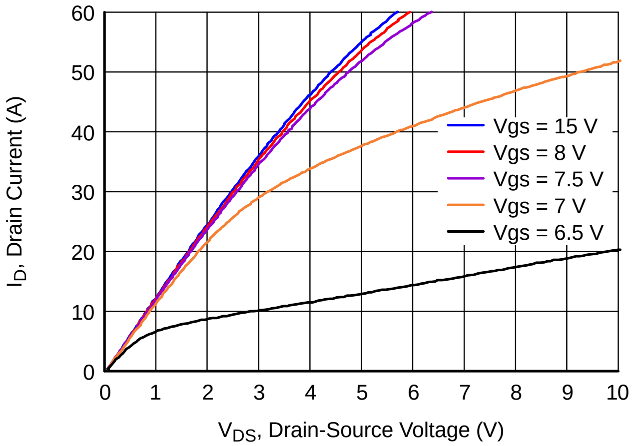


Figure 1. Typical Output Characteristics at T_J = −55 °C, t_p < 250 μs

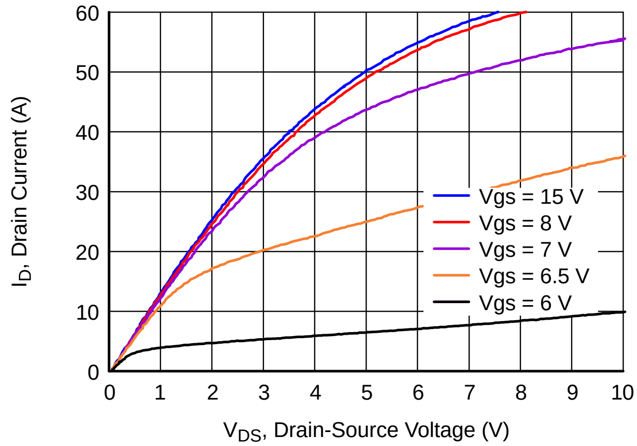


Figure 2. Typical Output Characteristics at T_J = 25 °C, t_p < 250 μs

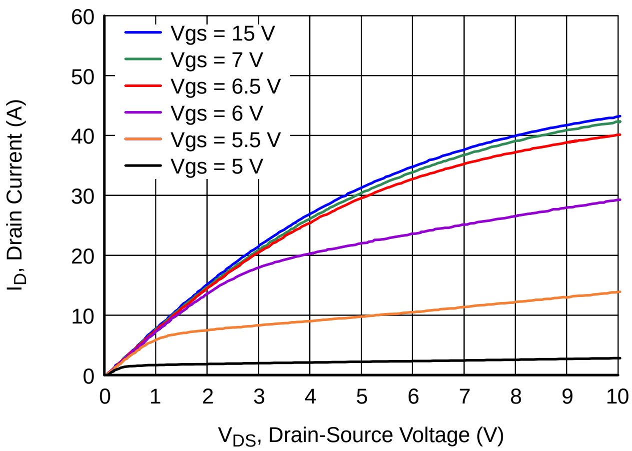


Figure 3. Typical Output Characteristics at T_J = 175 °C, t_p < 250 μs

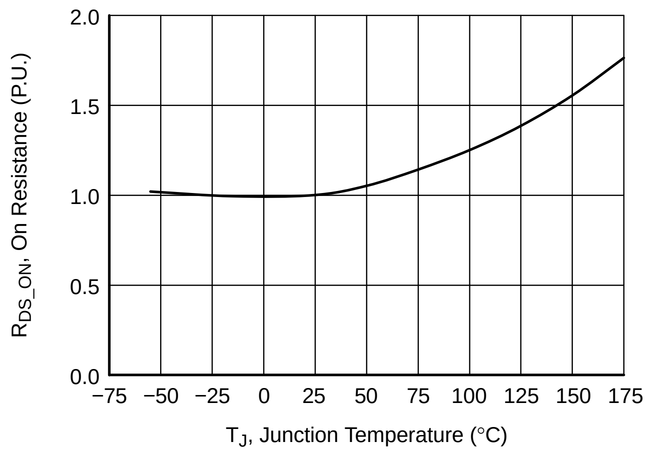


Figure 4. Normalized On-Resistance vs. Temperature at V_{GS} = 12 V and I_D = 20 A

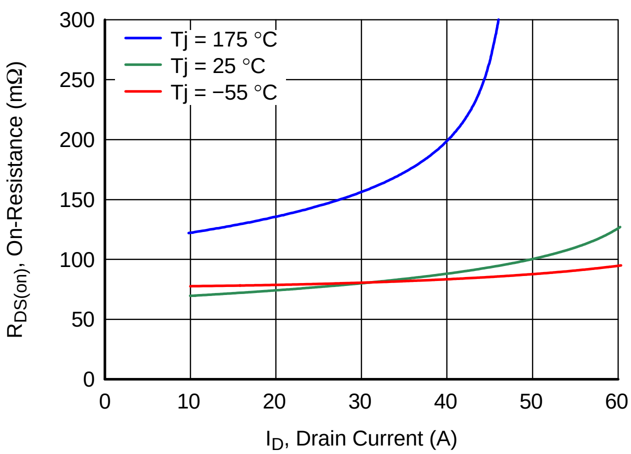


Figure 5. Typical Drain-Source On-Resistances at V_{GS} = 12 V

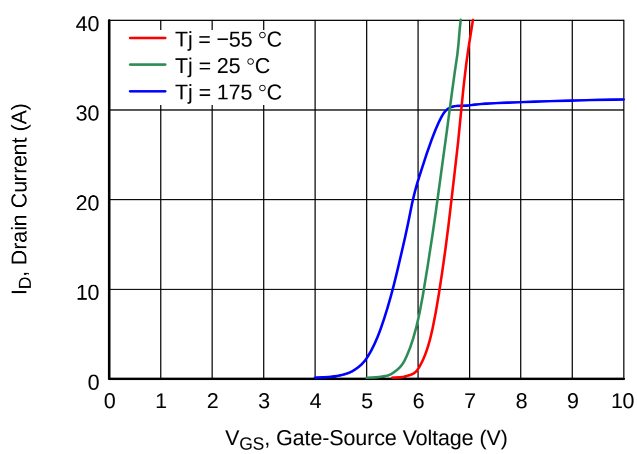


Figure 6. Typical Transfer Characteristics at V_{DS} = 5 V

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

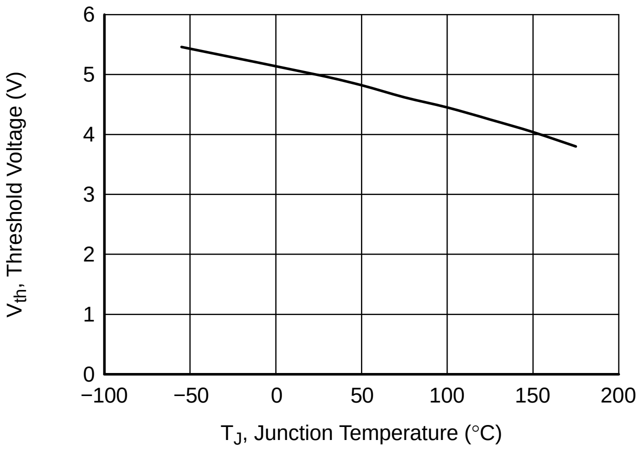


Figure 7. Threshold Voltage vs. Junction Temperature at V_{DS} = 5 V and I_D = 10 mA

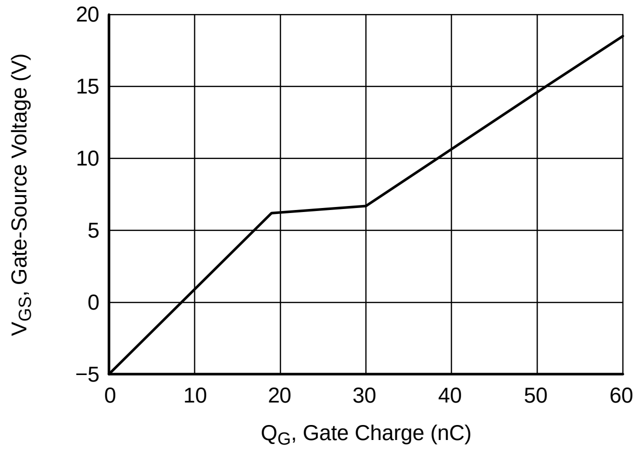


Figure 8. Typical Gate Charge at V_{DS} = 400 V and I_D = 20 A

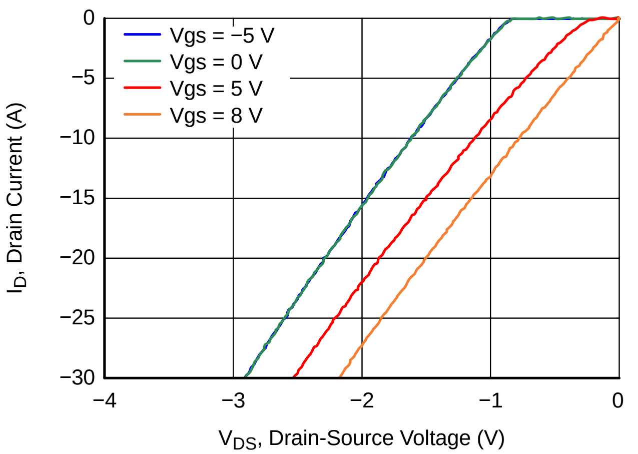


Figure 9. 3rd Quadrant Characteristics at T_J = −55 °C

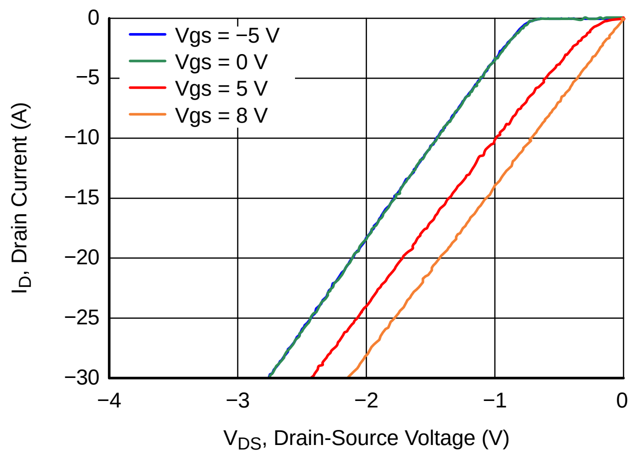


Figure 10. 3rd Quadrant Characteristics at T_J = 25 °C

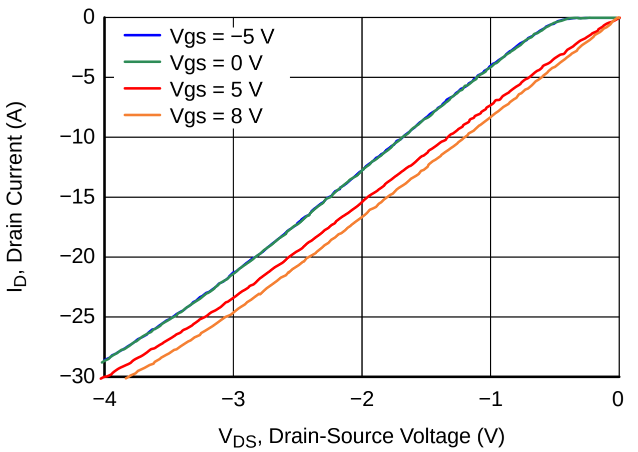


Figure 11. 3rd Quadrant Characteristics at T_J = 175 °C

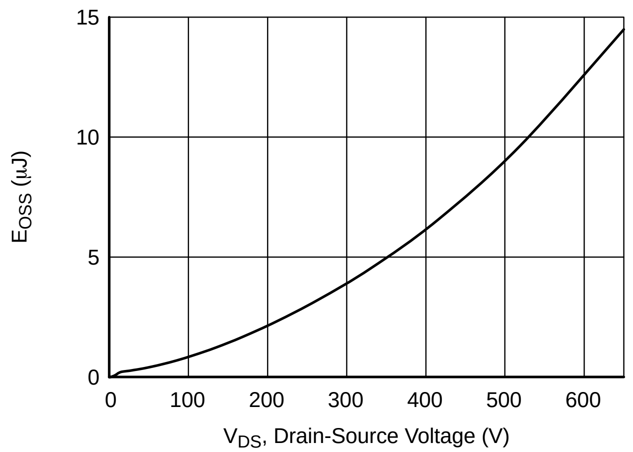


Figure 12. Typical Stored Energy in C_{OSS} at V_{GS} = 0 V

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

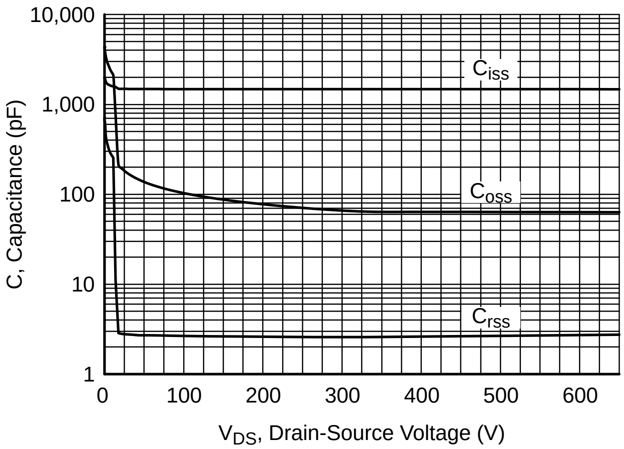


Figure 13. Typical Capacitances at f = 100 kHz and V_{GS} = 0 V

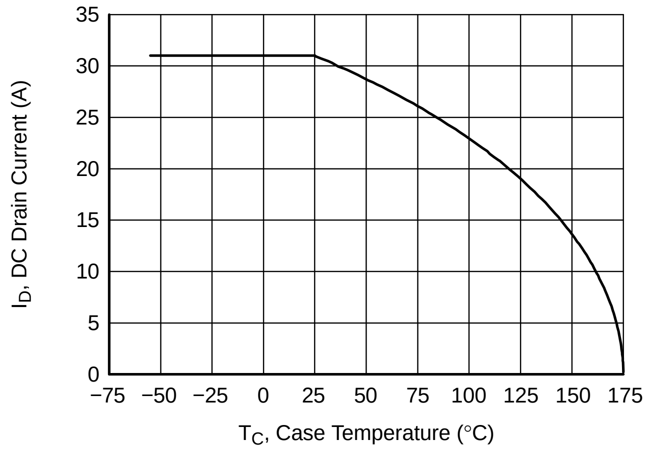


Figure 14. DC Drain Current Derating

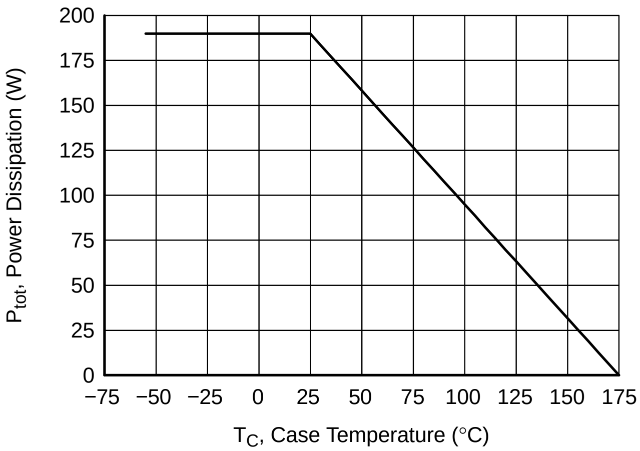


Figure 15. Total Power Dissipation

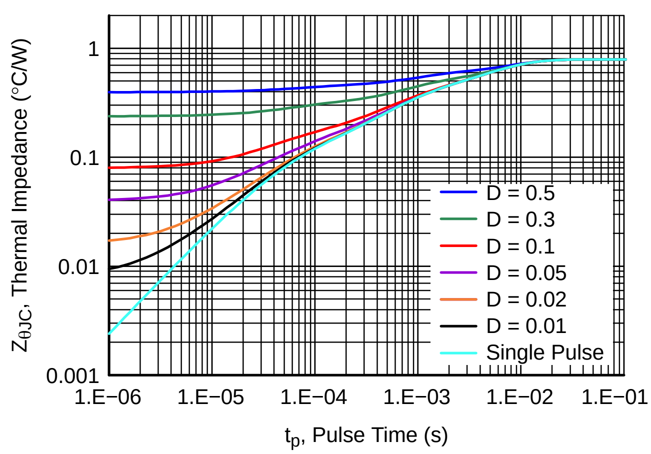


Figure 16. Maximum Transient Thermal Impedance

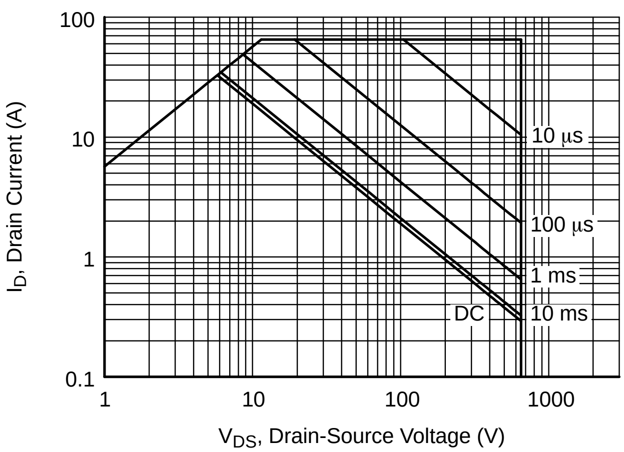


Figure 17. Safe Operation Area at T_C = 25 °C, D = 0, Parameter t_p

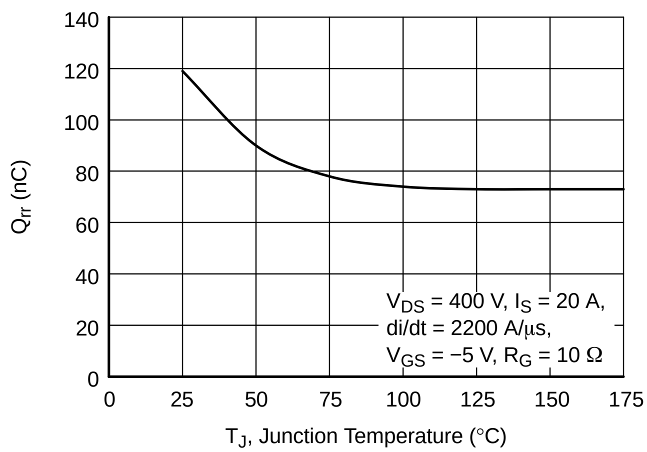
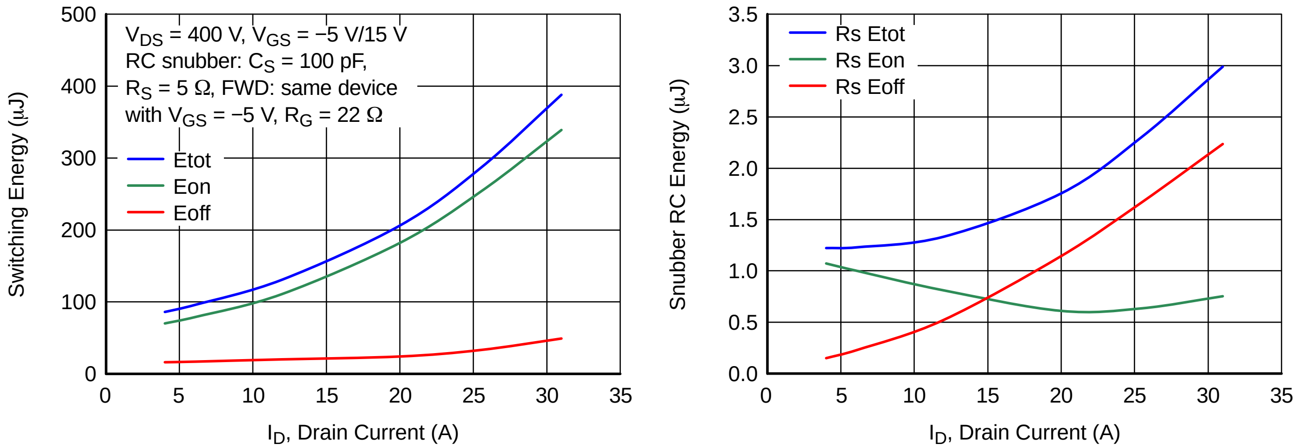


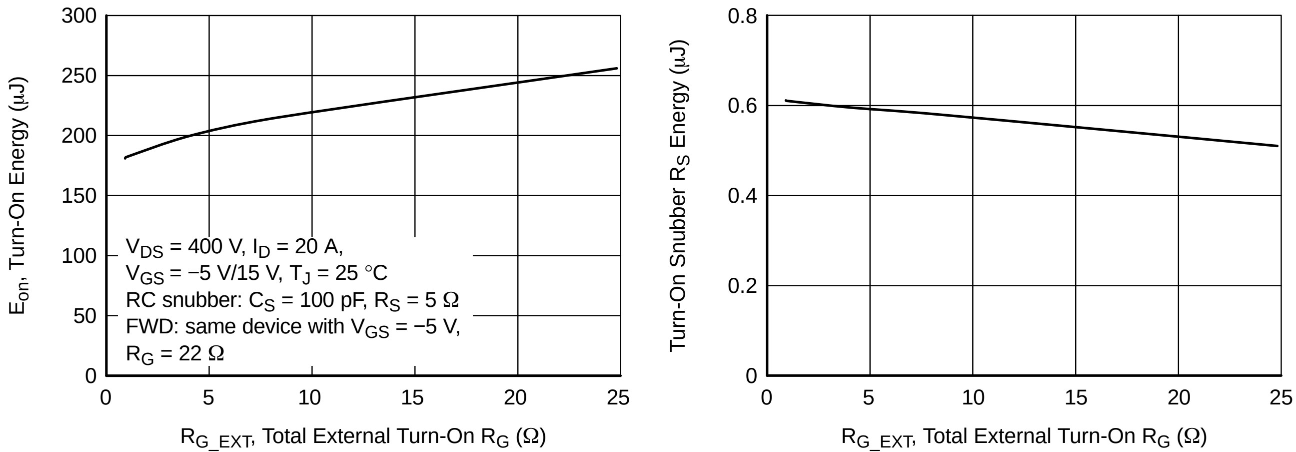
Figure 18. Reverse Recovery Charge Q_{rr} vs. Junction Temperature

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)



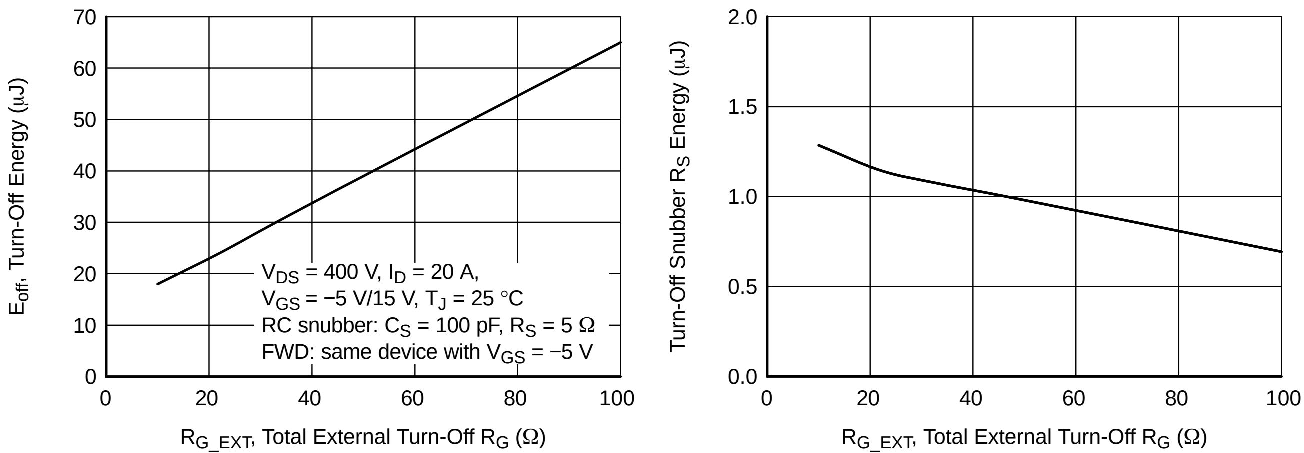
(a) (b)

Figure 19. Clamped Inductive Switching Energy (a) and RC Snubber Energy Loss (b) vs. Drain Current at T_J = 25 °C, Turn-On R_{G_EXT} = 1 Ω, and Turn-off R_{G_EXT} = 22 Ω



(a) (b)

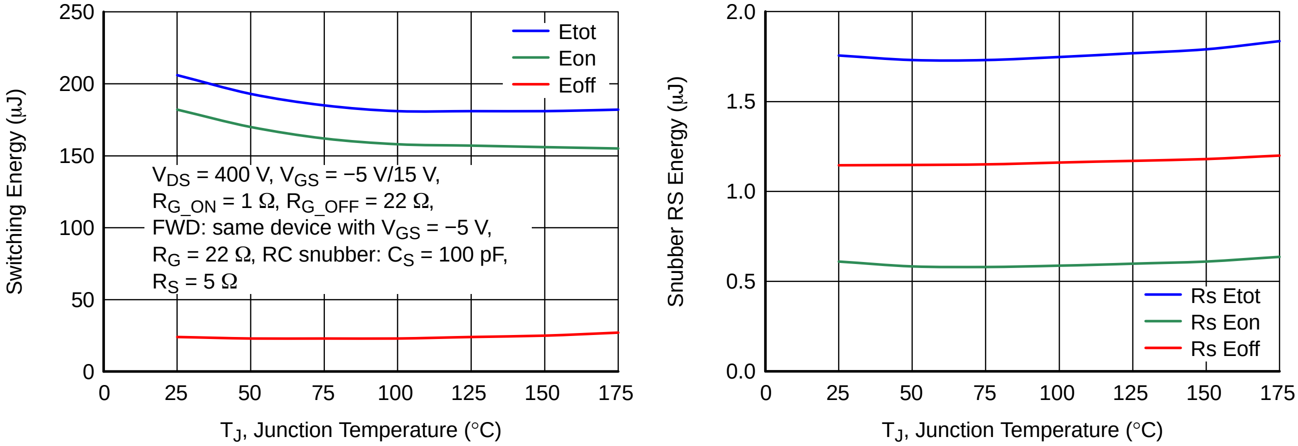
Figure 20. Clamped Inductive Switching Turn-On Energy Including RC Snubber Energy Loss (a) and RC Snubber Energy Loss (b) as a Function of Total External Turn-On Gate Resistor R_{G_EXT}



(a) (b)

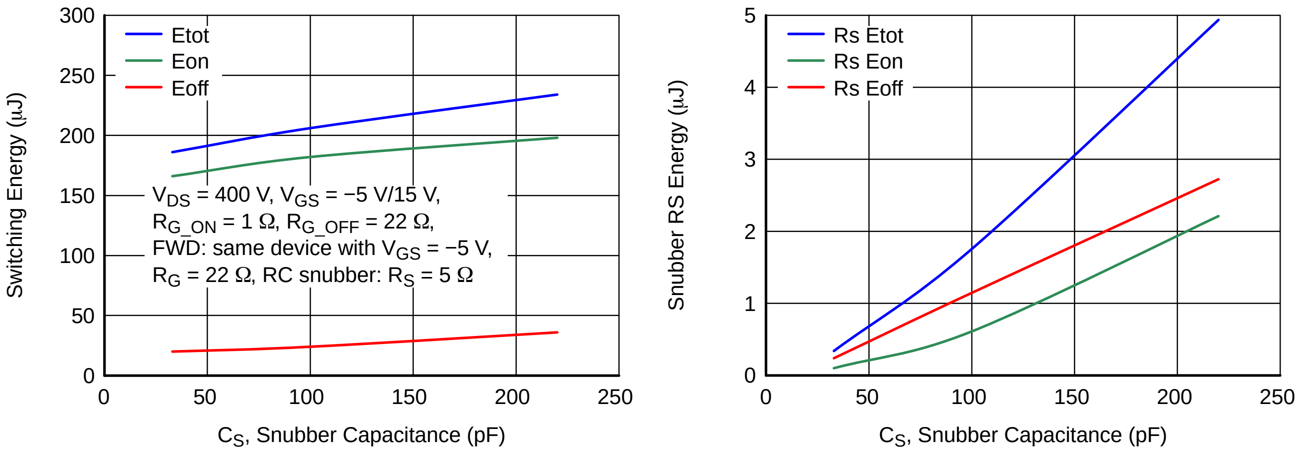
Figure 21. Clamped Inductive Switching Turn-Off Energy Including RC Snubber Energy Loss (a) and RC Snubber Energy Loss (b) as a Function of Total External Turn-Off Gate Resistor R_{G_EXT}

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)



(a) (b)

Figure 22. Clamped Inductive Switching Energy Including RC Snubber Energy Loss (a) and RC Snubber Energy Loss (b) as a Function of Junction Temperature at I_D = 20 A



(a) (b)

Figure 23. Clamped Inductive Switching Energy Including RC Snubber Energy Loss (a) and RC Snubber Energy Loss (b) as a Function of Snubber Capacitance at I_D = 20 A and T_J = 25 °C

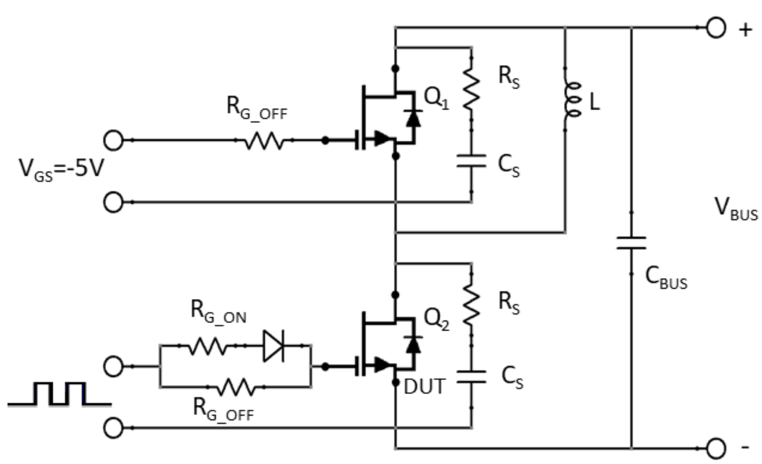


Figure 24. Clamped Inductive Load Switching Test Circuit
An RC Snubber (R_S = 5 Ω and C_S = 100 pF) is Required to Improve the Turn-off Waveforms

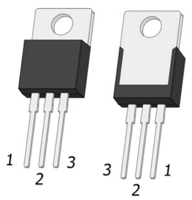
APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a highvoltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

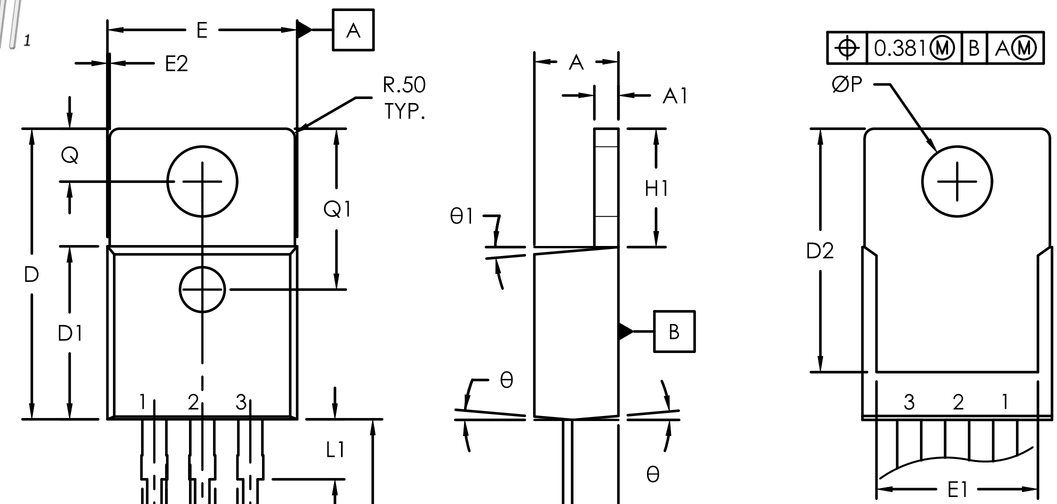
ORDERING INFORMATION

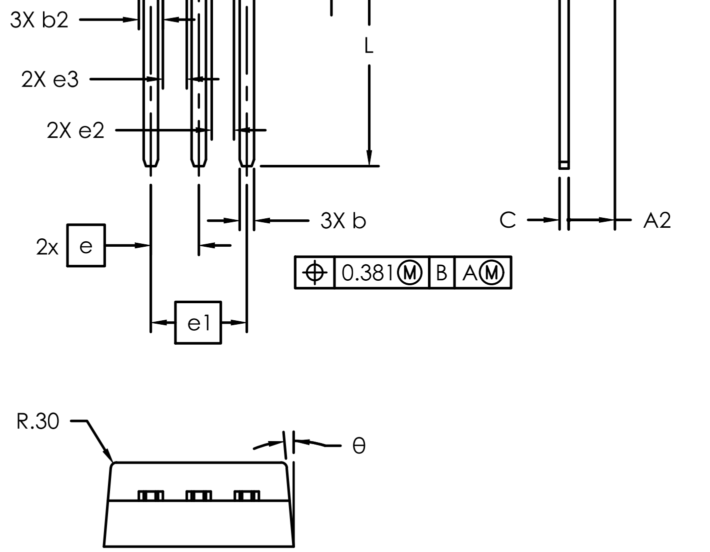
Part Number	Marking	Package	Shipping†
UF3C065080T3S	UF3C065080T3S	TO220-3 10.16x15.37x4.19, 2.54P (Pb-Free, Halogen Free)	1000 / Tube



TO220−3 10.16x15.37x4.19, 2.54P
CASE 221AL
ISSUE B

DATE 22 APR 2025



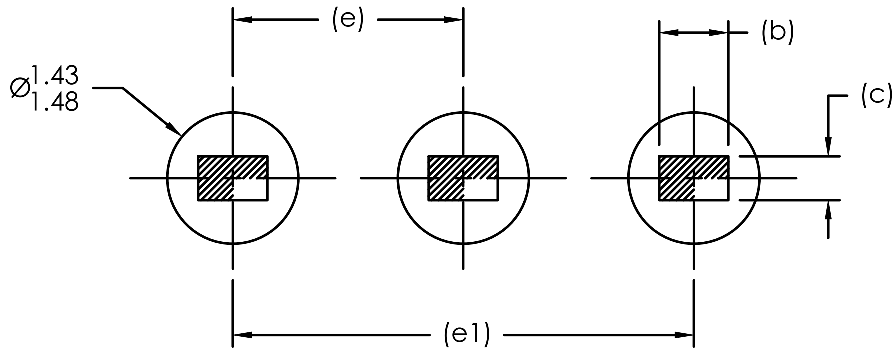


SYM	millimeters		
	MIN	NOM	MAX
A	3.56	4.19	4.83
A1	0.51	0.95	1.40
A2	2.03	2.48	2.92
b	0.38	0.70	1.02
b2	1.02	1.40	1.78
c	0.36	0.56	0.76
D	14.22	15.37	16.51
D1	8.38	8.89	9.40
D2	12.19	12.66	13.13
E	9.65	10.16	10.67
e	2.54 BSC		
e1	5.08 BSC		
e2	1.03	1.13	1.23
e3	1.17	1.27	1.37
E1	6.86	7.87	8.89
E2	–	–	0.76
L	12.57	13.65	14.73
L1	–	–	6.35
ØP	3.53	3.81	4.09
H1	5.84	6.35	6.86
Q	2.54	2.98	3.43
Q1	8.38	8.51	8.64
θ	5°		
θ1	5°		

NOTES:
1. Dimensioning and Tolerancing as per ASME Y14.5M - 2018.
2. Controlling Dimension: Millimeters
3. Dimensions D and E does not include Mold Flash. These dimensions are measure at the outermost extreme of the plastic body.
4. Through hole diameter value = End Hole Diameter
5. PCB through hole pattern as per IPC-2222

DOCUMENT NUMBER:	**98AON66225E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO220−3 10.16x15.37x4.19, 2.54P**	**PAGE 1 OF 2**

RECOMMENDED PCB PATTERN



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

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