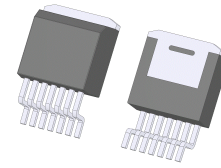


# Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO-263-7, 1700 V, 410 mohm

## UF3C170400B7S



TO-263-7  
 CASE 418BA

### Description

This SiC FET device is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gatedrive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-263-7 package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive.

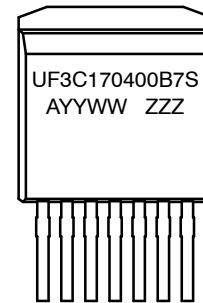
### Features

- On-resistance  $R_{DS(on)}$ : 410 m $\Omega$  (Typ)
- Operating Temperature: 175 °C (Max)
- Excellent Reverse Recovery:  $Q_{rr}$  = 70 nC
- Low Body Diode  $V_{FSD}$ : 1.5 V
- Low Gate Charge:  $Q_G$  = 23.1 nC
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2 and CDM Class C3
- This Device is Halogen Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

### Typical Applications

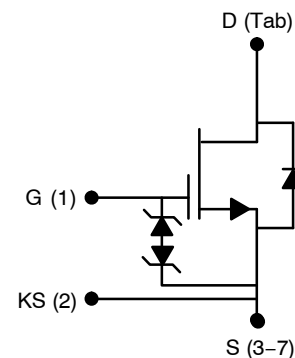
- Switching Power Supplies
- Auxiliary Power Supplies
- Load Switches

### MARKING DIAGRAM



UF3C170400B7S = Specific Device Code  
 A = Assembly Location  
 YY = Year  
 WW = Work Week  
 ZZZ = Lot ID

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

# UF3C170400B7S

## MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	$V_{DS}$		1700	V
Gate-source Voltage	$V_{GS}$	DC	-25 to +25	V
Continuous Drain Current (Note 1)	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	7.6	A
		$T_C = 100\text{ }^\circ\text{C}$	5.9	A
Pulsed Drain Current (Note 2)	$I_{DM}$	$T_C = 25\text{ }^\circ\text{C}$	14	A
Single Pulsed Avalanche Energy (Note 3)	$E_{AS}$	$L = 15\text{ mH}$ , $I_{AS} = 1.25\text{ A}$	11.7	mJ
Power Dissipation	$P_{tot}$	$T_C = 25\text{ }^\circ\text{C}$	100	W
Maximum Junction Temperature	$T_{J, max}$		175	$^\circ\text{C}$
Operating and Storage Temperature	$T_J$ , $T_{STG}$		-55 to 175	$^\circ\text{C}$
Reflow Soldering Temperature	$T_{solder}$	Reflow MSL 1	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by  $T_{J, max}$ .
2. Pulse width  $t_p$  limited by  $T_{J, max}$ .
3. Starting  $T_J = 25\text{ }^\circ\text{C}$ .

## THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	1.2	1.5	$^\circ\text{C/W}$

# UF3C170400B7S

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>TYPICAL PERFORMANCE – STATIC</b>						
Drain-source Breakdown Voltage	BV <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	1700	–	–	V
Total Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 1700 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 25 °C	–	1.5	60	μA
		V <sub>DS</sub> = 1700 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	–	5.5	–	
Total Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, T <sub>J</sub> = 25 °C, V <sub>GS</sub> = -20 V / +20 V	–	6	±20	μA
Drain-source On-resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 12 V, I <sub>D</sub> = 5 A, T <sub>J</sub> = 25 °C	–	410	515	mΩ
		V <sub>GS</sub> = 12 V, I <sub>D</sub> = 5 A, T <sub>J</sub> = 125 °C	–	780	–	
		V <sub>GS</sub> = 12 V, I <sub>D</sub> = 5 A, T <sub>J</sub> = 175 °C	–	1070	–	
Gate Threshold Voltage	V <sub>G(th)</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 10 mA	3	4.7	6	V
Gate Resistance	R <sub>G</sub>	f = 1 MHz, open drain	–	4.1	–	Ω

## TYPICAL PERFORMANCE – REVERSE DIODE

Diode Continuous Forward Current (Note 1)	I <sub>S</sub>	T <sub>C</sub> = 25 °C	–	–	7.6	A
Diode Pulse Current (Note 2)	I <sub>S, pulse</sub>	T <sub>C</sub> = 25 °C	–	–	14	A
Forward Voltage	V <sub>FSD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2 A, T <sub>J</sub> = 25 °C	–	1.5	1.75	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2 A, T <sub>J</sub> = 175 °C	–	2.4	–	
Reverse Recovery Charge	Q <sub>rr</sub>	V <sub>DS</sub> = 1200 V, I <sub>S</sub> = 5 A, V <sub>GS</sub> = -5 V, R <sub>G, EXT</sub> = 10 Ω, di/dt = 4000 A/μs, T <sub>J</sub> = 25 °C	–	70	–	nC
Reverse Recovery Time	t <sub>rr</sub>		–	29	–	ns
Reverse Recovery Charge	Q <sub>rr</sub>	V <sub>DS</sub> = 1200 V, I <sub>S</sub> = 5 A, V <sub>GS</sub> = -5 V, R <sub>G, EXT</sub> = 10 Ω, di/dt = 4000 A/μs, T <sub>J</sub> = 150 °C	–	67	–	nC
Reverse Recovery Time	t <sub>rr</sub>		–	27	–	ns

## TYPICAL PERFORMANCE – DYNAMIC

Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 1200 V, V <sub>GS</sub> = 0 V, f = 100 kHz	–	734	–	pF
Output Capacitance	C <sub>oss</sub>		–	13.6	–	
Reverse Transfer Capacitance	C <sub>rss</sub>		–	2	–	
Effective Output Capacitance, Energy Related	C <sub>oss(er)</sub>	V <sub>DS</sub> = 0 V to 1200 V, V <sub>GS</sub> = 0 V	–	15.5	–	pF
Effective Output Capacitance, Time Related	C <sub>oss(tr)</sub>		–	28	–	
C <sub>OSS</sub> Stored Energy	E <sub>oss</sub>	V <sub>DS</sub> = 1200 V, V <sub>GS</sub> = 0 V	–	11.2	–	μJ
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> = 1200 V, I <sub>D</sub> = 5 A, V <sub>GS</sub> = 0 V to 15 V	–	23.1	–	nC
Gate-drain Charge	Q <sub>GD</sub>		–	6.5	–	
Gate-source Charge	Q <sub>GS</sub>		–	5.6	–	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> = 1200 V, I <sub>D</sub> = 5 A, Gate Driver = 0 V to +15 V, R <sub>G, EXT</sub> = 50 Ω, Inductive Load, FWD: 2x UJ3D1202TS in series, T <sub>J</sub> = 25 °C	–	43	–	ns
Rise Time	t <sub>r</sub>		–	16	–	
Turn-off Delay Time	t <sub>d(off)</sub>		–	102	–	
Fall Time	t <sub>f</sub>		–	27.5	–	
Turn-on Energy	E <sub>ON</sub>		–	143	–	μJ
Turn-off Energy	E <sub>OFF</sub>		–	29	–	
Total Switching Energy	E <sub>TOTAL</sub>		–	172	–	

# UF3C170400B7S

## ELECTRICAL CHARACTERISTICS ( $T_J = +25\text{ }^\circ\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>TYPICAL PERFORMANCE - DYNAMIC</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 1200\text{ V}$ , $I_D = 5\text{ A}$ , Gate Driver = 0 V to +15 V, $R_{G,EXT} = 50\ \Omega$ , Inductive Load, FWD: 2x UJ3D1202TS in series, $T_J = 150\text{ }^\circ\text{C}$	-	33	-	ns
Rise Time	$t_r$		-	15	-	
Turn-off Delay Time	$t_{d(off)}$		-	99	-	
Fall Time	$t_f$		-	35	-	
Turn-on Energy	$E_{ON}$		-	127	-	$\mu\text{J}$
Turn-off Energy	$E_{OFF}$		-	27	-	
Total Switching Energy	$E_{TOTAL}$		-	154	-	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAMS

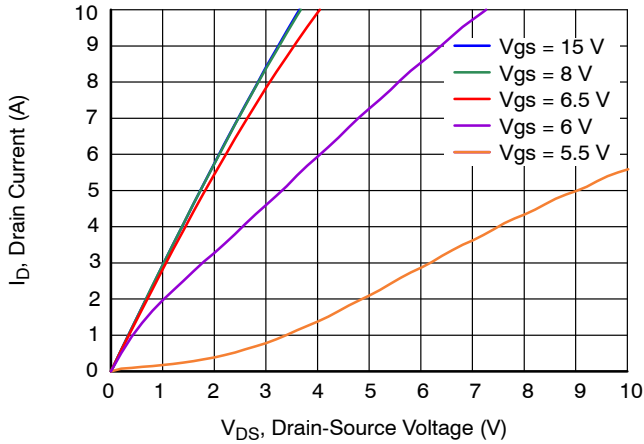


Figure 1. Typical Output Characteristics at  $T_J = -55^\circ\text{C}$ ,  $t_p < 250\ \mu\text{s}$

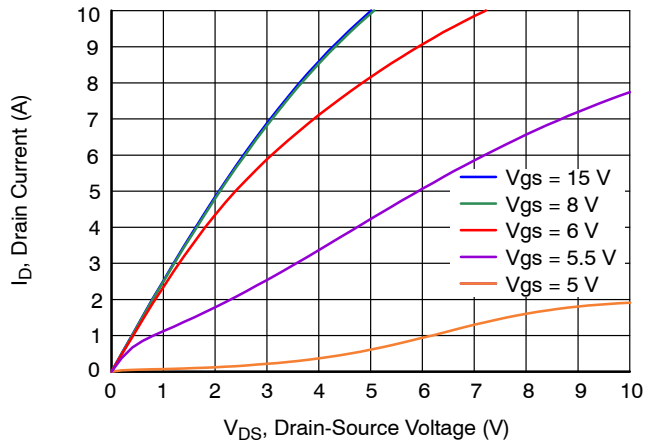


Figure 2. Typical Output Characteristics at  $T_J = 25^\circ\text{C}$ ,  $t_p < 250\ \mu\text{s}$

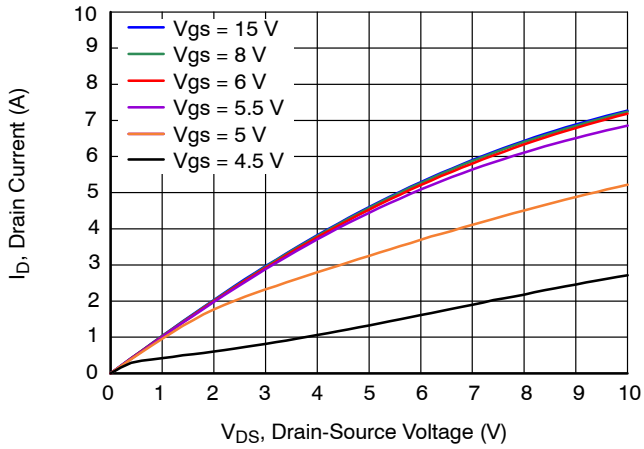


Figure 3. Typical Output Characteristics at  $T_J = 175^\circ\text{C}$ ,  $t_p < 250\ \mu\text{s}$

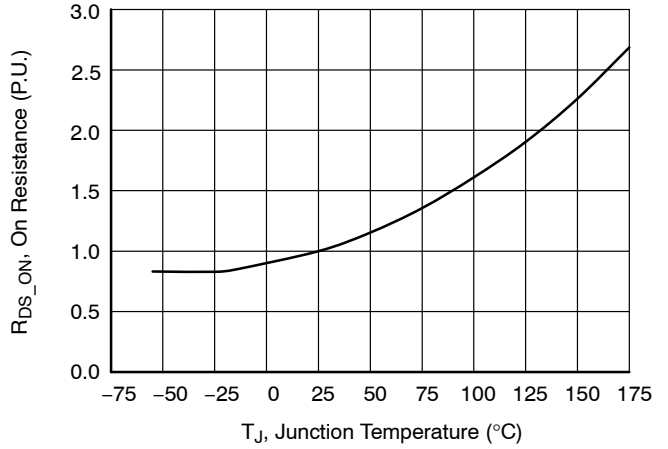


Figure 4. Normalized On-Resistance vs. Temperature at  $V_{GS} = 12\ \text{V}$  and  $I_D = 5\ \text{A}$

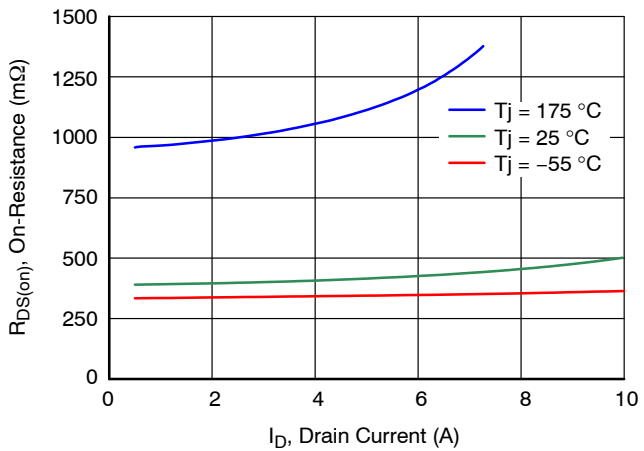


Figure 5. Typical Drain-Source On-Resistances at  $V_{GS} = 12\ \text{V}$

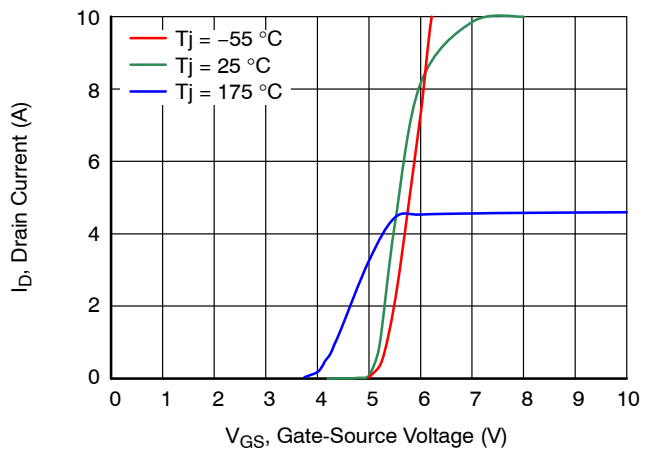


Figure 6. Typical Transfer Characteristics at  $V_{DS} = 5\ \text{V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

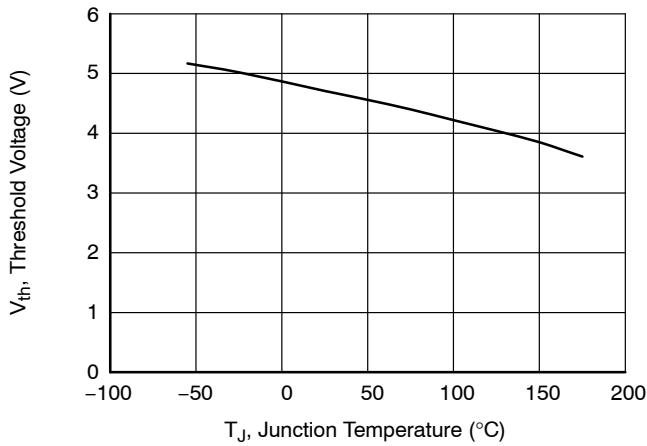


Figure 7. Threshold Voltage vs. Junction Temperature at  $V_{DS} = 5\text{ V}$  and  $I_D = 10\text{ mA}$

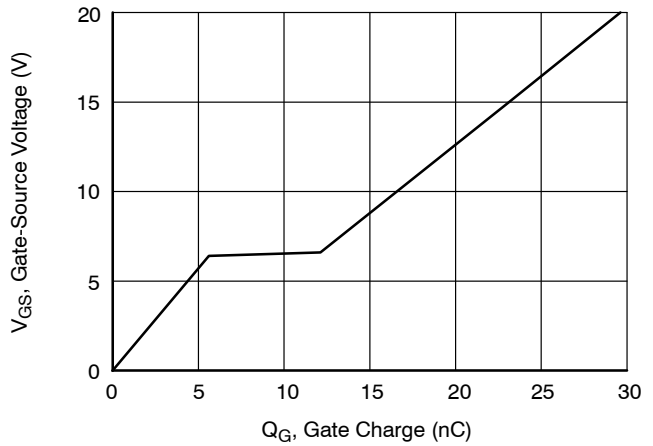


Figure 8. Typical Gate Charge at  $V_{DS} = 1200\text{ V}$  and  $I_D = 5\text{ A}$

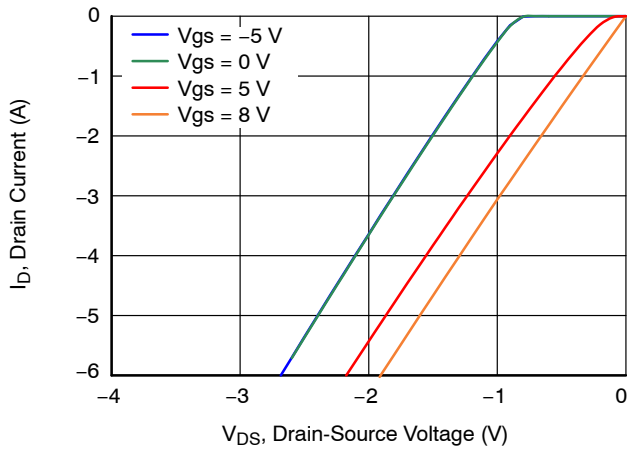


Figure 9. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = -55\text{ °C}$

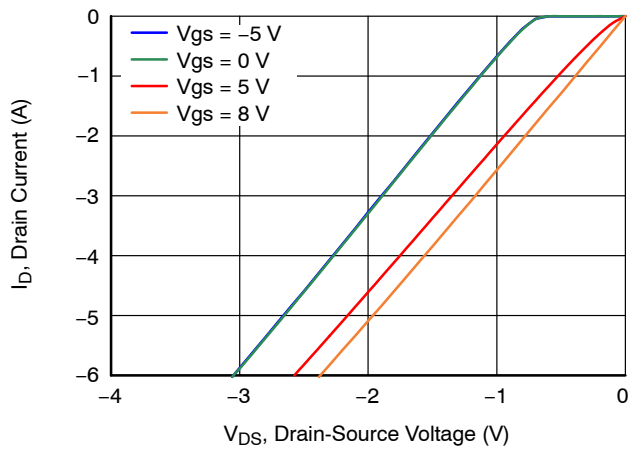


Figure 10. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 25\text{ °C}$

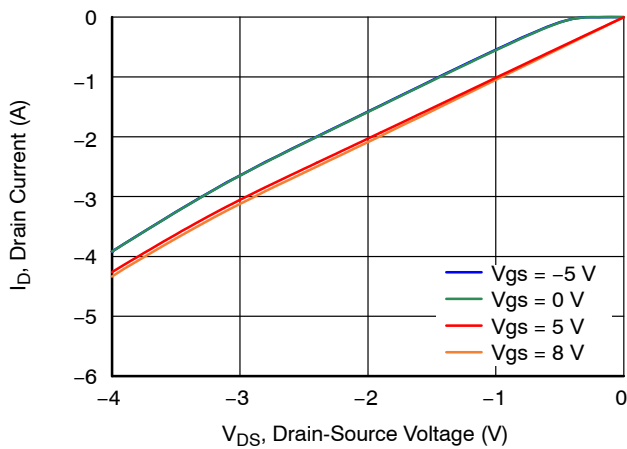


Figure 11. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 175\text{ °C}$

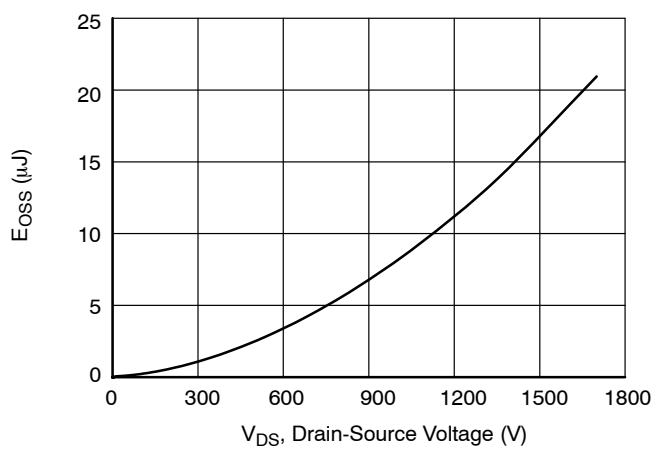


Figure 12. Typical Stored Energy in  $C_{OSS}$  at  $V_{GS} = 0\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

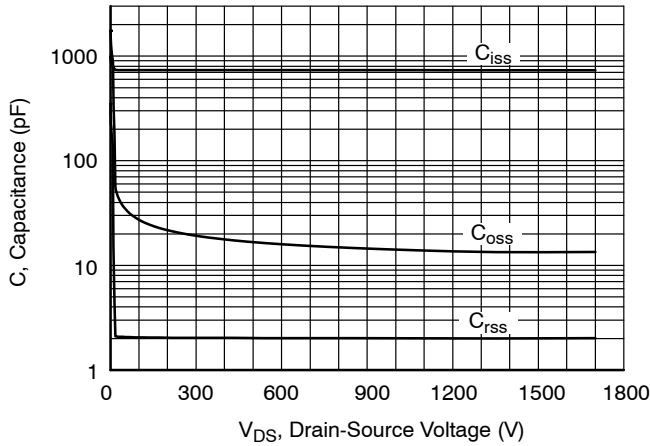


Figure 13. Typical Capacitances at  $f = 100 \text{ kHz}$  and  $V_{GS} = 0 \text{ V}$

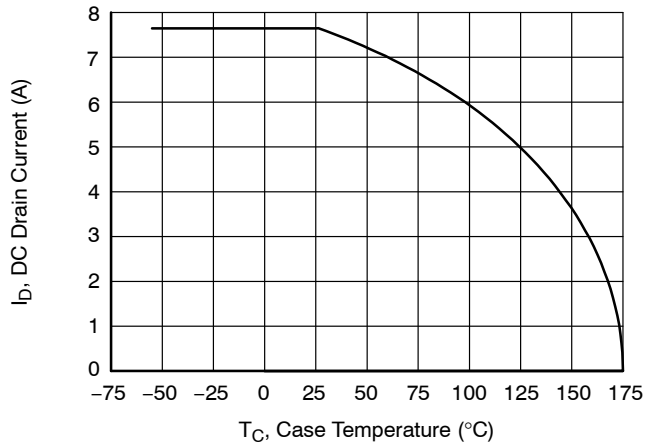


Figure 14. DC Drain Current Derating

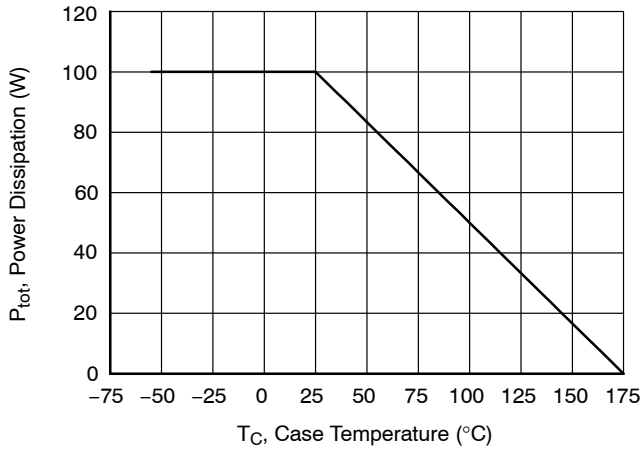


Figure 15. Total Power Dissipation

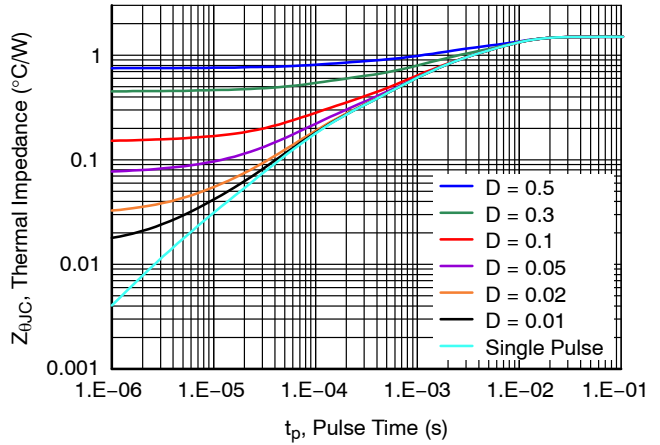


Figure 16. Maximum Transient Thermal Impedance

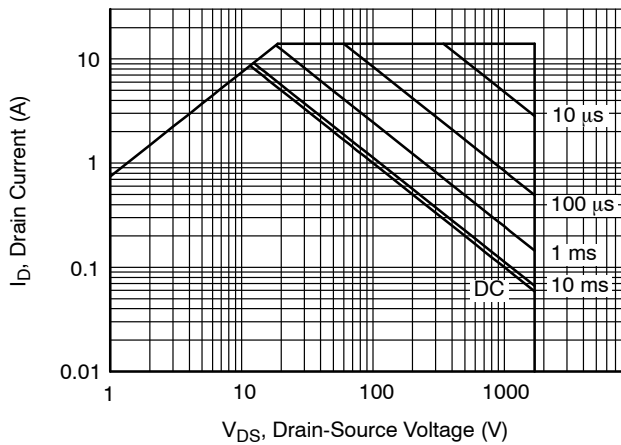


Figure 17. Safe Operation Area at  $T_C = 25 \text{ }^\circ\text{C}$ ,  $D = 0$ , Parameter  $t_p$

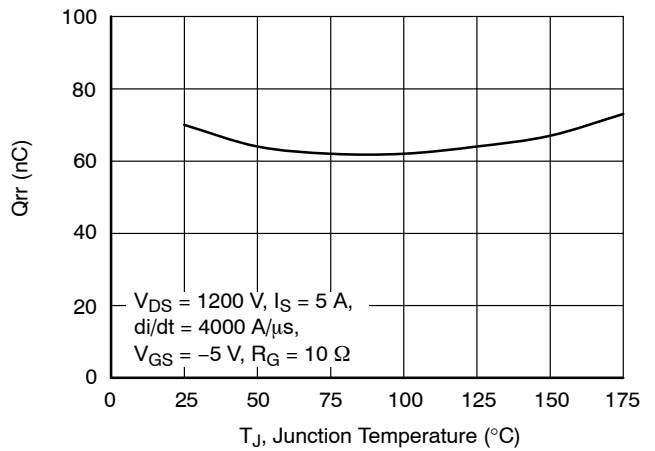


Figure 18. Reverse Recovery Charge  $Q_{rr}$  vs. Junction Temperature

TYPICAL PERFORMANCE DIAGRAMS (continued)

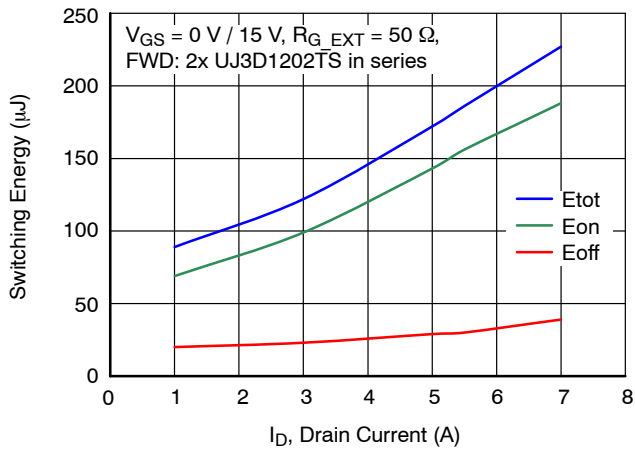


Figure 19. Clamped Inductive Switching Energy vs. Drain Current at  $V_{DS} = 1200\text{ V}$  and  $T_J = 25\text{ }^\circ\text{C}$

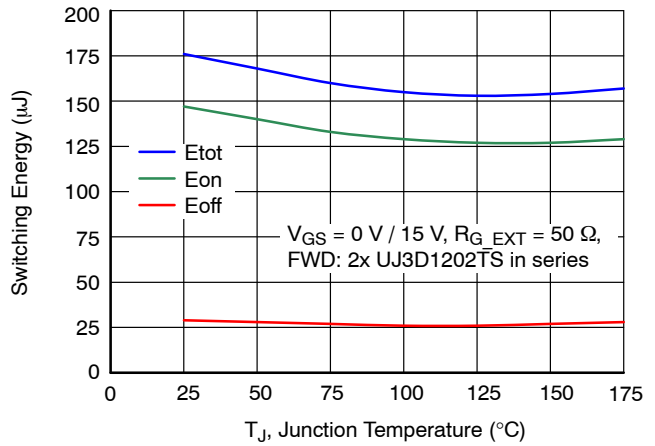


Figure 20. Clamped Inductive Switching Energy vs. Junction Temperature at  $V_{DS} = 1200\text{ V}$ , and  $I_D = 5\text{ A}$

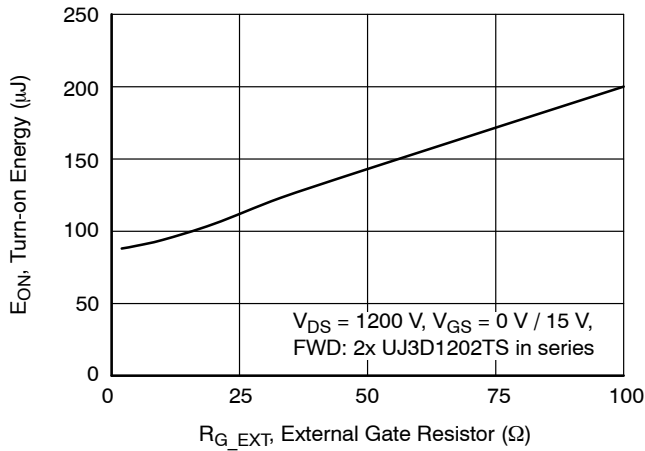


Figure 21. Clamped Inductive Switching Turn-on Energy vs. Gate Resistor  $R_{G\_EXT}$

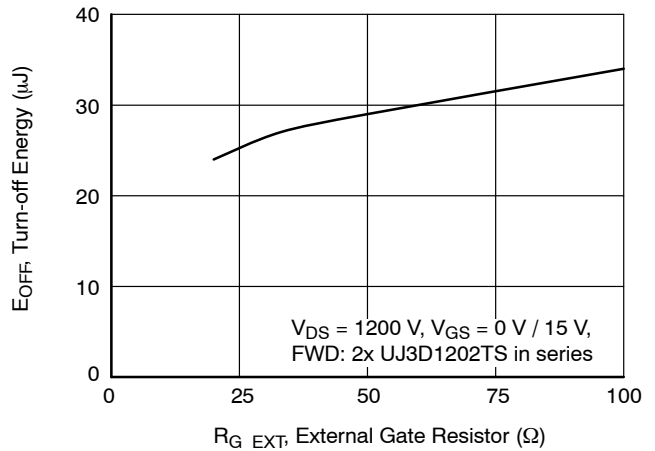


Figure 22. Clamped Inductive Switching Turn-off Energy vs. Gate Resistor  $R_{G\_EXT}$



APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

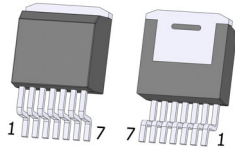
Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see [www.onsemi.com](http://www.onsemi.com).

A snubber circuit with a small  $R_{(G)}$ , or gate resistor, provides better EMI suppression with higher efficiency compared to using a high  $R_{(G)}$  value. There is no extra gate delay time when using the snubber circuitry, and a small  $R_{(G)}$  will better control both the turn-off  $V_{(DS)}$  peak spike and ringing duration, while a high  $R_{(G)}$  will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high  $R_{(G)}$ , while greatly reducing  $E_{(OFF)}$  from mid-to-full load range with only a small increase in  $E_{(ON)}$ . Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at [www.onsemi.com](http://www.onsemi.com)

ORDERING INFORMATION

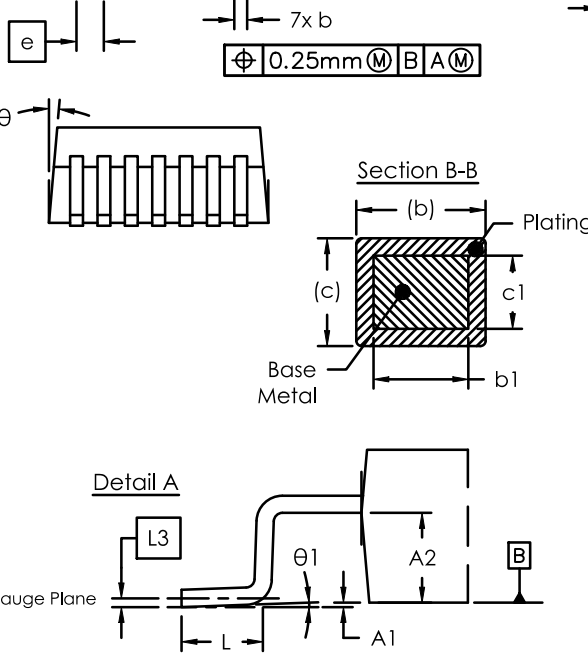
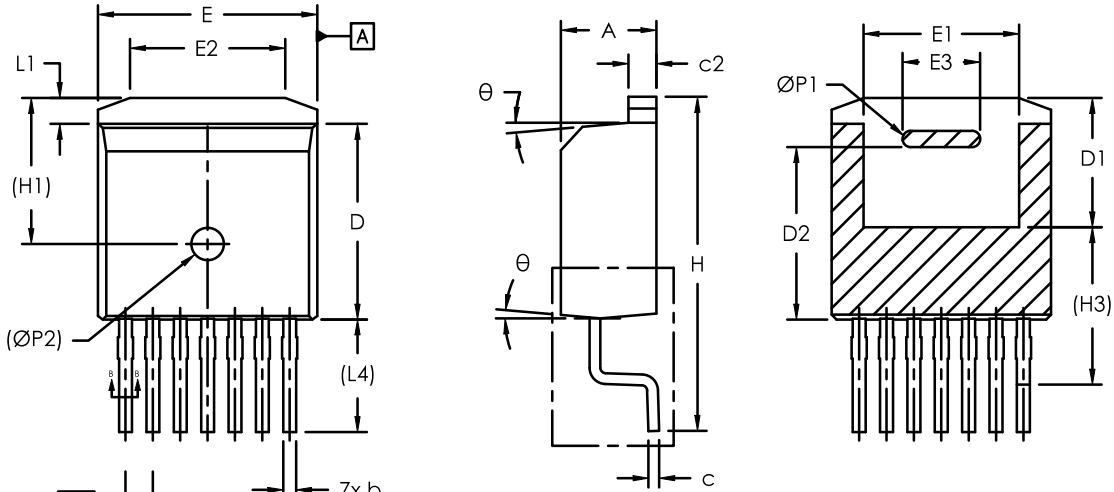
Part Number	Marking	Package	Shipping <sup>†</sup>
UF3C170400B7S	UF3C170400B7S	TO-263-7	800 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](http://www.onsemi.com).



TO-263-7 10.18x9.08x4.43, 1.27P  
CASE 418BA  
ISSUE B

DATE 17 APR 2025



SYM	MILLIMETERS		
	Min	Nom	Max
A	4.30	4.43	4.56
A1	0.00	0.13	0.25
A2	2.45	2.60	2.75
b	0.50	0.60	0.70
b1	0.50	-	-
c	0.40	0.50	0.60
c1	0.40	-	-
c2	1.20	1.30	1.40
D	8.93	9.08	9.23
D1	5.85	6.00	6.15
D2	7.90	8.00	8.10
e	1.27 BSC		
E	10.08	10.18	10.28
E1	6.82	7.22	7.62
E2	6.50	7.55	8.60
E3	3.50	3.60	3.70
H	15.00	15.50	16.00
H1	6.78 REF		
H3	7.30 REF.		
L	1.90	2.20	2.50
L1	0.98	1.20	1.42
L3	0.25 BSC		
L4	5.22 REF		
ØP1	0.65	0.75	0.85
ØP2	1.50 REF		
θ	5°		
θ1	3°		

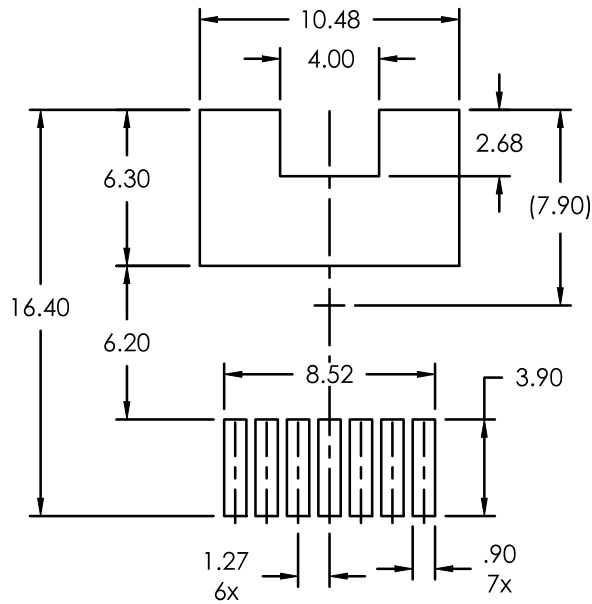
Notes:

1. Dimensioning and Tolerancing as per ASME Y14.5M, 2018.
2. Controlling Dimension : Millimeters
3. Package body sides exclude mold flash and gate burrs.
4. Dimension L is measured on gauge plane.
5. Dimension c1 and b1 applies to base metal only.

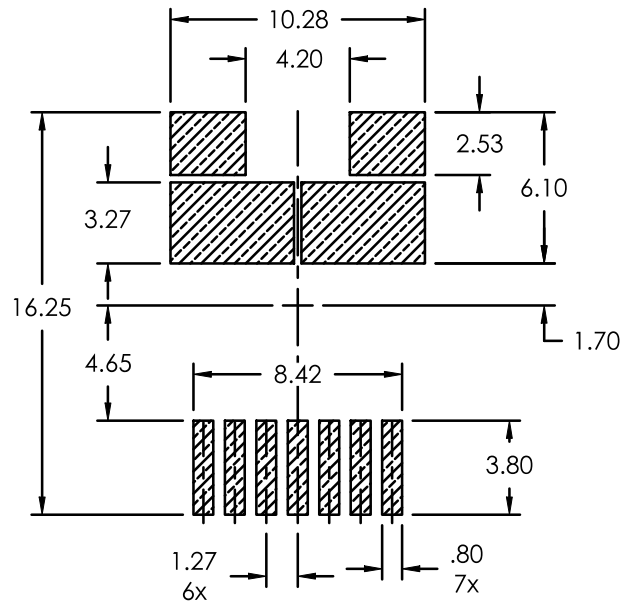
<b>DOCUMENT NUMBER:</b>	<b>98AON13800G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TO-263-7 10.18x9.08x4.43, 1.27P</b>	<b>PAGE 1 OF 2</b>

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RECOMMENDED PCB FOOTPRINT

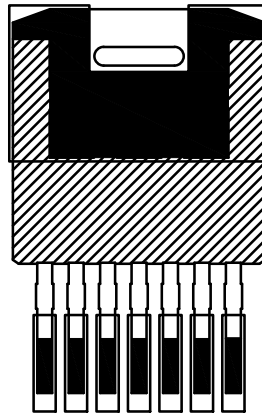


RECOMMENDED STENCIL APERTURE



NOTE: LAND PATTERN AND STENCIL APERTURE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE. END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

PCB FOOTPRINT with PACKAGE OVERLAY



- AREA IN CONTACT WITH THE PACKAGE
- MOLD COMPOUND

<b>DOCUMENT NUMBER:</b>	<b>98AON13800G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TO-263-7 10.18x9.08x4.43, 1.27P</b>	<b>PAGE 2 OF 2</b>

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