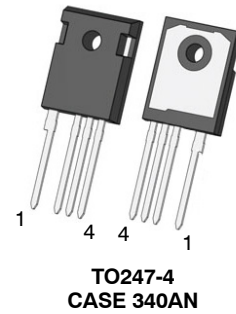


Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO247-4, 650 V, 6.7 mohm

UF3SC065007K4S



Description

This SiC FET device is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO247-4 package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive.

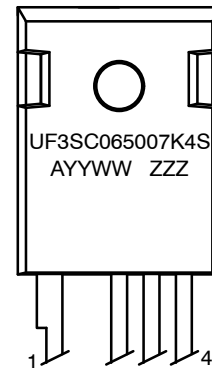
Features

- Typical On-resistance $R_{DS(on),typ}$ of 6.7 m Ω
- Maximum Operating Temperature of 175 °C
- Excellent Reverse Recovery
- Low Gate Charge
- Low Intrinsic Capacitance
- ESD Protected, HBM Class 2
- TO247-4 Package for Faster Switching, Clean Gate Waveforms
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Typical Applications

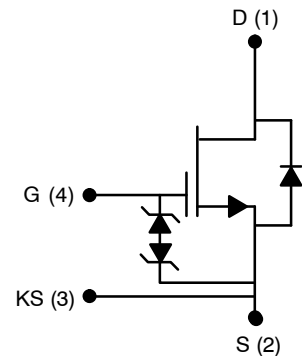
- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

MARKING DIAGRAM



UF3SC065007K4S = Specific Device Code
 A = Assembly Location
 YY = Year
 WW = Work Week
 ZZZ = Lot Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

UF3SC065007K4S

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		650	V
Gate-source Voltage	V_{GS}	DC	-20 to +20	V
Continuous Drain Current (Note 1)	I_D	$T_C < 135\text{ }^\circ\text{C}$	120	A
Pulsed Drain Current (Note 2)	I_{DM}	$T_C = 25\text{ }^\circ\text{C}$	550	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	$L = 15\text{ mH}, I_{AS} = 8.6\text{ A}$	555	mJ
Power Dissipation	P_{tot}	$T_C = 25\text{ }^\circ\text{C}$	789	W
Maximum Junction Temperature	$T_{J, max}$		175	$^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Max. Lead Temperature for Soldering, 1/8" from Case for 5 seconds	T_L		250	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by bondwires.
2. Pulse width t_p limited by $T_{J, max}$.
3. Starting $T_J = 25\text{ }^\circ\text{C}$.

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	0.15	0.19	$^\circ\text{C/W}$

UF3SC065007K4S

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC						
Drain-source Breakdown Voltage	BV _{DS}	V _{GS} = 0 V, I _D = 1 mA	650	–	–	V
Total Drain Leakage Current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V, T _J = 25 °C	–	7	600	μA
		V _{DS} = 650 V, V _{GS} = 0 V, T _J = 175 °C	–	70	–	
Total Gate Leakage Current	I _{GSS}	V _{DS} = 0 V, T _J = 25 °C, V _{GS} = -20 V / +20 V	–	5	±20	μA
Drain-source On-resistance	R _{DS(on)}	V _{GS} = 12 V, I _D = 50 A, T _J = 25 °C	–	6.7	9	mΩ
		V _{GS} = 12 V, I _D = 50 A, T _J = 125 °C	–	8.8	–	
		V _{GS} = 12 V, I _D = 50 A, T _J = 175 °C	–	11	–	
Gate Threshold Voltage	V _{G(th)}	V _{DS} = 5 V, I _D = 10 mA	4	4.7	6	V
Gate Resistance	R _G	f = 1 MHz, open drain	–	0.8	1.5	Ω

TYPICAL PERFORMANCE – REVERSE DIODE

Diode Continuous Forward Current (Note 1)	I _S	T _C < 135 °C	–	–	120	A
Diode Pulse Current (Note 2)	I _{S, pulse}	T _C = 25 °C	–	–	550	A
Forward Voltage	V _{FSD}	V _{GS} = 0 V, I _S = 80 A, T _J = 25 °C	–	1.31	1.5	V
		V _{GS} = 0 V, I _S = 80 A, T _J = 175 °C	–	1.4	–	
Reverse Recovery Charge	Q _{rr}	V _{DS} = 400 V, I _S = 80 A, V _{GS} = -5 V, R _{G, EXT} = 10 Ω, di/dt = 1400 A/μs, T _J = 25 °C	–	856	–	nC
Reverse Recovery Time	t _{rr}		–	53	–	ns
Reverse Recovery Charge	Q _{rr}	V _{DS} = 400 V, I _S = 80 A, V _{GS} = -5 V, R _{G, EXT} = 10 Ω, di/dt = 1400 A/μs, T _J = 150 °C	–	865	–	nC
Reverse Recovery Time	t _{rr}		–	35	–	ns

TYPICAL PERFORMANCE – DYNAMIC

Input Capacitance	C _{iss}	V _{DS} = 100 V, V _{GS} = 0 V, f = 100 kHz	–	8360	–	pF	
Output Capacitance	C _{oss}		–	1190	–		
Reverse Transfer Capacitance	C _{rss}		–	11.3	–		
Effective Output Capacitance, Energy Related	C _{oss(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	856	–	pF	
Effective Output Capacitance, Time Related	C _{oss(tr)}		–	1806	–	pF	
C _{OSS} Stored Energy	E _{oss}	V _{DS} = 400 V, V _{GS} = 0 V	–	69	–	μJ	
Total Gate Charge	Q _G	V _{DS} = 400 V, I _D = 80 A, V _{GS} = -5 V to 15 V	–	214	–	nC	
Gate-drain Charge	Q _{GD}		–	28	–		
Gate-source Charge	Q _{GS}		–	96	–		
Turn-on Delay Time	t _{d(on)}	V _{DS} = 400 V, I _D = 80 A, Gate Driver = -5 V to +15 V, Turn-on R _{G, EXT} = 1.5 Ω, Turn-off R _{G, EXT} = 5 Ω, Inductive Load, FWD: same device with V _{GS} = -5 V, R _G = 10 Ω, T _J = 25 °C	–	36	–	ns	
Rise Time	t _r		–	46	–		
Turn-off Delay Time	t _{d(off)}		–	72	–		
Fall Time	t _f		–	14	–		
Turn-on Energy	E _{ON}			–	925	–	μJ
Turn-off Energy	E _{OFF}			–	83	–	
Total Switching Energy	E _{TOTAL}			–	1008	–	
Turn-on Delay Time	t _{d(on)}		V _{DS} = 400 V, I _D = 80 A, Gate Driver = -5 V to +15 V, Turn-on R _{G, EXT} = 1.5 Ω, Turn-off R _{G, EXT} = 5 Ω, Inductive Load, FWD: same device with V _{GS} = -5 V, R _G = 10 Ω, T _J = 150 °C	–	38	–	ns
Rise Time	t _r			–	47	–	
Turn-off Delay Time	t _{d(off)}			–	75	–	
Fall Time	t _f	–		14	–		
Turn-on Energy	E _{ON}			–	1081	–	μJ
Turn-off Energy	E _{OFF}			–	105	–	
Total Switching Energy	E _{TOTAL}			–	1186	–	

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ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
TYPICAL PERFORMANCE - DYNAMIC							
Turn-on Delay Time	t _{d(on)}	V _{DS} = 400 V, I _D = 80 A, Gate Driver = -5 V to +15 V, Turn-on R _{G, EXT} = 1.5 Ω, Turn-off R _{G, EXT} = 5 Ω, Inductive Load, FWD: UJ3D065030TS T _J = 25 °C	-	36	-	ns	
Rise Time	t _r		-	37	-		
Turn-off Delay Time	t _{d(off)}		-	72	-		
Fall Time	t _f			-	14	-	
Turn-on Energy	E _{ON}			-	545	-	μJ
Turn-off Energy	E _{OFF}			-	82	-	
Total Switching Energy	E _{TOTAL}			-	627	-	
Turn-on Delay Time	t _{d(on)}	V _{DS} = 400 V, I _D = 80 A, Gate Driver = -5 V to +15 V, Turn-on R _{G, EXT} = 1.5 Ω, Turn-off R _{G, EXT} = 5 Ω, Inductive Load, FWD: UJ3D065030TS T _J = 150 °C	-	34	-	ns	
Rise Time	t _r		-	40	-		
Turn-off Delay Time	t _{d(off)}		-	79	-		
Fall Time	t _f			-	14	-	
Turn-on Energy	E _{ON}			-	555	-	μJ
Turn-off Energy	E _{OFF}			-	84	-	
Total Switching Energy	E _{TOTAL}			-	639	-	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAMS

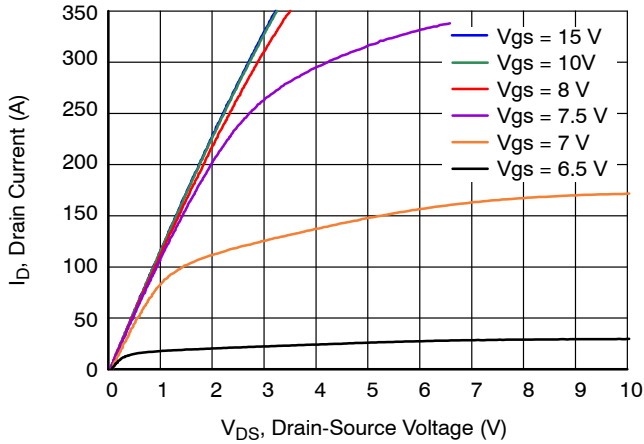


Figure 1. Typical Output Characteristics at $T_J = -55\text{ }^\circ\text{C}$, $t_p < 250\text{ }\mu\text{s}$

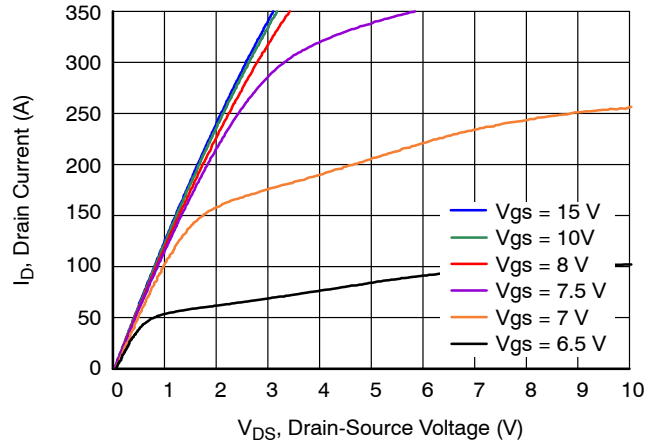


Figure 2. Typical Output Characteristics at $T_J = 25\text{ }^\circ\text{C}$, $t_p < 250\text{ }\mu\text{s}$

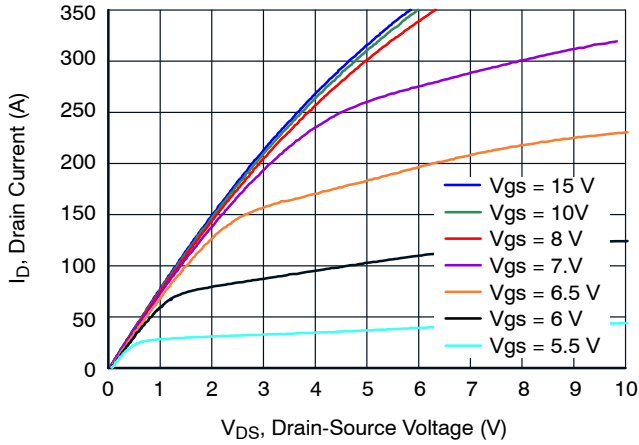


Figure 3. Typical Output Characteristics at $T_J = 175\text{ }^\circ\text{C}$, $t_p < 250\text{ }\mu\text{s}$

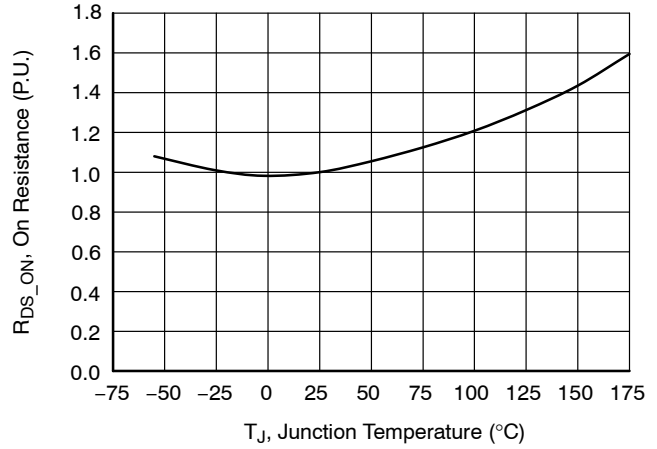


Figure 4. Normalized On-Resistance vs. Temperature at $V_{GS} = 12\text{ V}$ and $I_D = 50\text{ A}$

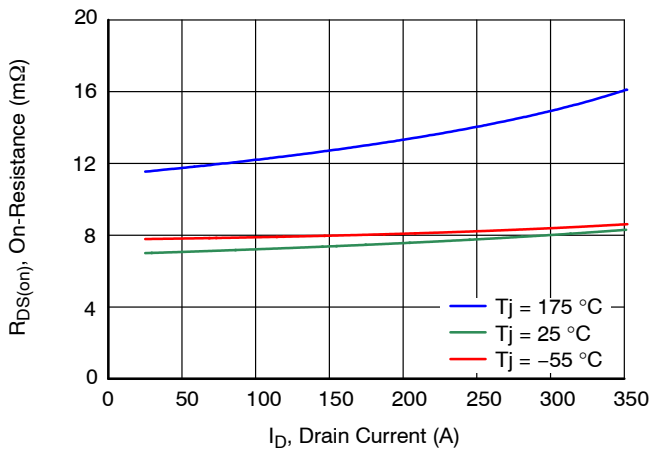


Figure 5. Typical Drain-Source On-Resistances at $V_{GS} = 12\text{ V}$

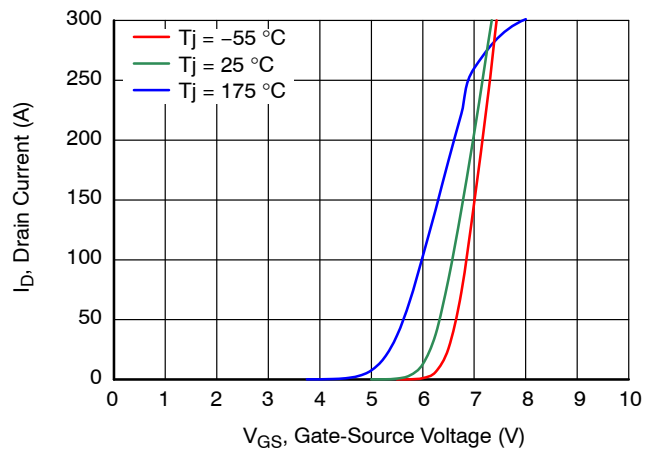


Figure 6. Typical Transfer Characteristics at $V_{DS} = 5\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

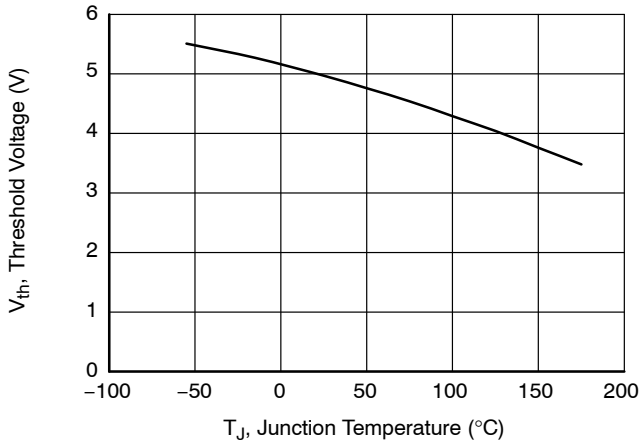


Figure 7. Threshold Voltage vs. Junction Temperature at $V_{DS} = 5\text{ V}$ and $I_D = 10\text{ mA}$

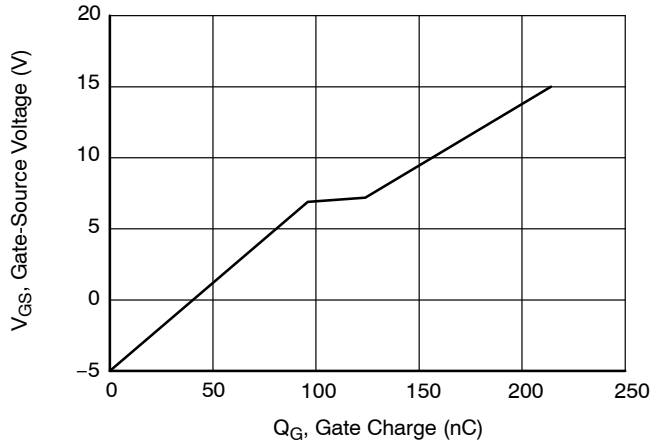


Figure 8. Typical Gate Charge at $V_{DS} = 400\text{ V}$ and $I_D = 80\text{ A}$

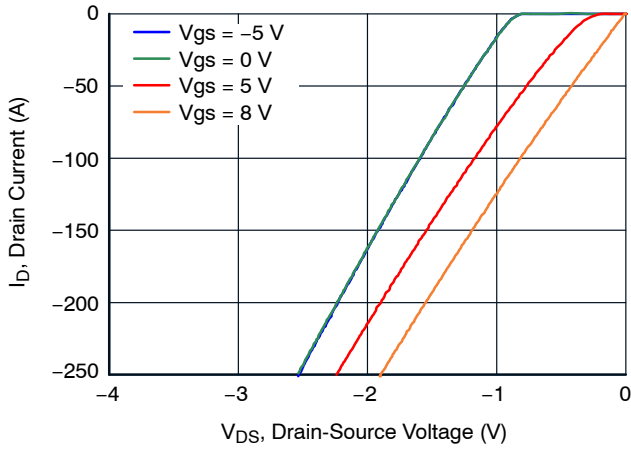


Figure 9. 3rd Quadrant Characteristics at $T_J = -55\text{ °C}$

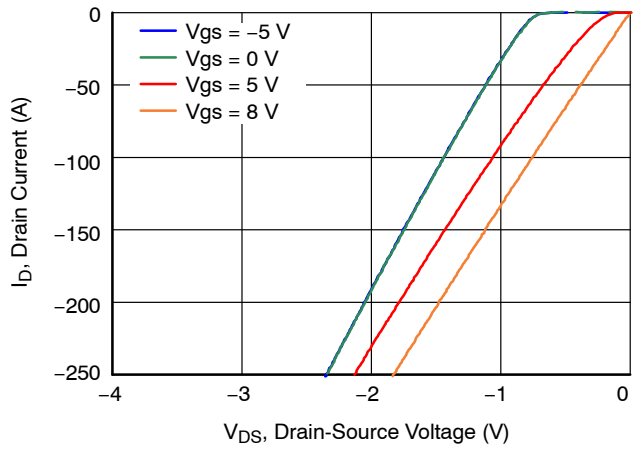


Figure 10. 3rd Quadrant Characteristics at $T_J = 25\text{ °C}$

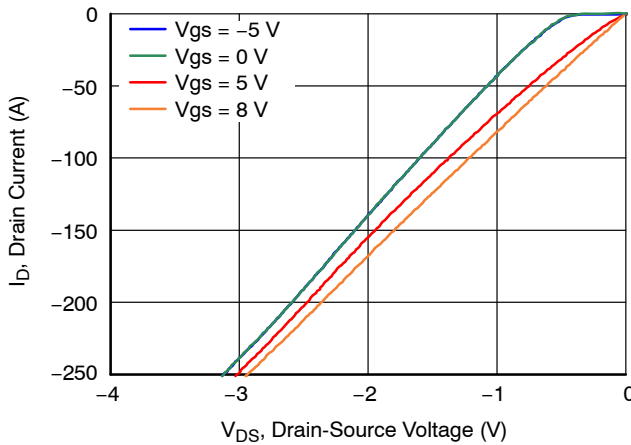


Figure 11. 3rd Quadrant Characteristics at $T_J = 175\text{ °C}$

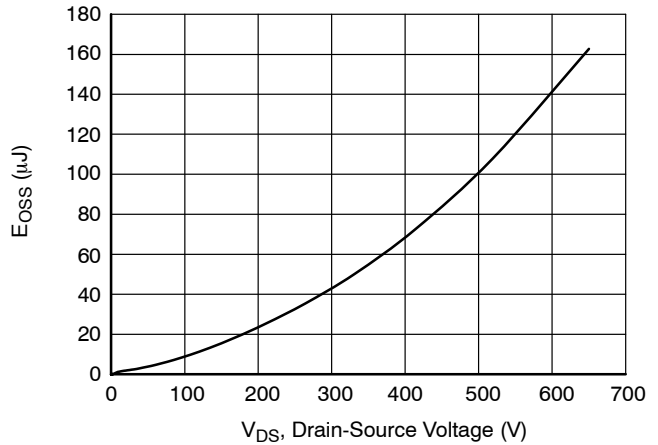


Figure 12. Typical Stored Energy in C_{OSS} at $V_{GS} = 0\text{ V}$

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TYPICAL PERFORMANCE DIAGRAMS (continued)

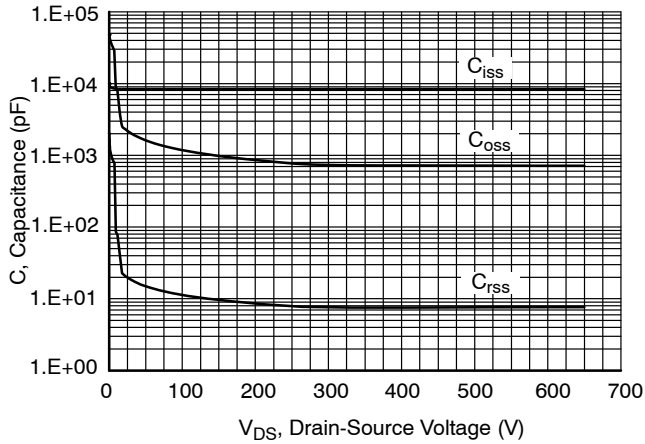


Figure 13. Typical Capacitances at $f = 100 \text{ kHz}$ and $V_{GS} = 0 \text{ V}$

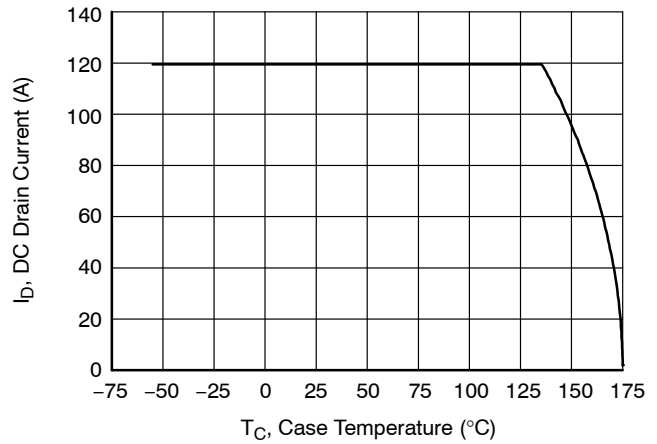


Figure 14. DC Drain Current Derating

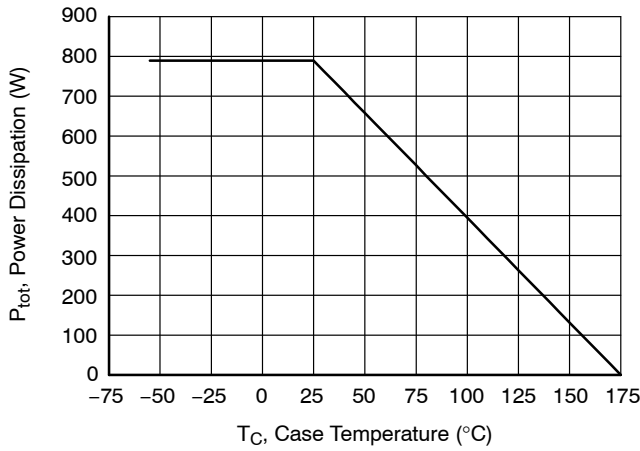


Figure 15. Total Power Dissipation

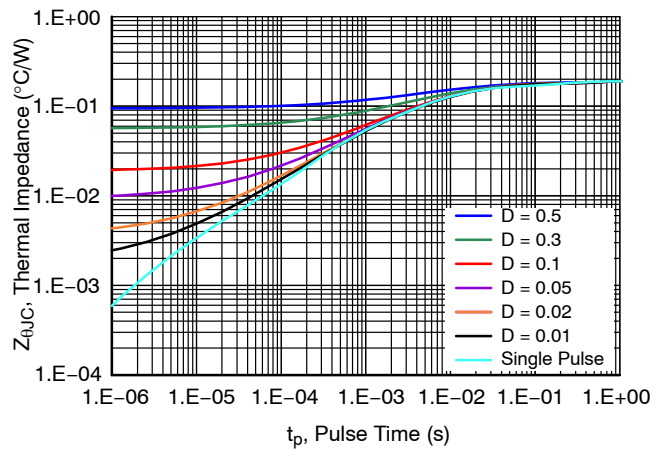


Figure 16. Maximum Transient Thermal Impedance

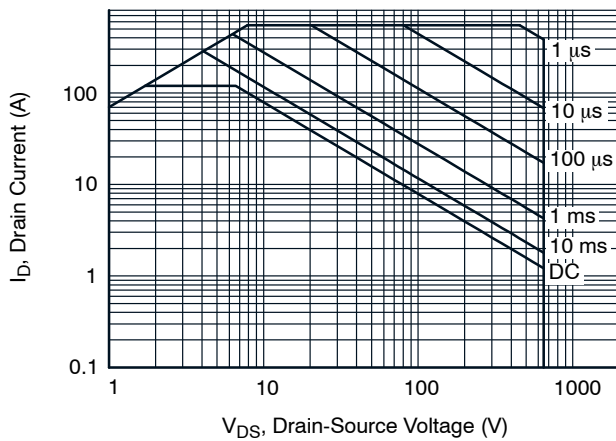


Figure 17. Safe Operation Area at $T_C = 25 \text{ }^\circ\text{C}$, $D = 0$, Parameter t_p

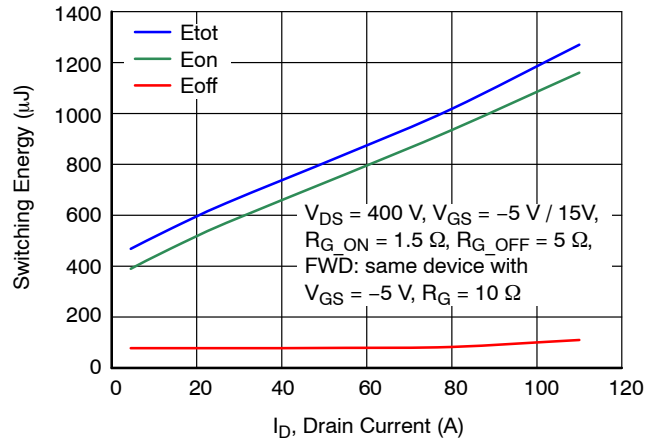


Figure 18. Clamped Inductive Switching Energy vs. Drain Current at $T_J = 25 \text{ }^\circ\text{C}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

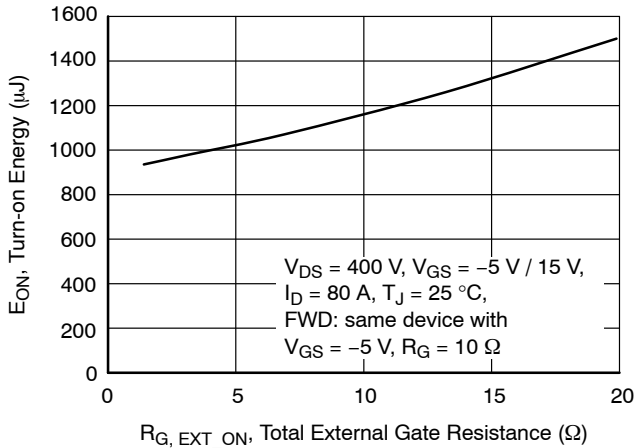


Figure 19. Clamped Inductive Switching Turn-on Energy vs. R_{G, EXT_ON}

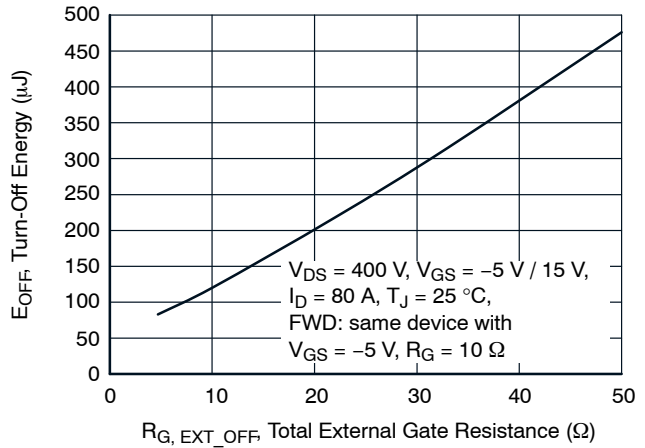


Figure 20. Clamped Inductive Switching Turn-off Energy vs. R_{G, EXT_OFF}

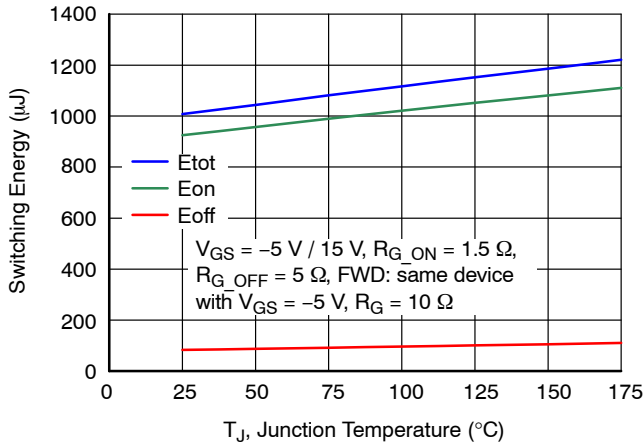


Figure 21. Clamped Inductive Switching Energy vs. Junction Temperature at $V_{DS} = 400\text{ V}$ and $I_D = 80\text{ A}$

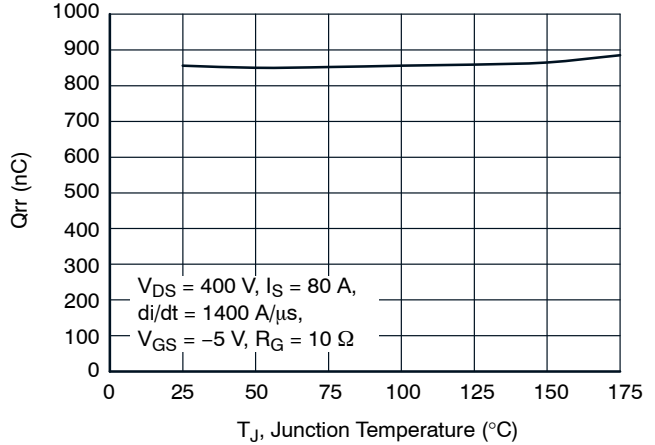


Figure 22. Reverse Recovery Charge Q_{rr} vs. Junction Temperature

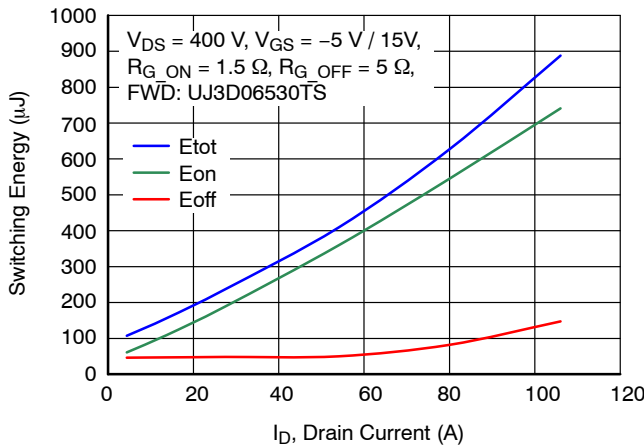


Figure 23. Clamped Inductive Switching Energy vs. Drain Current at $T_J = 25\text{ °C}$

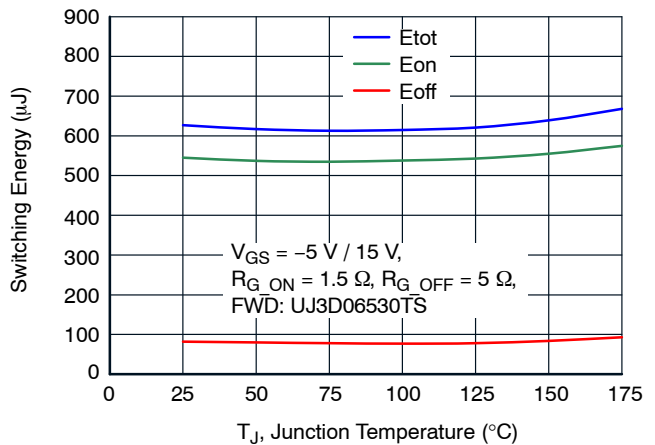


Figure 24. Clamped Inductive Switching Energy vs. Junction Temperature at $V_{DS} = 400\text{ V}$ and $I_D = 80\text{ A}$

UF3SC065007K4S

APPLICATIONS INFORMATION

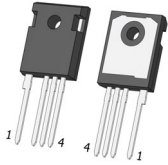
SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses.

The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

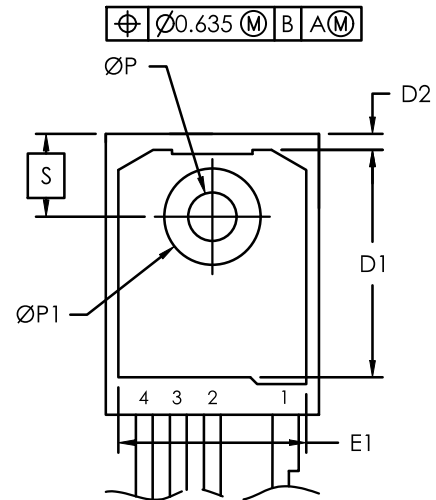
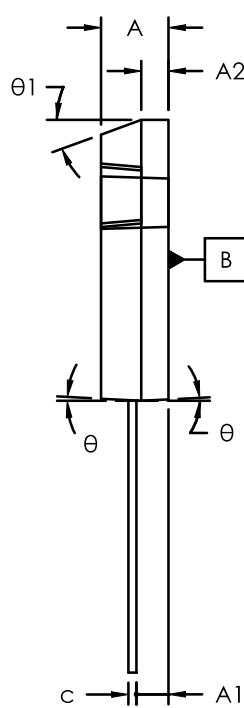
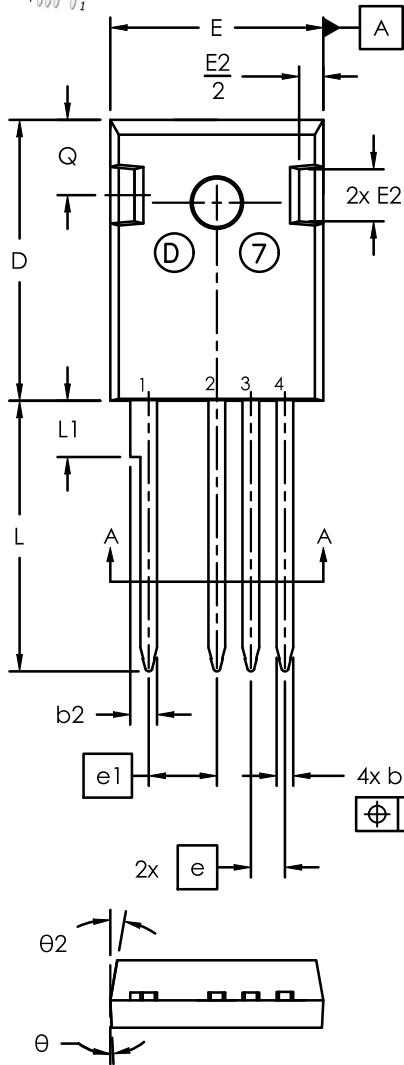
ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UF3SC065007K4S	UF3SC065007K4S	TO247-4	600 Units / Tube



TO247-4 15.90x20.96x5.03, 5.44P
CASE 340AN
ISSUE D

DATE 14 APR 2025



$\text{Ø} \text{Ø}0.254 \text{ (M) B A (M)}$

SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
c	0.38	0.60	0.89
D	20.80	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	2.54 BSC		
e1	5.08 BSC		
E1	13.46	—	—
E2	3.43	3.89	5.20
L	19.81	20.17	20.32
L1	—	—	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.17 BSC		
θ	3°		
θ1	20°		
θ2	10°		

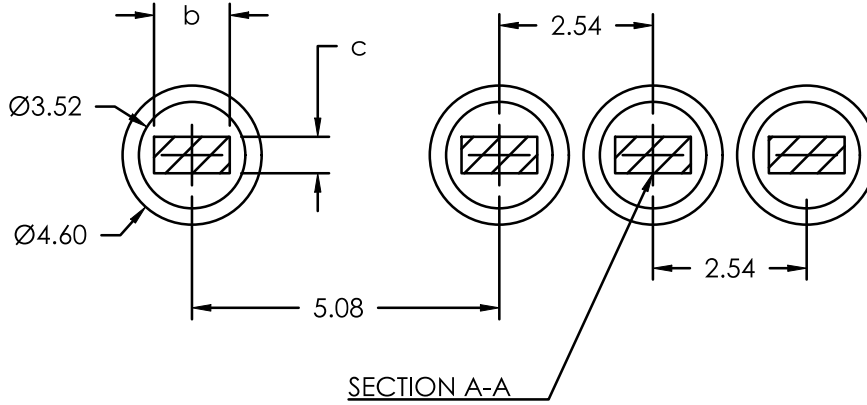
NOTE:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.
5. Through Hole diameter value = End Hole diameter
6. PCB Through Hole pattern as per IPC-2221/IPC-2222

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DESCRIPTION:	TO247-4 15.90x20.96x5.03, 5.44P	PAGE 1 OF 2

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RECOMMENDED PCB THROUGH HOLE



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

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DESCRIPTION:	TO247-4 15.90x20.96x5.03, 5.44P	PAGE 2 OF 2

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