

Silicon Carbide (SiC) JFET – EliteSiC, Power N-Channel, TO247-3, 1200 V, 66 mohm

UJ3N120065K3S

Description

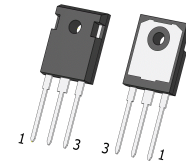
onsemi offers the high-performance G3 SiC normally-on JFET transistors. This series exhibits ultra-low on resistance ($R_{DS(on)}$) and gate charge (Q_G) allowing for low conduction and switching loss. The device normally-on characteristics with low $R_{DS(on)}$ at $V_{GS} = 0$ V is also ideal for current protection circuits without the need for active control, as well as for cascode operation.

Features

- Typical On-resistance $R_{DS(on),typ}$ of 66 m Ω
- Voltage Controlled
- Maximum Operating Temperature of 175 °C
- Extremely Fast Switching not Dependent on Temperature
- Low Gate Charge
- Low Intrinsic Capacitance
- This Device is Pb-Free, Halogen Free and is ROHS Compliant

Typical Applications

- Over Current Protection Circuits
- DC-AC Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating



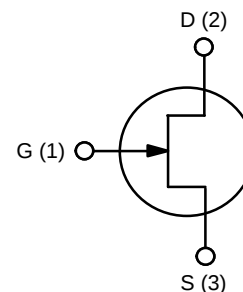
TO247-3
CASE 340AK

MARKING DIAGRAM



UJ3N120065K3S = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week
ZZZ = Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

UJ3N120065K3S

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		1200	V
Gate-source Voltage	V_{GS}	DC	-20 to +3	V
		AC (Note 1)	-30 to +20	V
Continuous Drain Current (Note 2)	I_D	$T_C = 25\text{ }^{\circ}\text{C}$	34	A
		$T_C = 100\text{ }^{\circ}\text{C}$	25	A
Pulsed Drain Current (Note 3)	I_{DM}	$T_C = 25\text{ }^{\circ}\text{C}$	90	A
Power Dissipation	P_{tot}	$T_C = 25\text{ }^{\circ}\text{C}$	254	W
Maximum Junction Temperature	$T_{J,max}$		175	$^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}		-55 to 175	$^{\circ}\text{C}$
Max. Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	T_L		250	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. +20 V AC rating applies for turn-on pulses < 200 ns applied with external $R_G > 1\text{ }\Omega$.
2. Limited by $T_{J,max}$
3. Pulse width t_p limited by $T_{J,max}$

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-case	$R_{\theta JC}$		-	0.45	0.59	$^{\circ}\text{C/W}$

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ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC						
Drain-source Breakdown Voltage	BV _{DS}	V _{GS} = -20 V, I _D = 1 mA	1200	–	–	V
Total Drain Leakage Current	I _{DSS}	V _{DS} = 1200 V, V _{GS} = -20 V, T _J = 25 °C	–	5	30	μA
		V _{DS} = 1200 V, V _{GS} = -20 V, T _J = 175 °C	–	56	–	
Total Gate Leakage Current	I _{GSS}	V _{GS} = -20 V, T _J = 25 °C	–	0.1	50	μA
		V _{GS} = -20 V, T _J = 175 °C	–	1	–	
Drain-source On-resistance	R _{DS(on)}	V _{GS} = 2 V, I _D = 10 A, T _J = 25 °C	–	55	–	mΩ
		V _{GS} = 0 V, I _D = 10 A, T _J = 25 °C	–	66	90	
		V _{GS} = 2 V, I _D = 10 A, T _J = 175 °C	–	122	–	
		V _{GS} = 0 V, I _D = 10 A, T _J = 175 °C	–	142	–	
Gate Threshold Voltage	V _{G(th)}	V _{DS} = 5 V, I _D = 35 mA	-9.3	-6.6	-4.7	V
Gate Resistance	R _G	f = 1 MHz, open drain	–	2.6	–	Ω

TYPICAL PERFORMANCE – DYNAMIC

Input Capacitance	C _{iss}	V _{DS} = 100 V, V _{GS} = -20 V, f = 100 kHz	–	1008	–	pF
Output Capacitance	C _{oss}		–	100	–	
Reverse Transfer Capacitance	C _{rss}		–	95	–	
Effective Output Capacitance, Energy Related	C _{oss(er)}	V _{DS} = 0 V to 800 V, V _{GS} = -20 V	–	56	–	pF
C _{oss} Stored Energy	E _{oss}	V _{DS} = 800 V, V _{GS} = -20 V	–	18	–	μJ
Total Gate Charge	Q _G	V _{DS} = 800 V, I _D = 25 A, V _{GS} = -18 V to 0 V	–	114	–	nC
Gate-drain Charge	Q _{GD}		–	75	–	
Gate-source Charge	Q _{GS}		–	16	–	
Turn-on Delay Time	t _{d(on)}	V _{DS} = 800 V, I _D = 25 A, Gate Driver = -18 V to 0 V, R _G = 1 Ω, Inductive Load, FWD: UJ2D1215T, T _J = 25 °C	–	32	–	ns
Rise Time	t _r		–	43	–	
Turn-off Delay Time	t _{d(off)}		–	19	–	
Fall Time	t _f		–	16	–	
Turn-on Energy	E _{ON}	V _{DS} = 800 V, I _D = 25 A, Gate Driver = -18 V to 0 V, R _G = 1 Ω, Inductive Load, FWD: UJ2D1215T, T _J = 150 °C	–	785	–	μJ
Turn-off Energy	E _{OFF}		–	150	–	
Total Switching Energy	E _{TOTAL}		–	935	–	
Turn-on Delay Time	t _{d(on)}		–	28	–	ns
Rise Time	t _r		–	42	–	
Turn-off Delay Time	t _{d(off)}		–	18	–	
Fall Time	t _f		–	15	–	
Turn-on Energy	E _{ON}		–	730	–	μJ
Turn-off Energy	E _{OFF}		–	146	–	
Total Switching Energy	E _{TOTAL}		–	876	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAMS

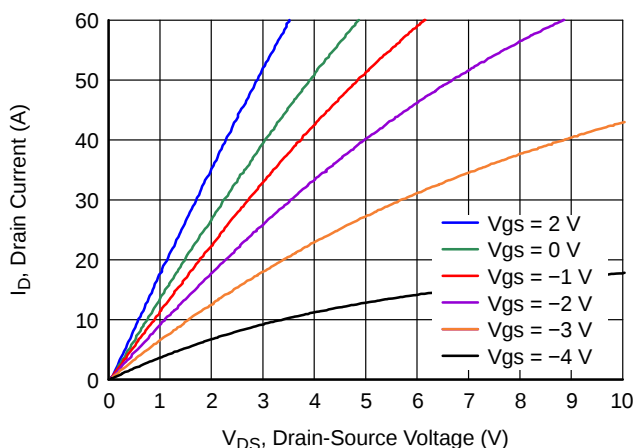


Figure 1. Typical Output Characteristics at $T_j = -55\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

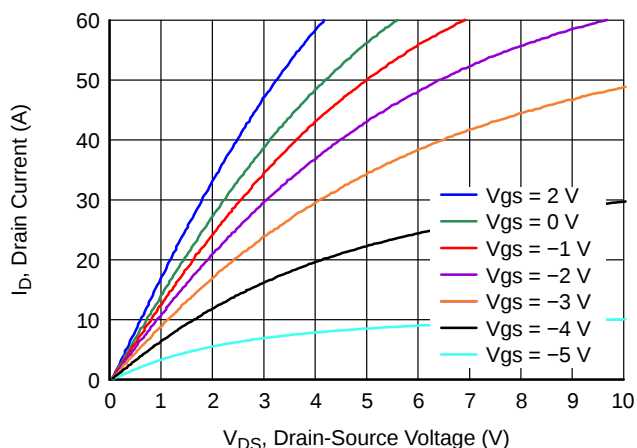


Figure 2. Typical Output Characteristics at $T_j = 25\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

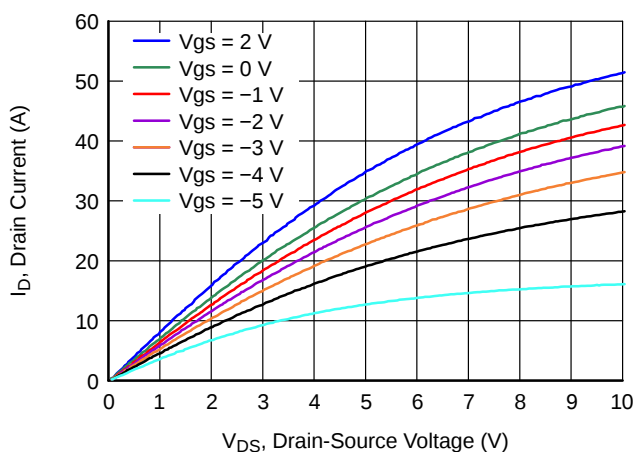


Figure 3. Typical Output Characteristics at $T_j = 175\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

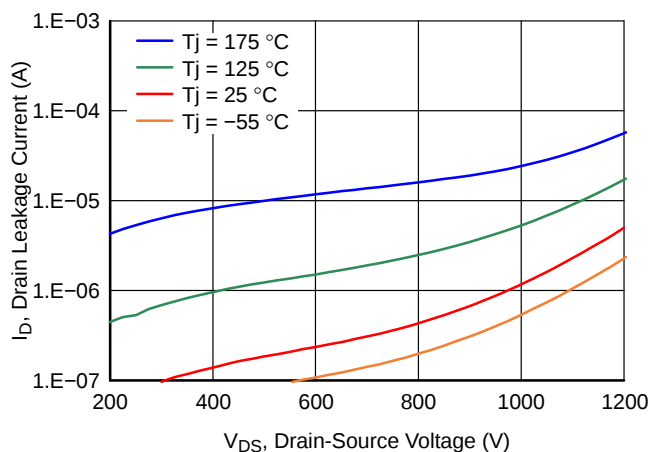


Figure 4. Typical Drain-source Leakage at $V_{GS} = -20\text{ V}$

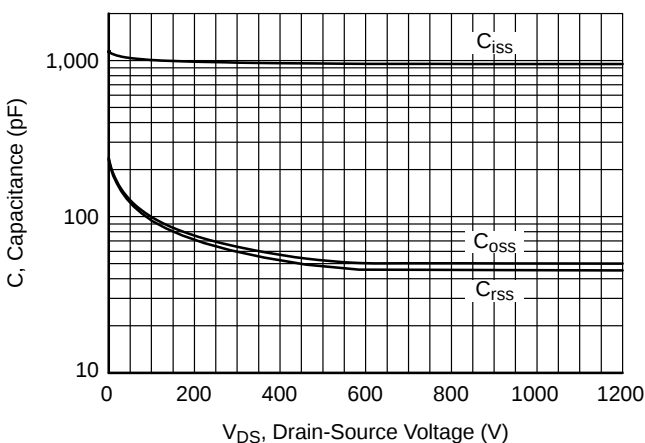


Figure 5. Typical Capacitances at $f = 100\text{ kHz}$ and $V_{GS} = -20\text{ V}$

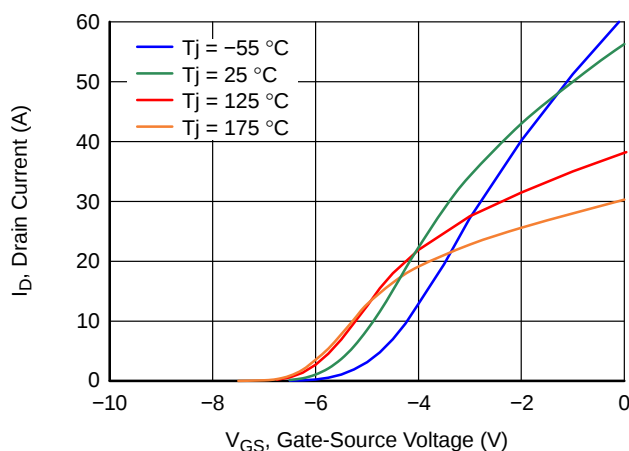


Figure 6. Typical Transfer Characteristics at $V_{DS} = 5\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

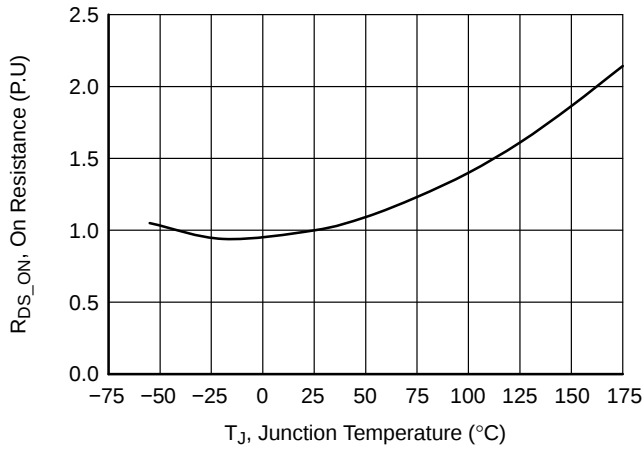


Figure 7. Normalized On-resistance vs. Junction Temperature at $V_{GS} = 0$ V and $I_D = 10$ mA

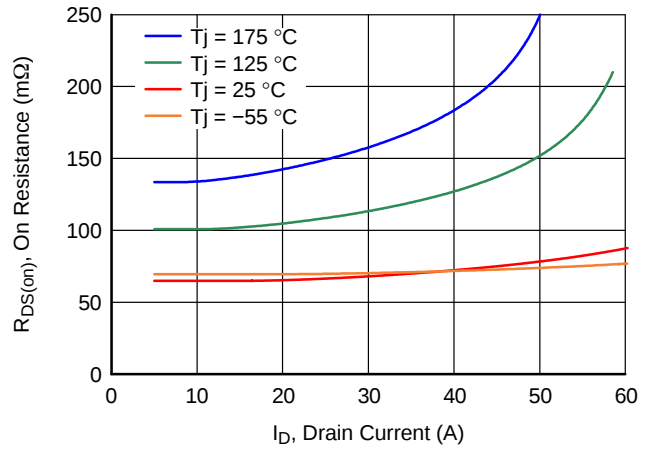


Figure 8. Typical Drain-source On-resistances at $V_{GS} = 0$ V

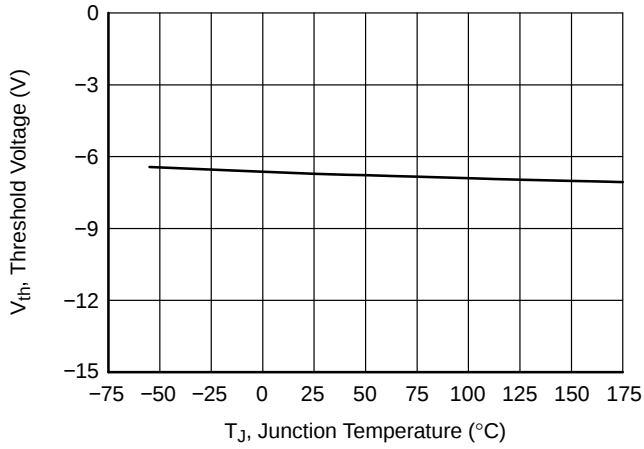


Figure 9. Threshold Voltage vs. Junction Temperature at $V_{DS} = 5$ V and $I_D = 35$ mA

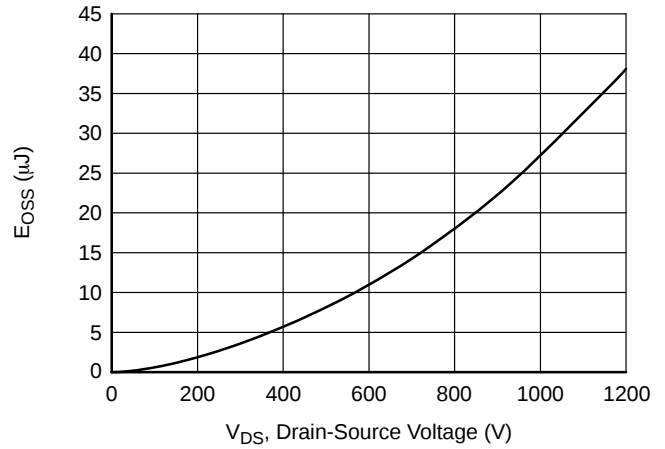


Figure 10. Typical Stored Energy in C_{OSS} at $V_{GS} = -20$ V

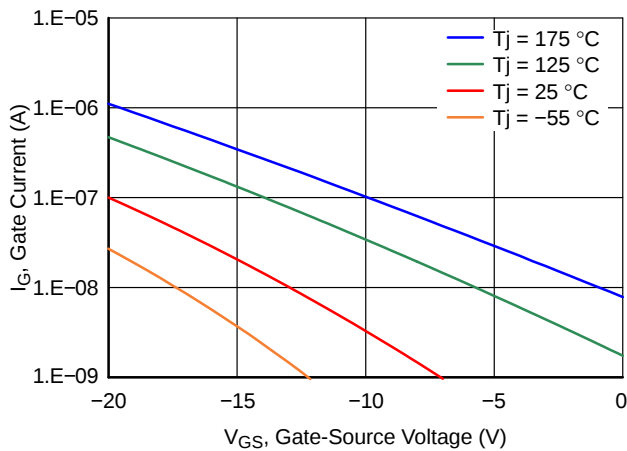


Figure 11. Typical Gate Leakage at $V_{DS} = 0$ V

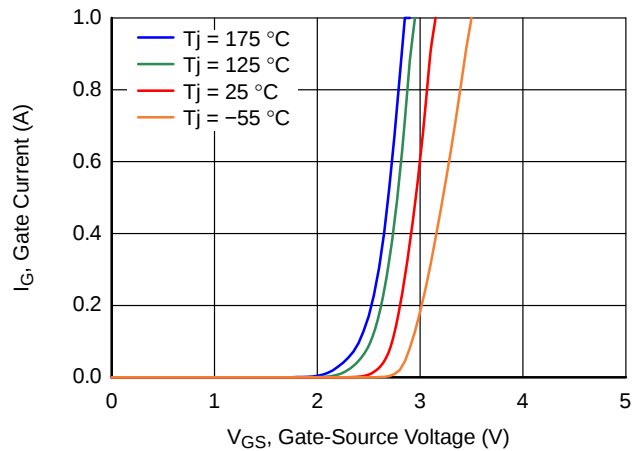


Figure 12. Typical Gate Forward Current at $V_{DS} = 0$ V

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

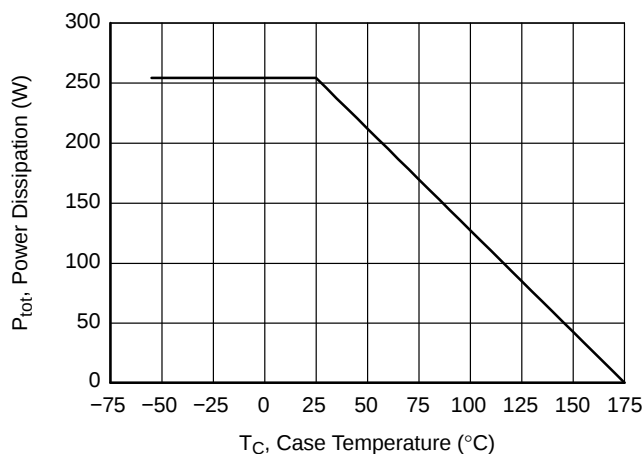


Figure 13. Total Power Dissipation

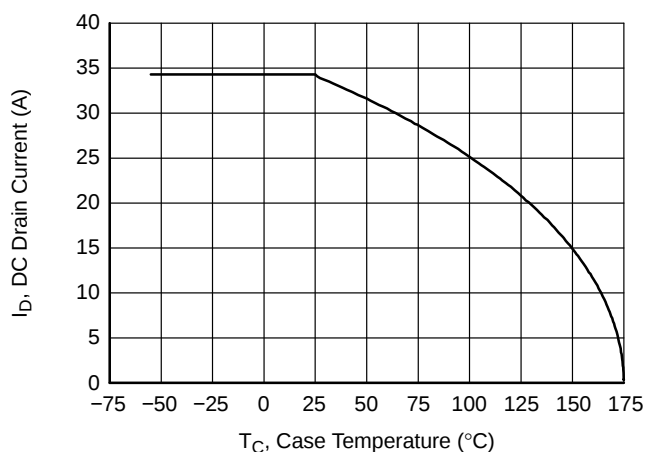


Figure 14. DC Drain Current Derating

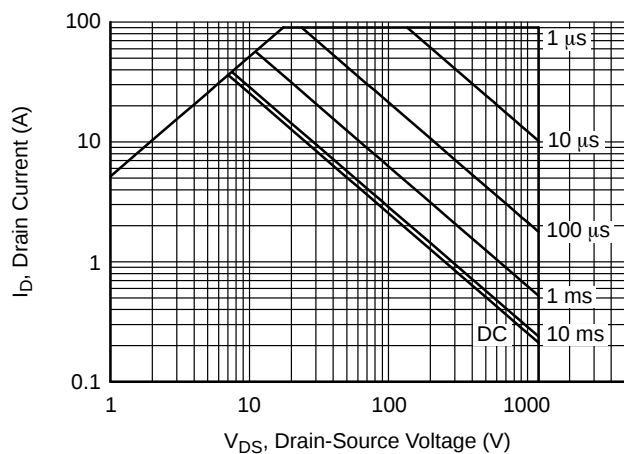


Figure 15. Safe Operation Area at $T_C = 25^\circ\text{C}$, Parameter t_p

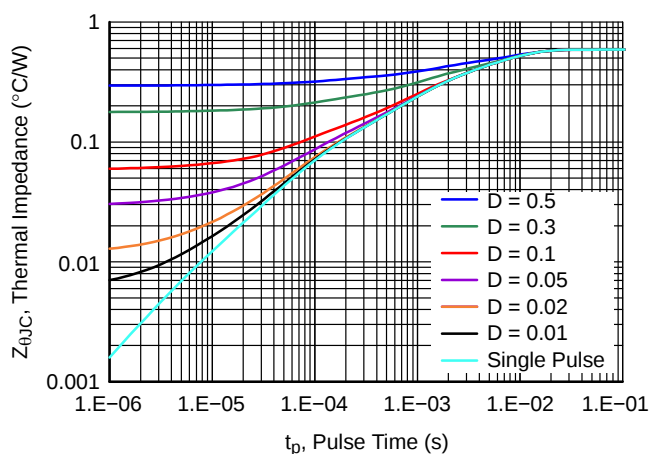


Figure 16. Maximum Transient Thermal Impedance

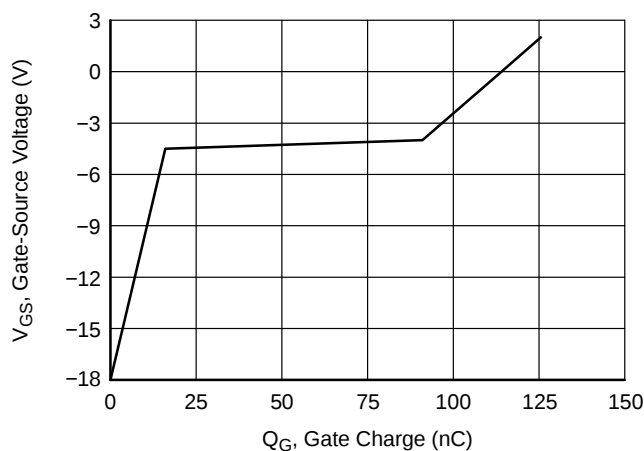


Figure 17. Typical Gate Charge at $V_{DS} = 800\text{ V}$ and $I_D = 25\text{ A}$

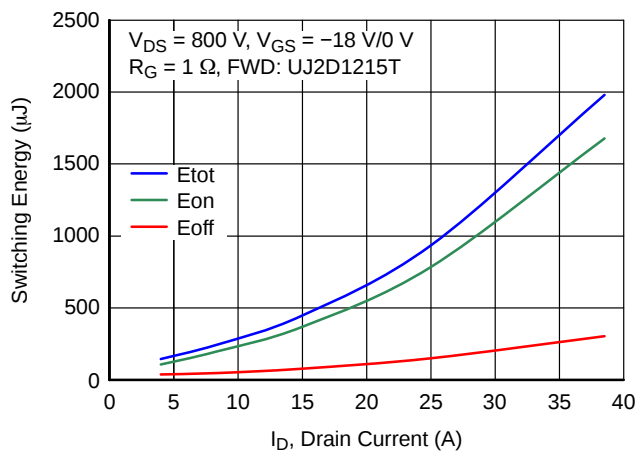


Figure 18. Clamped Inductive Switching Energy vs. Drain Current at $T_J = 25^\circ\text{C}$

UJ3N120065K3S

TYPICAL PERFORMANCE DIAGRAMS (CONTINUED)

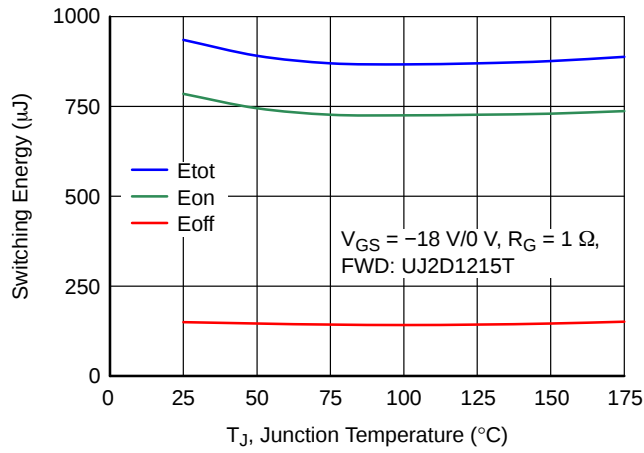


Figure 19. Clamped Inductive Switching Energy vs. Junction Temperature at $V_{\text{DS}} = 800 \text{ V}$ and $I_{\text{D}} = 25 \text{ A}$

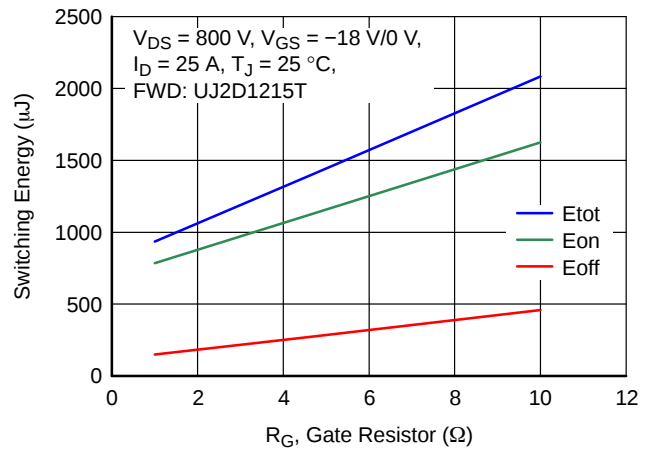


Figure 20. Clamped Inductive Switching Energy vs. Gate Resistor R_G

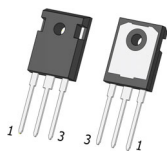
ORDERING INFORMATION

Part Number	Marking	Package	Shipping [†]
UJ3N120065K3S	UJ3N120065K3S	TO247-3 15.90x20.96x5.03, 5.44P (Pb-Free, Halogen Free)	600 / Tube

UJ3N120065K3S

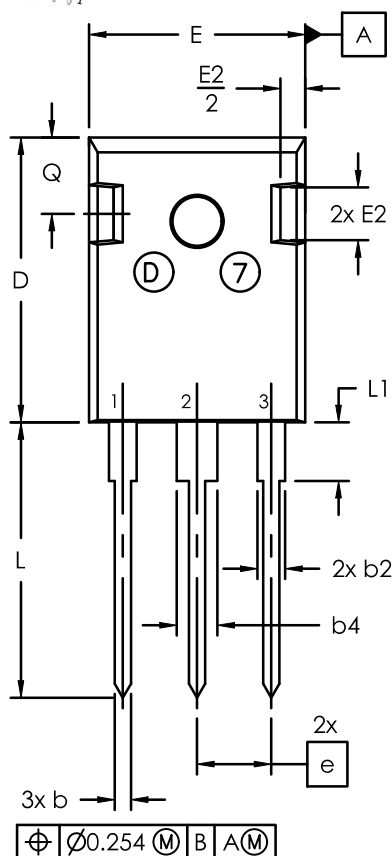
REVISION HISTORY

Revision	Description of Changes	Date
B	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with onsemi standards for SiC products.	1/15/2025
2	Converted the Data Sheet to onsemi format.	6/4/2025

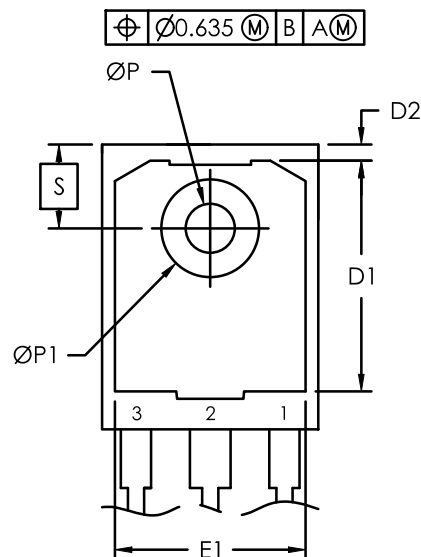
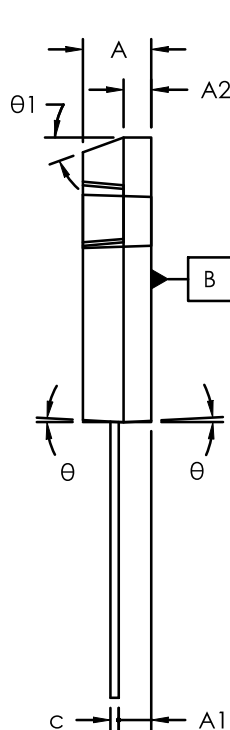
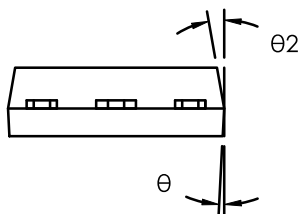


TO247-3 15.90x20.96x5.03, 5.44P
CASE 340AK
ISSUE B

DATE 14 APR 2025



$\varnothing 0.254$ (M) B A (M)



SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
b4	2.59	3.00	3.43
c	0.38	0.60	0.89
D	20.70	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	5.44 BSC		
E1	13.00	13.30	13.60
E2	3.43	3.89	5.20
L	19.62	20.27	20.32
L1	—	—	4.50
$\varnothing P$	3.40	3.60	3.80
$\varnothing P1$	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.15 BSC		
θ	3°		
$\theta 1$	20°		
$\theta 2$	10°		

NOTE:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. $\varnothing P$ to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.

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DESCRIPTION:	TO247-3 15.90x20.96x5.03, 5.44P	PAGE 1 OF 1

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