

## **SiC JFET Division**

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# Silicon Carbide (SiC) Cascode JFET -EliteSiC, Power N-Channel, D2PAK-7L, 750 V, 23 mohm

Rev. C, January 2025

### Description

The UJ4C075023B7S is a 750V,  $23m\Omega$  G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D²PAK-7L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

### **Features**

D (Tab)

- On-resistance R<sub>DS(on)</sub>: 23mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q<sub>rr</sub> = 80nC
- Low body diode V<sub>FSD</sub>: 1.23V
- Low gate charge: Q<sub>G</sub> = 37.8nC
- Threshold voltage V<sub>G(th)</sub>: 4.8V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3
- D<sup>2</sup>PAK-7L package for faster switching, clean gate waveforms

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G(1)

KS (2)€

DATASHEET

J4C075023B7S

Part Number	Package	Marking
UJ4C075023B7S	D <sup>2</sup> PAK-7L	UJ4C075023B7S







### Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating













## **Maximum Ratings**

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	$V_{DS}$		750	V
Cata aguraga valtaga	\/	DC	-20 to +20	V
Gate-source voltage	$V_{GS}$	AC (f > 1Hz)	-25 to +25	V
Continuous drain current <sup>1</sup>	1	T <sub>C</sub> = 25°C	64	А
Continuous drain current	I <sub>D</sub>	T <sub>C</sub> = 100°C	46	Α
Pulsed drain current <sup>2</sup>	I <sub>DM</sub>	T <sub>C</sub> = 25°C	196	Α
Single pulsed avalanche energy <sup>3</sup>	E <sub>AS</sub>	L=15mH, I <sub>AS</sub> =3A	67	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \le 500V$	150	V/ns
Power dissipation	P <sub>tot</sub>	T <sub>C</sub> = 25°C	278	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	$T_J, T_{STG}$		-55 to 175	°C
Reflow soldering temperature	T <sub>solder</sub>	reflow MSL 1	245	°C

- 1. Limited by  $T_{J,max}$
- 2. Pulse width  $t_p$  limited by  $T_{J,max}$
- 3. Starting  $T_J = 25^{\circ}C$

## **Thermal Characteristics**

Darameter	Symbol	Test Conditions	Value			Limita
Parameter			Min	Тур	Max	Units
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.42	0.54	°C/W















## Electrical Characteristics (T<sub>J</sub> = +25°C unless otherwise specified)

## Typical Performance - Static

Parameter	Symbol Test Conditions		Value			Units
r al allietei			Min	Тур Мах		Offics
Drain-source breakdown voltage	BV <sub>DS</sub>	$V_{GS}$ =0V, $I_D$ =1mA	750			V
Total drain leakage current		V <sub>DS</sub> =750V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C		2	30	
Total drain leakage current	I <sub>DSS</sub>	V <sub>DS</sub> =750V, V <sub>GS</sub> =0V, T <sub>J</sub> =175°C		15		μΑ
Total gate leakage current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, T <sub>J</sub> =25°C, V <sub>GS</sub> =-20V / +20V		6	±20	μА
	R <sub>DS(on)</sub>	$V_{GS}$ =12V, $I_{D}$ =40A, $T_{J}$ =25°C		23	29	
Drain-source on-resistance		V <sub>GS</sub> =12V, I <sub>D</sub> =40A, T <sub>J</sub> =125°C		39		mΩ
		$V_{GS}$ =12V, $I_{D}$ =40A, $T_{J}$ =175°C		50		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}$ =5V, $I_{D}$ =10mA	4	4.8	6	V
Gate resistance	$R_{G}$	f=1MHz, open drain		4.5		Ω

## Typical Performance - Reverse Diode

Parameter	Symbol	Tost Conditions	Value			11-24-	
Parameter	Symbol Test Conditions		Min Typ		Max	- Units	
Diode continuous forward current <sup>1</sup>	I <sub>S</sub>	T <sub>C</sub> = 25°C			64	Α	
Diode pulse current <sup>2</sup>	I <sub>S,pulse</sub>	T <sub>C</sub> = 25°C			196	Α	
Forward voltage	$V_{FSD}$	V <sub>GS</sub> =0V, I <sub>S</sub> =20A, T <sub>J</sub> =25°C	1.23 1.39		1.39	V	
1 of ward voltage	• FSD	V <sub>GS</sub> =0V, I <sub>S</sub> =20A, T <sub>J</sub> =175°C		1.45		v	
Reverse recovery charge	Q <sub>rr</sub>	$V_R$ =400V, $I_S$ =40A, $V_{GS}$ =0V, $R_{G\_EXT}$ =50 $\Omega$		80		nC	
Reverse recovery time	t <sub>rr</sub>	di/dt=1200A/μs, Τ <sub>J</sub> =25°C		12		ns	
Reverse recovery charge	Q <sub>rr</sub>	$V_R$ =400V, $I_S$ =40A, $V_{GS}$ =0V, $R_{G\_EXT}$ =50 $\Omega$		84		nC	
Reverse recovery time	t <sub>rr</sub>	di/dt=1200A/μs, Τ <sub>J</sub> =150°C		12.8		ns	













## Typical Performance - Dynamic

Danamadan	Cymalaal	Test Conditions	Value			Units	
Parameter	Parameter Symbol		Min	Тур	Max	UTILS	
Input capacitance	$C_{iss}$	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V		1400			
Output capacitance	$C_{oss}$	f=100kHz		93		pF	
Reverse transfer capacitance	$C_{rss}$	1-100KH2		2.5			
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}$ =0V to 400V, $V_{GS}$ =0V		116		pF	
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}$ =0V to 400V, $V_{GS}$ =0V		232		pF	
C <sub>OSS</sub> stored energy	$E_{oss}$	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V		9.3		μЈ	
Total gate charge	$Q_{G}$	- V <sub>DS</sub> =400V, I <sub>D</sub> =40A,		37.8			
Gate-drain charge	$Q_{GD}$	$V_{DS} = 400V, I_D = 40A,$ $V_{GS} = 0V \text{ to } 15V$		8		nC	
Gate-source charge	$Q_{GS}$			11.8			
Turn-on delay time	$t_{d(on)}$	Notes 4, $V_{DS}=400V, I_{D}=40A, Gate$ Driver =0V to +15V, $Turn-on R_{G,EXT}=1\Omega,$		11		ns - μJ	
Rise time	t <sub>r</sub>			23			
Turn-off delay time	$t_{d(off)}$			158			
Fall time	$t_f$	Turn-off $R_{G,EXT}$ =50 $\Omega$ ,		17			
Turn-on energy	E <sub>ON</sub>	inductive Load, FWD: same device with $V_{GS} = 0V$		219			
Turn-off energy	$E_{OFF}$	and $R_G = 50\Omega$ ,		167			
Total switching energy	E <sub>TOTAL</sub>	T <sub>J</sub> =25°C		386			
Turn-on delay time	$t_{d(on)}$	Notes 4,		11		ns	
Rise time	t <sub>r</sub>	$V_{DS}$ =400V, $I_D$ =40A, Gate Driver =0V to +15V.		23			
Turn-off delay time	$t_{d(off)}$	Turn-on $R_{G,EXT}=1\Omega$ , Turn-off $R_{G,EXT}=50\Omega$ ,		160			
Fall time	t <sub>f</sub>			18.4			
Turn-on energy	E <sub>ON</sub>	inductive Load, FWD: same device with $V_{GS} = 0V$		238			
Turn-off energy	E <sub>OFF</sub>	and $R_G = 50\Omega$ ,		189		μЈ	
Total switching energy	E <sub>TOTAL</sub>	T <sub>J</sub> =150°C		427			

 $<sup>4.\,</sup>Measured\,with\,the\,switching\,test\,circuit\,in\,Figure\,23.$ 













## Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions	Value			Units
Parameter	Зуппоп	rest Conditions	Min	Тур	Max	Offics
Turn-on delay time	t <sub>d(on)</sub>			13		
Rise time	t <sub>r</sub>	Notes 5 and 6, V <sub>DS</sub> =400V, I <sub>D</sub> =40A, Gate		23		ns
Turn-off delay time	$t_{d(off)}$	$V_{DS}$ =400V, $I_D$ =40A, Gate Driver =0V to +15V,		44		115
Fall time	t <sub>f</sub>	Turn-on $R_{G,EXT} = 1\Omega$ ,		9.6		
Turn-on energy including R <sub>S</sub> energy	E <sub>ON</sub>	Turn-off $R_{G,EXT}$ =5 $\Omega$ , inductive Load, FWD: same		231		
Turn-off energy including R <sub>S</sub> energy	E <sub>OFF</sub>	device with $V_{GS} = 0V$ and		53		
Total switching energy	E <sub>TOTAL</sub>	$R_G = 5\Omega$ , RC snubber: $R_S = 10\Omega$ and $C_S = 200$ pF, $T_J = 25$ °C		284		μЈ
Snubber R <sub>S</sub> energy during turn-on	E <sub>RS_ON</sub>			8		
Snubber R <sub>S</sub> energy during turn-off	E <sub>RS_OFF</sub>			5		
Turn-on delay time	t <sub>d(on)</sub>			12		
Rise time	t <sub>r</sub>	Notes 5 and 6, V <sub>DS</sub> =400V, I <sub>D</sub> =40A, Gate		23		ns
Turn-off delay time	$t_{d(off)}$	Driver = 0V to +15V,		44		115
Fall time	t <sub>f</sub>	Turn-on $R_{G,EXT}=1\Omega$ ,		9.6		
Turn-on energy including R <sub>S</sub> energy	E <sub>ON</sub>	Turn-off $R_{G,EXT}$ =5 $\Omega$ , inductive Load, FWD: same device with $V_{GS}$ = 0V and $R_{G}$ = 5 $\Omega$ , RC snubber:		231		
Turn-off energy including $R_S$ energy	E <sub>OFF</sub>			53		μJ
Total switching energy	E <sub>TOTAL</sub>			284		
Snubber R <sub>S</sub> energy during turn-on	E <sub>RS_ON</sub>	$R_S$ =10 $\Omega$ and $C_S$ =200pF, $T_I$ =150°C		8.3		
Snubber R <sub>S</sub> energy during turn-off	E <sub>RS_OFF</sub>	., _50 0		6		

<sup>5.</sup> Measured with the switching test circuit in Figure 24.

<sup>6.</sup> In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.





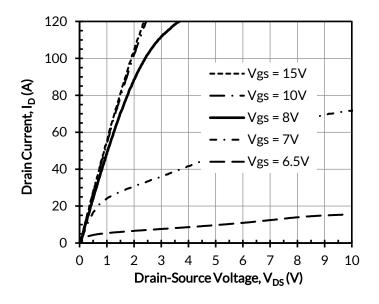








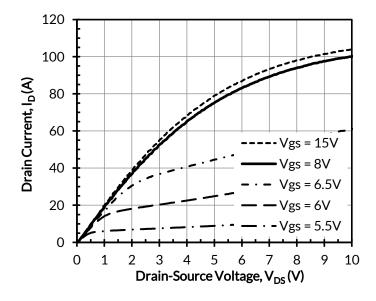
### **Typical Performance Diagrams**



120 100 Drain Current, I<sub>D</sub> (A) 80 60 Vgs = 15V Vgs = 8V 40 Vgs = 7V- Vgs = 6.5V 20 Vgs = 6V 0 1 2 3 5 10 Drain-Source Voltage,  $V_{DS}(V)$ 

Figure 1. Typical output characteristics at  $T_J$  = - 55°C, tp < 250 $\mu$ s

Figure 2. Typical output characteristics at  $T_J = 25$ °C,  $tp < 250\mu s$ 



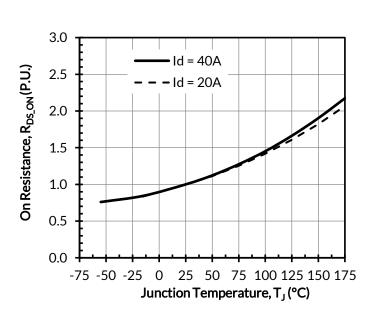


Figure 3. Typical output characteristics at  $T_J$  = 175°C, tp < 250 $\mu$ s

Figure 4. Normalized on-resistance vs. temperature at  $V_{GS}$  = 12V



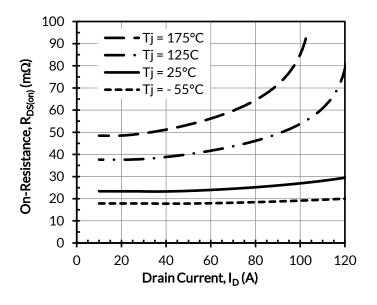








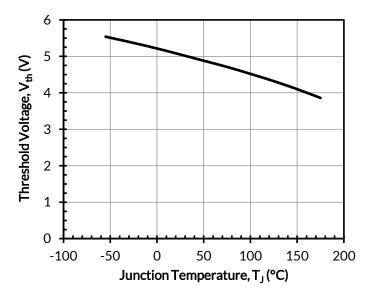




Tj = -55°C Tj = 25°C Drain Current, I<sub>D</sub> (A) Tj = 175°C Gate-Source Voltage,  $V_{GS}(V)$ 

Figure 5. Typical drain-source on-resistances at  $V_{\text{GS}}$  = 12V

Figure 6. Typical transfer characteristics at  $V_{DS} = 5V$ 



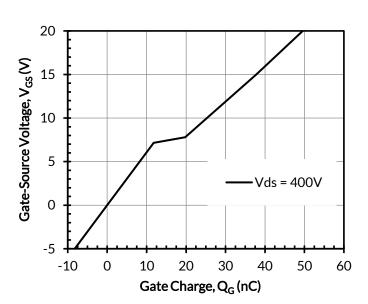


Figure 7. Threshold voltage vs. junction temperature at  $V_{DS}$  = 5V and  $I_{D}$  = 10mA

Figure 8. Typical gate charge at  $I_D = 40A$ 













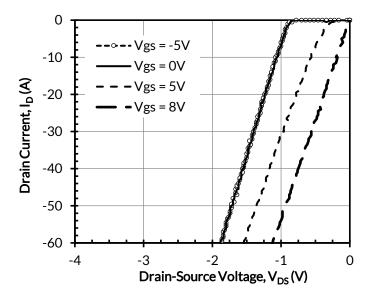
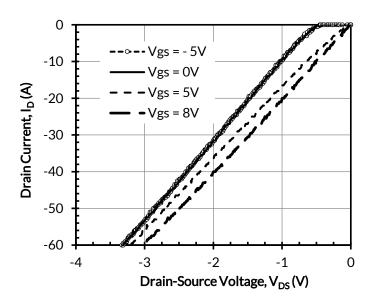


Figure 9. 3rd quadrant characteristics at  $T_J = -55$ °C

Figure 10. 3rd quadrant characteristics at  $T_J = 25$ °C



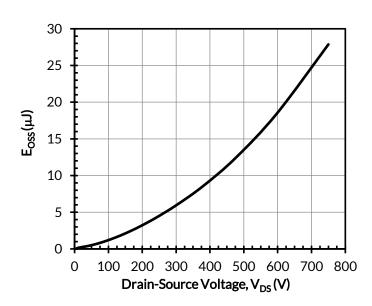


Figure 11. 3rd quadrant characteristics at  $T_J = 175$ °C

Figure 12. Typical stored energy in  $C_{OSS}$  at  $V_{GS} = 0V$ 



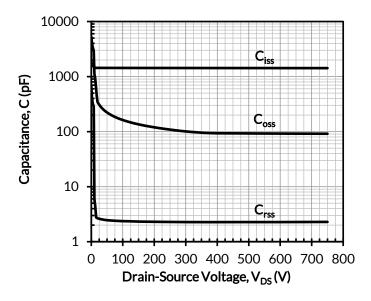












80 70 60 40 40 40 20 10 -75 -50 -25 0 25 50 75 100 125 150 175 Case Temperature, T<sub>c</sub> (°C)

Figure 13. Typical capacitances at f = 100kHz and  $V_{GS} = 0V$ 

Figure 14. DC drain current derating

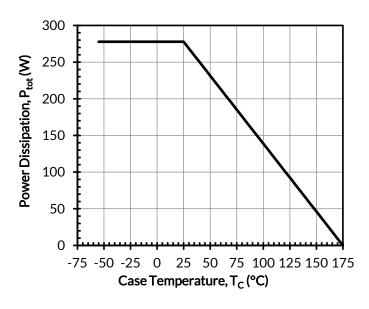


Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance













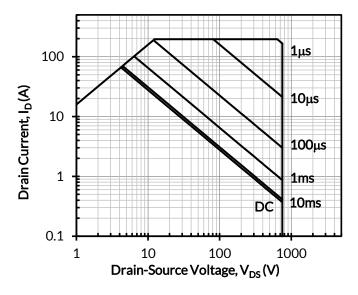


Figure 17. Safe operation area at  $T_C$  = 25°C, D = 0, Parameter  $t_p$ 

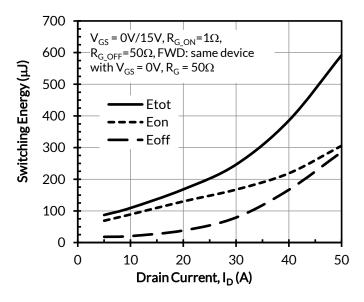


Figure 19. Clamped inductive switching energy vs. drain current at  $V_{DS}$  = 400V and  $T_J$  = 25°C

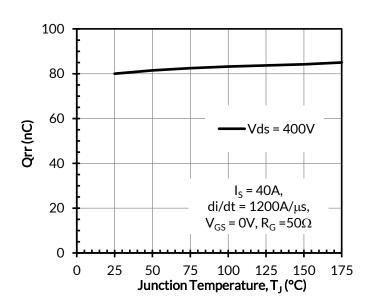


Figure 18. Reverse recovery charge Qrr vs. junction temperature

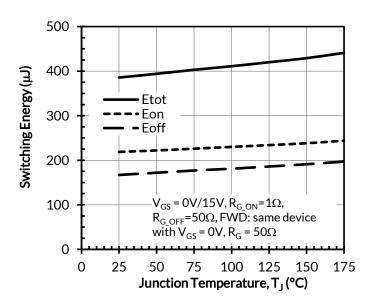


Figure 21. Clamped inductive switching energy vs. junction temperature at  $V_{DS}$  = 400V and  $I_D$  = 40A



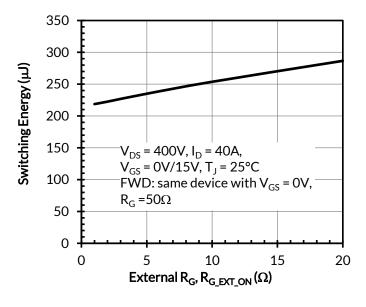








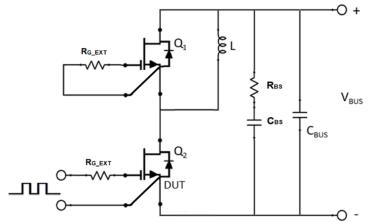




350  $V_{DS} = 400V, I_{D} = 40A,$  $V_{GS} = 0V/15V, T_J = 25^{\circ}C$ 300 FWD: same device with Switching Energy (µJ) 250  $V_{GS} = 0V, R_G = R_{GEXT}$ 200 150 100 50 0 20 40 60 80 0 100 External  $R_G$ ,  $R_{G\_EXT\_OFF}$  ( $\Omega$ )

Figure 21. Clamped inductive switching turn-on energy vs.  $R_{G,EXT\ ON}$ 

Figure 22. Clamped inductive switching turn-off energy vs.  $R_{G,EXT\_OFF}$ 



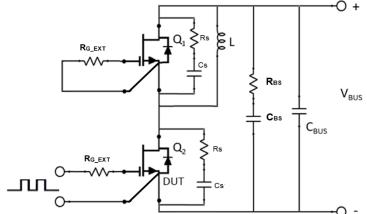


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ( $R_{BS}$  = 2.5 $\Omega$ ,  $C_{BS}$ =100nF) is used to reduce the power loop high frequency oscillations.

Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers ( $R_s = 10\Omega$ ,  $C_s = 200pF$ ) and a bus RC snubber ( $R_{BS} = 2.5\Omega$ ,  $C_{BS} = 100nF$ ).













### **Applications Information**

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small  $R_{(G)}$ , or gate resistor, provides better EMI suppression with higher efficiency compared to using a high  $R_{(G)}$  value. There is no extra gate delay time when using the snubber circuitry, and a small  $R_{(G)}$  will better control both the turn-off  $V_{(DS)}$  peak spike and ringing duration, while a high  $R_{(G)}$  will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high  $R_{(G)}$ , while greatly reducing  $E_{(OFF)}$  from mid-to-full load range with only a small increase in  $E_{(ON)}$ . Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

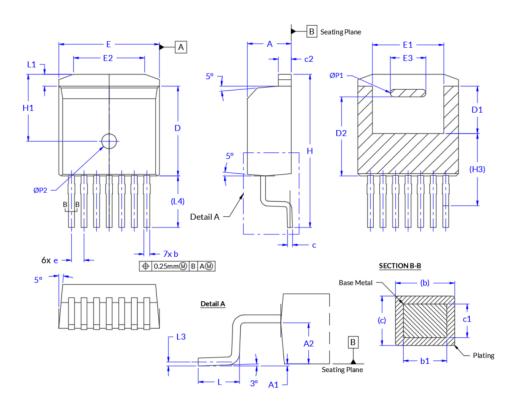
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TO263-7L (D2PAK-7L) PACKAGE OUTLINE, MARKING, TAPE AND REEL SPECIFICATION	PART	Page <b>1</b> of <b>4</b>
DS TO 263 71		Rev D

#### **PACKAGE OUTLINE**



	7L-D2PAK				
SYM	М	М	IN	CH	
31141	Min	Max	Min	Max	
Α	4.30	4.56	.169	.180	
A1	0.00	0.25	.000	.010	
A2	2.45	2.75	.096	.108	
b	0.50	0.70	.020	.028	
b1	0.50	-	.020	-	
С	0.40	0.60	.016	.024	
c1	0.40		.016		
c2	1.20	1.40	.047	.055	
D	8.93	9.23	.352	.363	
D1	4.65	4.95	.183	.195	
D2	7.90	8.10	.311	.319	
e	1.27 BSC		.050 BSC		
E	10.08	10.28	.397	.405	
E1	6.82	7.62	.269	.300	
E2	6.50	8.60	.256	.339	
E3	3.50	3.70	.138	.146	
Н	15.00	16.00	.591	.630	
H1	6.68	6.88	.263	.271	
H3	7.31	REF.	.287	REF	
L	1.90	2.50	.075	.098	
L1	0.98	1.42	.039	.056	
L3	0.25 BSC		.0098 BSC		
L4	5.22	REF	.205	REF	
ØP1	0.65	0.85	.026	.033	
ØP2	1.40	1.60	.055	.063	

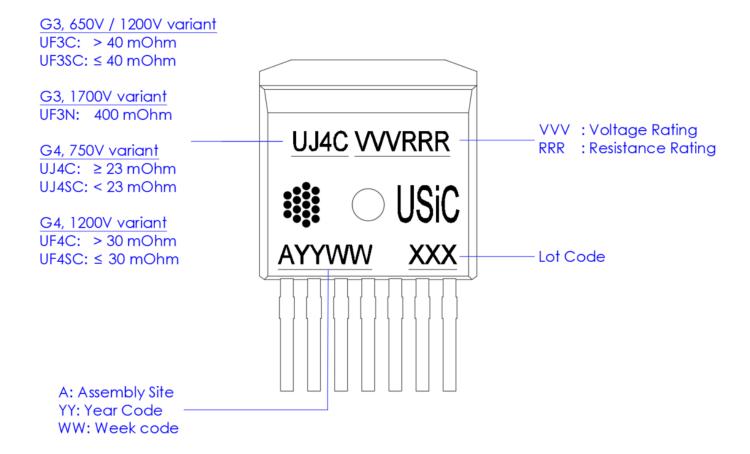
#### Notes:

- 1. GENERAL TOLERANCE: ±0.1 unless otherwise specified
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. PACKAGE BODY SIDES EXCLUDE MOLD FLASH AND GATE BURRS.
- 4. DIMENSION LIS MEASURED IN GAUGE LINE.
- 5. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
- 6. DIMENSION c1 AND b1 APPLIES TO BASE METAL ONLY



TO263-7L (D2PAK-7L) PACKAGE OUTLINE, PART MARKING, TAPE AND REEL SPECIFICATION	Page <b>2</b> of <b>4</b>
DS_TO_263_7L	Rev D

#### **PART MARKING**



Template: FOR-000530 Rev G



TO263-7L	(D2PAK-7L)	PACKAGE	OUTLINE,	PART
MARKING,	TAPE AND RE	<b>EL SPECIFIC</b>	ATION	

TO 000 7

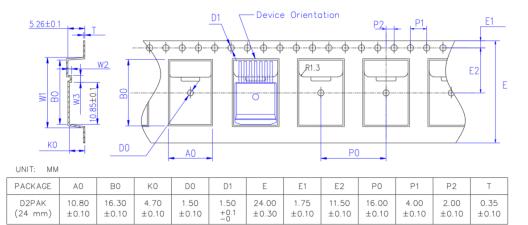
Page **3** of **4** 

Rev D

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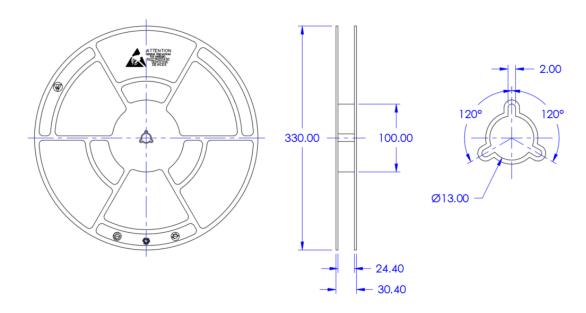
### **PACKING TYPE**

### Carrier Tape



Exterior		size	
Spec 1	W1	16.9±0.1	
	W2	1.3±0.1	
	W3	1.0±0.1	
Spec 2	W1	17.2±0.1	(1)
	W2	1.8±0.1	<b>(b)</b>
	W3	0.85±0.1	0

### Reel



All dimensions in millimeters Anti-Static Tape and Rell (T&R) Quantity per Reel: 800 units



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#### **REVISION HISTORY**

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
С	11/06/2023	Updated to Qorvo template Updated Package outline drawing based latest drawing revision	Glenn Galang
D	05/21/2024	Added illustration of device orientation on carrier tape (page 3)	Glenn Galang

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