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DATA SHEET
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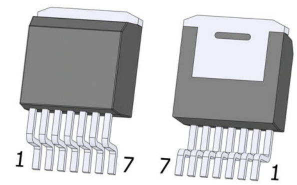
Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO-263-7, 750 V, 18 mohm

SiC JFET w/ Si MOSFET

UJ4SC075018B7S



TO-263-7
CASE 418BA

Description

The UJ4SC075018B7S is a 750 V, 18 mΩ G4 SiC FET. It is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-263-7 package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

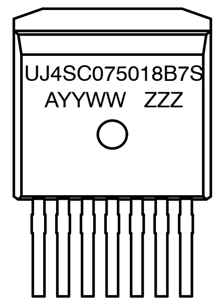
Features

- On-Resistance $R_{DS(on)}$: 18 mΩ (typ)
- Operating Temperature: 175 °C (Max)
- Excellent Reverse Recovery: Q_{rr} = 125 nC
- Low Body Diode V_{FSD}: 1.14 V
- Low Gate Charge : Q_G = 37.8 nC
- Threshold Voltage $V_{G(th)}$: 4.8 V (typ) Allowing 0 to 15 V Drive
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2
- TO-263-7 Package for Faster Switching, Clean Gate Waveforms
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Typical Applications

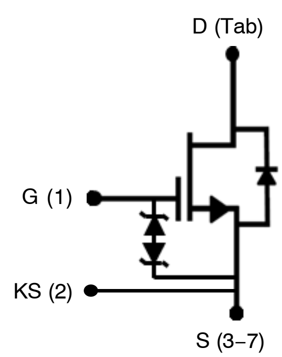
- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

MARKING DIAGRAM



UJ4SC075018B7S	=	Specific Device Number
A	=	Assembly Location
YY	=	Year
WW	=	Work Week
ZZZ	=	Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Value	Unit
V_{DS}	Drain-Source Voltage		750	V
V_{GS}	Gate-Source Voltage	DC	−20 to +20	V
		AC (f > 1 Hz)	−25 to +25	V
I_D	Continuous Drain Current (Note 1)	T_C = 25 °C	72	A
		T_C = 100 °C	52	A
I_{DM}	Pulsed Drain Current (Note 2)	T_C = 25 °C	208	A
E_{AS}	Single Pulsed Avalanche Energy (Note 3)	L = 15 mH, I_{AS} = 3.6 A	97.2	mJ
dv/dt	SiC FET dv/dt Ruggedness	$V_{DS} \leq$ 500 V	200	V/ns
P_{tot}	Power Dissipation	T_C = 25 °C	259	W
$T_{J,max}$	Maximum Junction Temperature		175	°C
T_J, T_{STG}	Operating and Storage Temperature		−55 to 175	°C
T_{SOLDER}	Reflow Soldering Temperature	Reflow MSL 1	245	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25 °C

THERMAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		–	0.45	0.58	°C/W

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC							
BV_{DS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA		750	–	–	V
I_{DSS}	Total Drain Leakage Current	V_{DS} = 750 V, V_{GS} = 0 V, T_J = 25 °C		–	1.3	45	μA
		V_{DS} = 750 V, V_{GS} = 0 V, T_J = 175°C		–	20	–	
I_{GSS}	Total Gate Leakage Current	V_{DS} = 0 V , T_J = 25 °C V_{GS} = −20 V / + 20 V		–	4.7	±20	μA
$R_{DS(on)}$	Drain-Source On-resistance	V_{GS} = 12 V, I_D = 50 A	T_J = 25 °C	–	18	23	mΩ
			T_J = 125 °C	–	29	–	
			T_J = 175 °C	–	37	–	
$V_{G(th)}$	Gate Threshold Voltage	V_{DS} = 5 V, I_D = 10 mA		4.0	4.8	6.0	V
R_G	Gate Resistance	f = 1 MHz, open drain		–	4.5	–	Ω
TYPICAL PERFORMANCE – REVERSE DIODE							
I_S	Diode Continuous Forward Current (Note 1)	T_C = 25 °C		–	–	72	A
$I_{S,pulse}$	Diode Pulse Current (Note 2)	T_C = 25 °C		–	–	208	A
V_{FSD}	Forward Voltage	V_{GS} = 0 V, I_S = 20 A, T_J = 25 °C		–	1.14	1.46	V
		V_{GS} = 0 V, I_S = 20 A, T_J = 175 °C		–	1.35	–	
Q_{rr}	Reverse Recovery Charge	V_{DS} = 400 V, I_S = 50 A, V_{GS} = 0 V, R_{G_EXT} = 50 Ω, di/dt = 1400 A/μs, T_J = 25 °C		–	125	–	nC
t_{rr}	Reverse Recovery Time			–	12.5	–	ns
Q_{rr}	Reverse Recovery Charge	V_{DS} = 400 V, I_S = 50 A, V_{GS} = 0 V, R_{G_EXT} = 50 Ω, di/dt = 1400 A/μs, T_J = 150 °C		–	128	–	nC
t_{rr}	Reverse Recovery Time			–	14.4	–	ns
TYPICAL PERFORMANCE – DYNAMIC							
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 100 kHz		–	1414	–	pF
C_{oss}	Output Capacitance			–	118	–	
C_{rss}	Reverse Transfer Capacitance			–	2.0	–	
$C_{oss(er)}$	Effective Output Capacitance, Energy Related	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		–	150	–	pF
$C_{oss(tr)}$	Effective Output Capacitance, Time Related			–	280	–	pF
E_{oss}	C_{OSS} Stored Energy	V_{DS} = 400 V, V_{GS} = 0 V		–	12	–	μJ
Q_G	Total Gate Charge	V_{DS} = 400 V, I_D = 50 A, V_{GS} = 0 V to 15 V		–	37.8	–	nC
Q_{GD}	Gate-Drain Charge			–	8.0	–	
Q_{GS}	Gate-Source Charge			–	11.8	–	
$t_{d(on)}$	Turn-on Delay Time	Note 4 V_{DS} = 400 V, I_D = 50 A, Gate Driver = 0 V, to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 50 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V and R_G = 50 Ω, T_J = 25 °C		–	13	–	ns
t_r	Rise Time			–	23	–	
$t_{d(off)}$	Turn-off Delay Time			–	136	–	
t_f	Fall Time			–	17.6	–	
E_{ON}	Turn-on Energy			–	209	–	μJ
E_{OFF}	Turn-off Energy			–	212	–	
E_{TOTAL}	Total Switching Energy			–	421	–	

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – DYNAMIC						
$t_{d(on)}$	Turn-on Delay Time	Note 4 V_{DS} = 400 V, I_D = 50 A, Gate Driver = 0 V, to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 50 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V and R_G = 50 Ω, T_J = 150 °C	–	10.5	–	ns
t_r	Rise Time		–	26	–	
$t_{d(off)}$	Turn-off Delay Time		–	146	–	
t_f	Fall Time		–	20	–	
E_{ON}	Turn-on Energy		–	245	–	μJ
E_{OFF}	Turn-off Energy		–	248	–	
E_{TOTAL}	Total Switching Energy		–	493	–	
$t_{d(on)}$	Turn-on Delay Time	Notes 5 and 6 V_{DS} = 400 V, I_D = 50 A, Gate Driver = 0 V, to +15 V, $R_{G,EXT}$ = 1 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V and R_G = 1 Ω, RC snubber: R_S = 10 Ω and C_S = 300 pF, T_J = 25 °C	–	19	–	ns
t_r	Rise Time		–	27	–	
$t_{d(off)}$	Turn-off Delay Time		–	41.6	–	
t_f	Fall Time		–	10.4	–	
E_{ON}	Turn-on Energy Including R_S Energy		–	169	–	μJ
E_{OFF}	Turn-off Energy Including R_S Energy		–	149	–	
E_{TOTAL}	Total Switching Energy		–	318	–	
E_{RS_ON}	Snubber R_S Energy During Turn-on		–	5	–	
E_{RS_OFF}	Snubber R_S Energy During Turn-off		–	8.5	–	
$t_{d(on)}$	Turn-on Delay Time	Notes 5 and 6 V_{DS} = 400 V, I_D = 50 A, Gate Driver = 0 V, to +15 V, $R_{G,EXT}$ = 1 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V and R_G = 1 Ω, RC snubber: R_S = 10 Ω and C_S = 300 pF, T_J = 150 °C	–	17	–	ns
t_r	Rise Time		–	29	–	
$t_{d(off)}$	Turn-off Delay Time		–	41	–	
t_f	Fall Time		–	9	–	
E_{ON}	Turn-on Energy Including R_S Energy		–	198	–	μJ
E_{OFF}	Turn-off Energy Including R_S Energy		–	153	–	
E_{TOTAL}	Total Switching Energy		–	351	–	
E_{RS_ON}	Snubber R_S Energy During Turn-on		–	5	–	
E_{RS_OFF}	Snubber R_S Energy During Turn-off		–	7	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Measured with the switching test circuit in Figure 23.
5. Measured with the switching test circuit in Figure 24.
6. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

TYPICAL CHARACTERISTICS

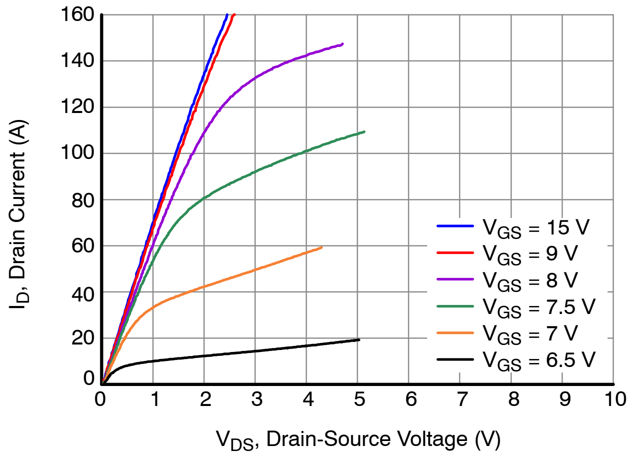


Figure 1. Typical Output Characteristics at T_J = –55 °C, t_p < 250 μs

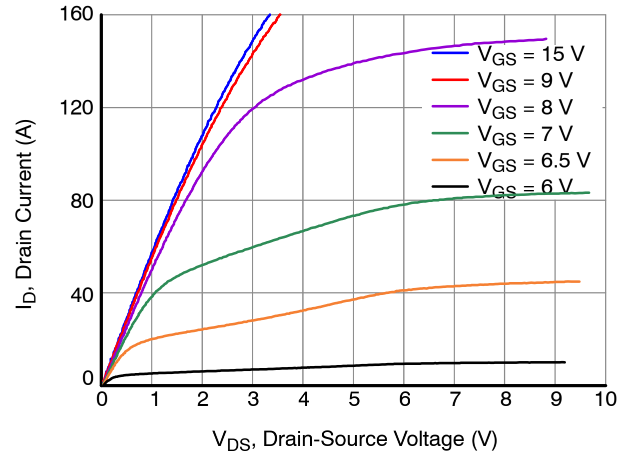


Figure 2. Typical Output Characteristics at T_J = 25 °C, t_p < 250 μs

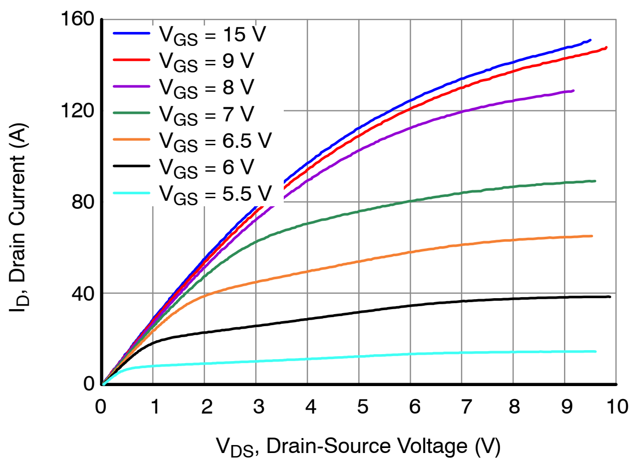


Figure 3. Typical Output Characteristics at T_J = 175 °C, t_p < 250 μs

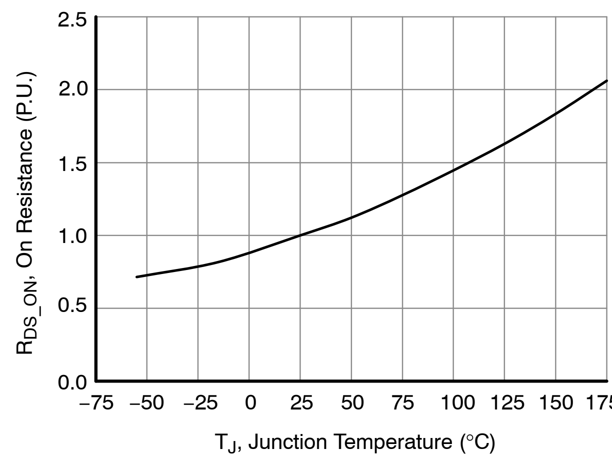


Figure 4. Normalized On-Resistance vs. Temperature at V_{GS} = 12 V and I_D = 50 A

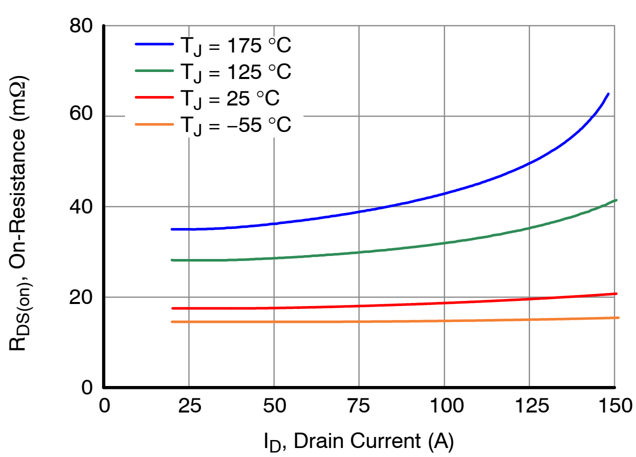


Figure 5. Typical Drain-Source On-Resistances at V_{GS} = 12 V

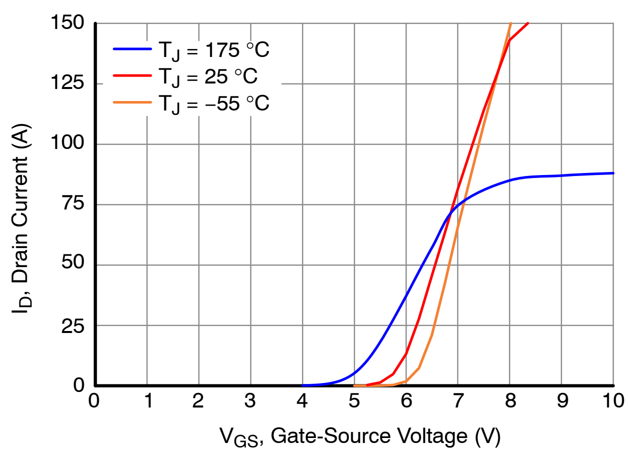


Figure 6. Typical Transfer Characteristics at V_{DS} = 5 V

TYPICAL CHARACTERISTICS (continued)

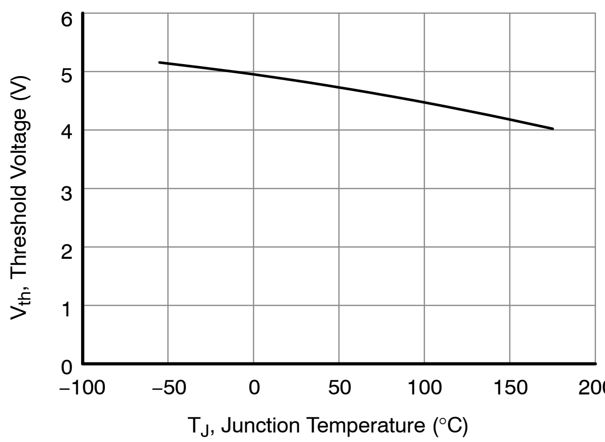


Figure 7. Threshold Voltage vs. Junction Temperature at V_{DS} = 5 V and I_D = 10 mA

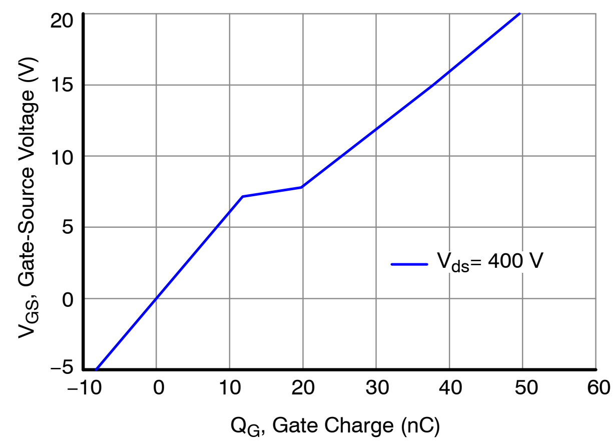


Figure 8. Typical Gate Charge at I_D = 50 A

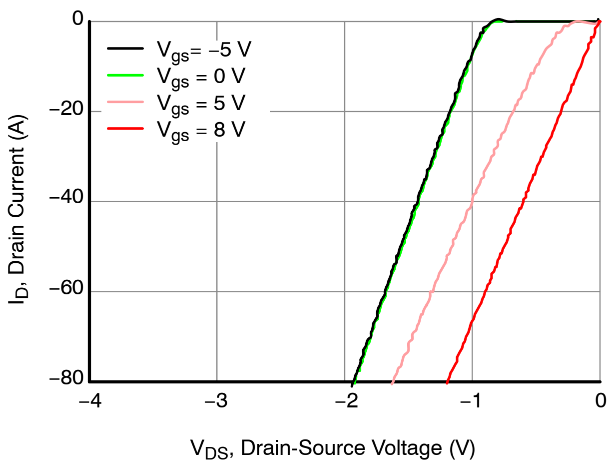


Figure 9. 3rd Quadrant Characteristics at T_J = −55 °C

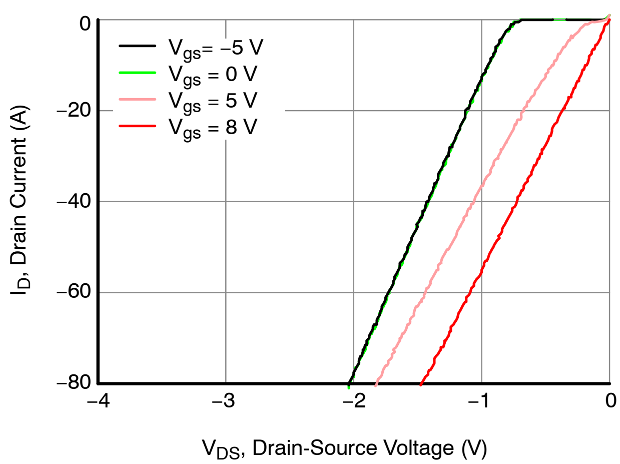


Figure 10. 3rd Quadrant Characteristics at T_J = 25 °C

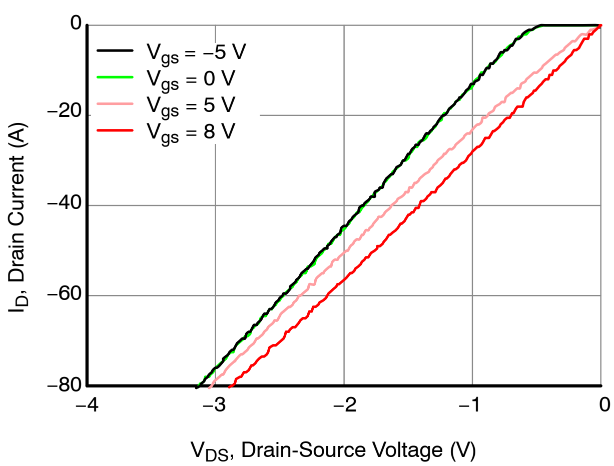


Figure 11. 3rd Quadrant Characteristics at T_J = 175 °C

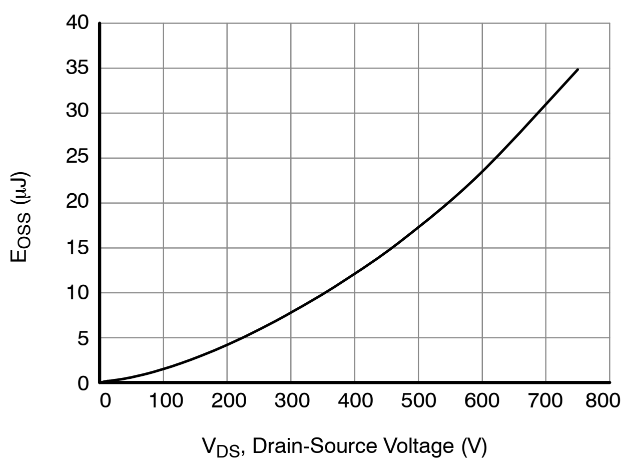


Figure 12. Typical Stored Energy in C_{OSS} at V_{GS} = 0 V

TYPICAL CHARACTERISTICS (continued)

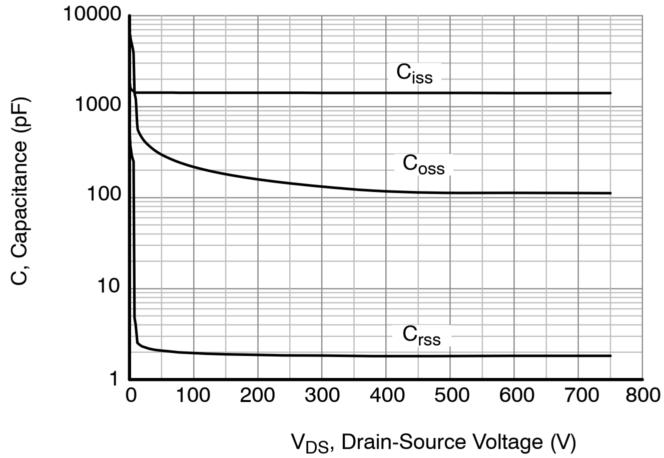


Figure 13. Typical Capacitances at f = 100 kHz and V_{GS} = 0 V

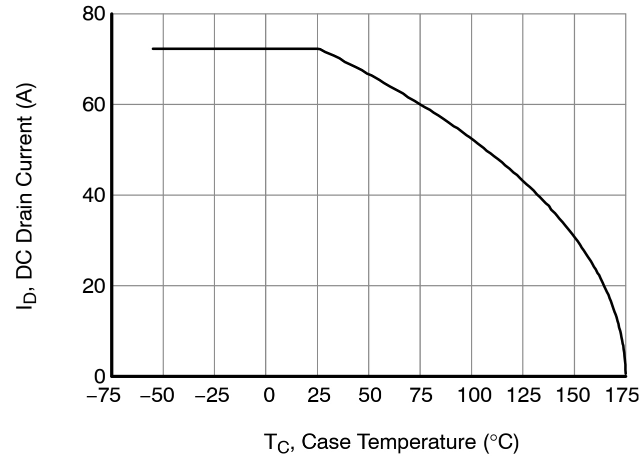


Figure 14. DC Drain Current Derating

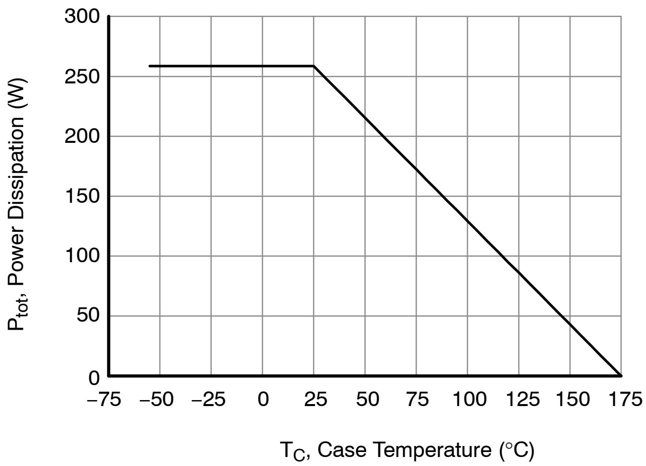


Figure 15. Total Power Dissipation

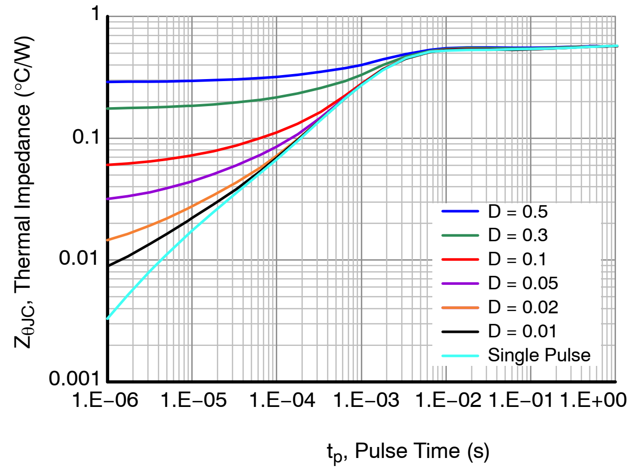


Figure 16. Maximum Transient Thermal Impedance

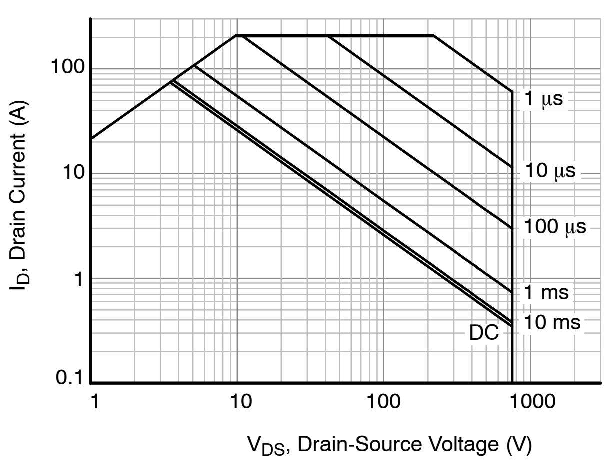


Figure 17. Safe Operation Area at T_C = 25 °C, D = 0, Parameter t_p

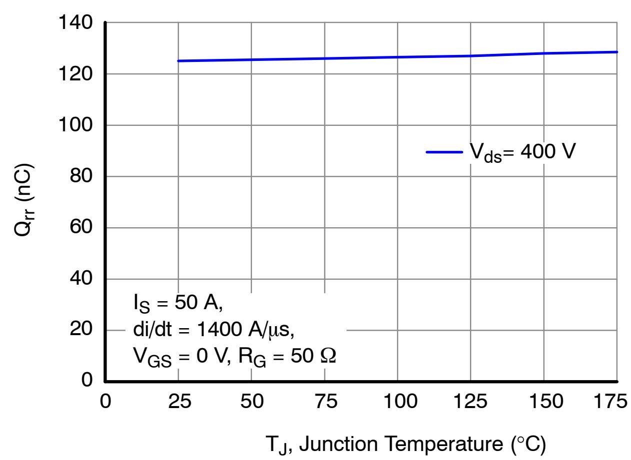


Figure 18. Reverse Recovery Charge Q_{rr} vs. Junction Temperature at V_{DS} = 400 V

TYPICAL CHARACTERISTICS (continued)

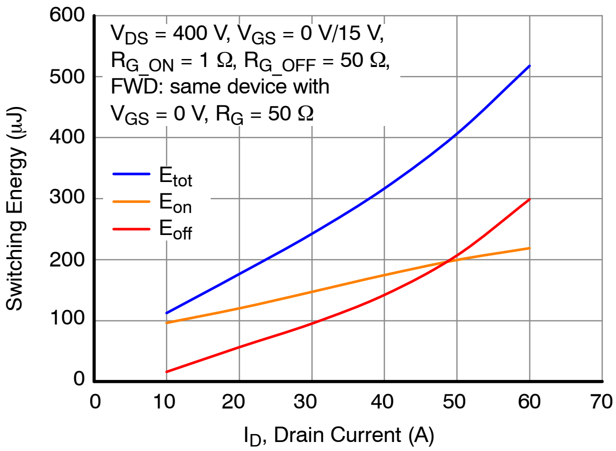


Figure 19. Clamped Inductive Switching Energy vs. Drain Current at V_{DS} = 400 V and T_J = 25 °C

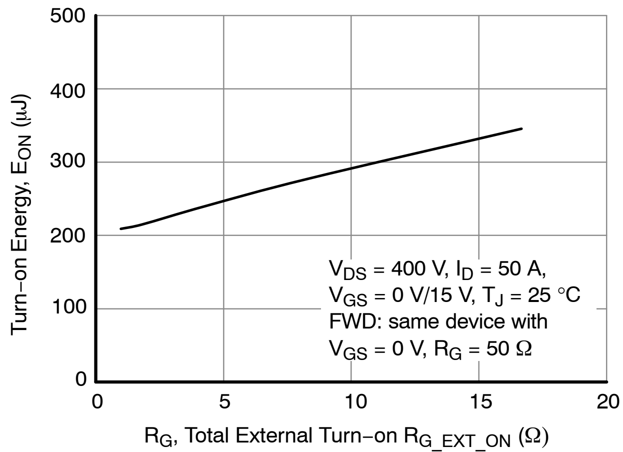


Figure 20. Clamped Inductive Switching Turn−On Energy vs. $R_{G\_EXT\_ON}$

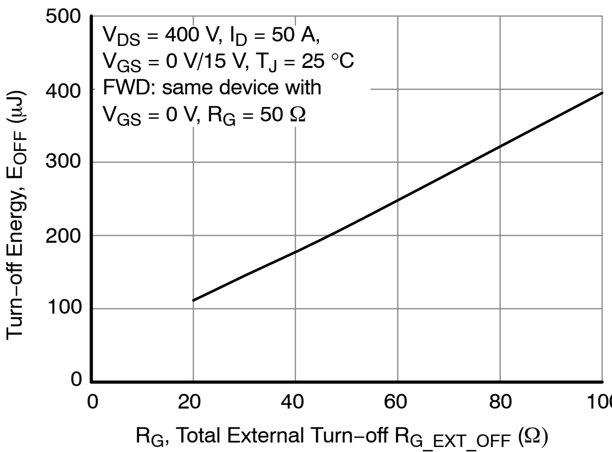


Figure 21. Clamped Inductive Switching Turn−Off Energy vs. $R_{G\_EXT\_OFF}$

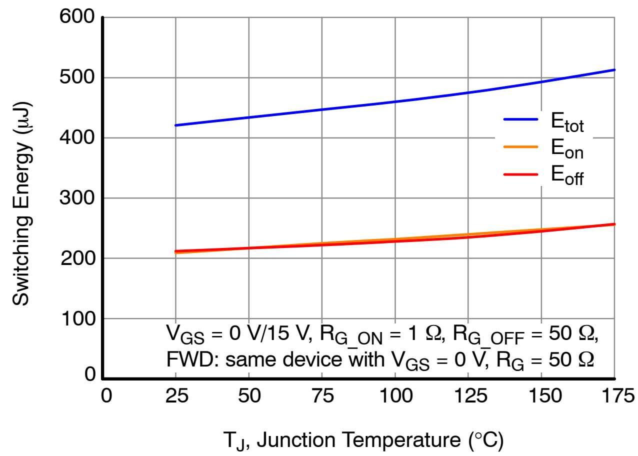


Figure 22. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 400 V and I_D = 50 A

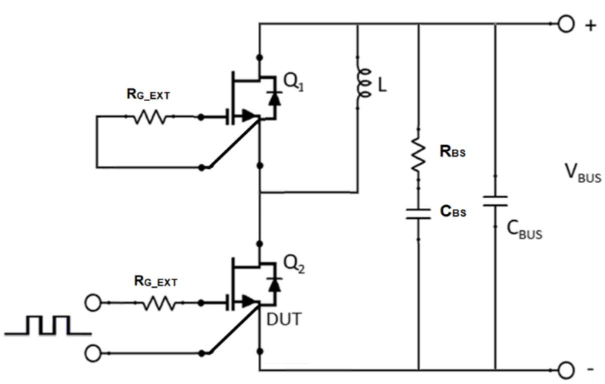


Figure 23. Schematic of the Half-Bridge Mode Switching Test Circuit. Note, a Bus RC Snubber (R_{BS} = 2.5 Ω, C_{BS} =100 nF) is Used to Reduce the Power Loop High Frequency Oscillations.

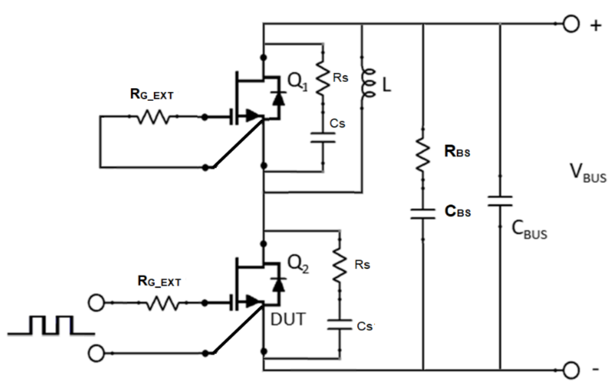


Figure 24. Schematic of the Half-Bridge Mode Switching Test Circuit with device RC Snubbers (R_S = 10 Ω, C_S =300 pF) and a Bus RC Snubber (R_{BS} = 2.5 Ω, C_{BS} =100 nF).

APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

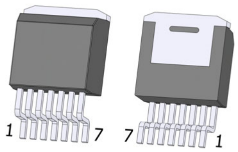
Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at www.onsemi.com.

ORDERING INFORMATION

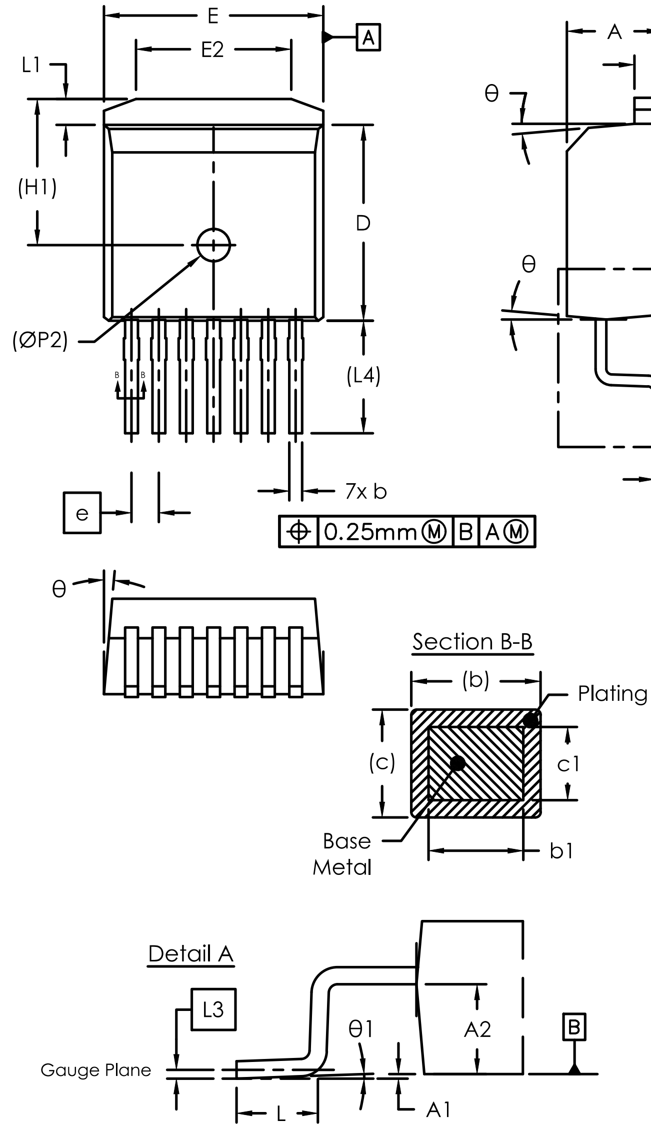
Part Number	Marking	Package	Shipping†
UJ4SC075018B7S	UJ4SC075018B7S	TO-263-7 (Pb-Free, Halogen Free)	800 units / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



TO−263−7 10.18x9.08x4.43, 1.27P
CASE 418BA
ISSUE B

DATE 17 APR 2025



SYM	MILLIMETERS		
	Min	Nom	Max
A	4.30	4.43	4.56
A1	0.00	0.13	0.25
A2	2.45	2.60	2.75
b	0.50	0.60	0.70
b1	0.50	-	-
c	0.40	0.50	0.60
c1	0.40	-	-
c2	1.20	1.30	1.40
D	8.93	9.08	9.23
D1	5.85	6.00	6.15
D2	7.90	8.00	8.10
e	1.27 BSC		
E	10.08	10.18	10.28
E1	6.82	7.22	7.62
E2	6.50	7.55	8.60
E3	3.50	3.60	3.70
H	15.00	15.50	16.00
H1	6.78 REF		
H3	7.30 REF.		
L	1.90	2.20	2.50
L1	0.98	1.20	1.42
L3	0.25 BSC		
L4	5.22 REF		
ØP1	0.65	0.75	0.85
ØP2	1.50 REF		
θ	5°		
θ1	3°		

Notes:

1. Dimensioning and Tolerancing as per ASME Y14.5M, 2018.
2. Controlling Dimension : Millimeters
3. Package body sides exclude mold flash and gate burrs.
4. Dimension L is measured on gauge plane.
5. Dimension c1 and b1 applies to base metal only.

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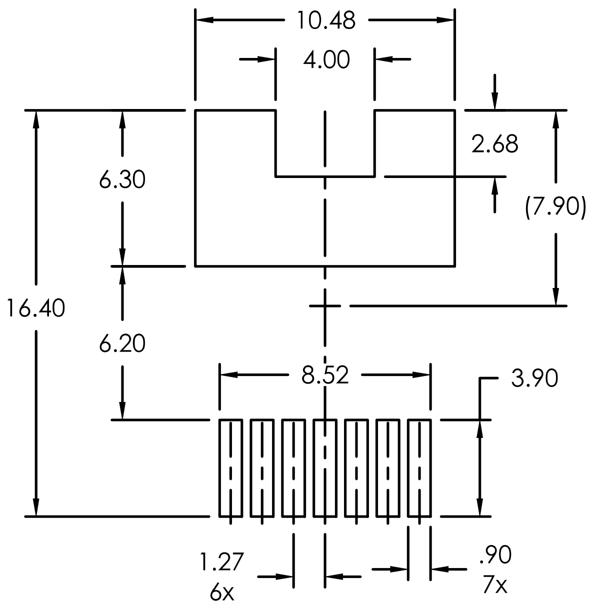
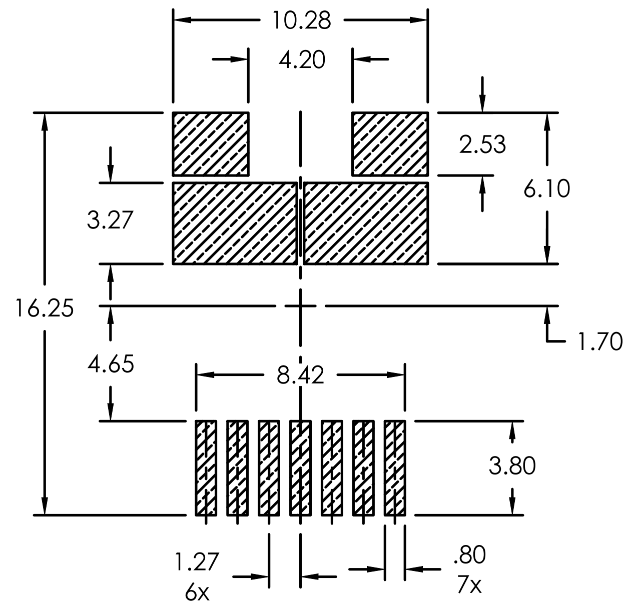
TO−263−7 10.18x9.08x4.43, 1.27P
CASE 418BA
ISSUE B

DATE 17 APR 2025

RECOMMENDED PCB FOOTPRINT

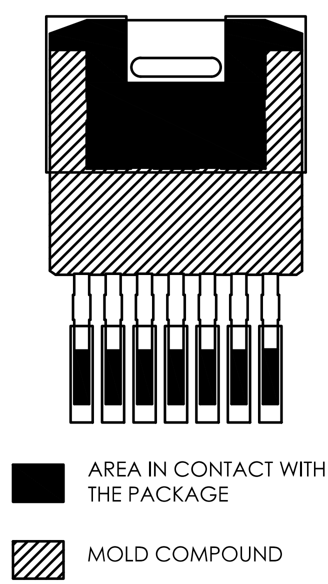


RECOMMENDED STENCIL APERTURE



NOTE: LAND PATTERN AND STENCIL APERTURE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE. END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

PCB FOOTPRINT with PACKAGE OVERLAY



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ADDITIONAL INFORMATION

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