NB6N14SMNG Evaluation Board User's Manual

NB6N14SMNGEVB

Introduction

onsemi has developed the QFN16EVB evaluation board for its high-performance devices packaged in the 16-pin QFN. This evaluation board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the operation of various **onsemi** products. Many QFN16EVBs are dedicated with a device already installed, and can be ordered from www.onsemi.com at the specific device web page.

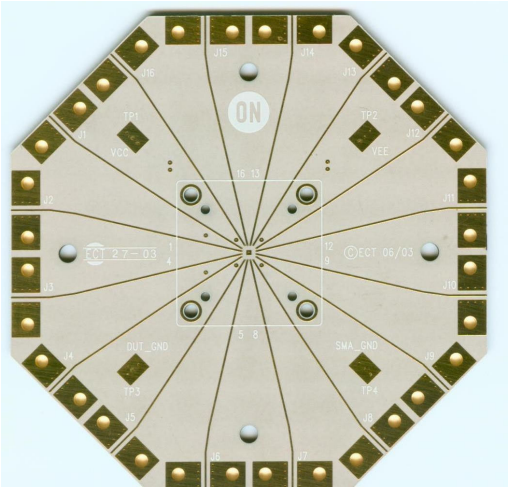
This evaluation board manual contains:

- Information on 16-lead QFN Evaluation Board
- Assembly Instructions
- Appropriate Lab Setup
- Bill of Materials

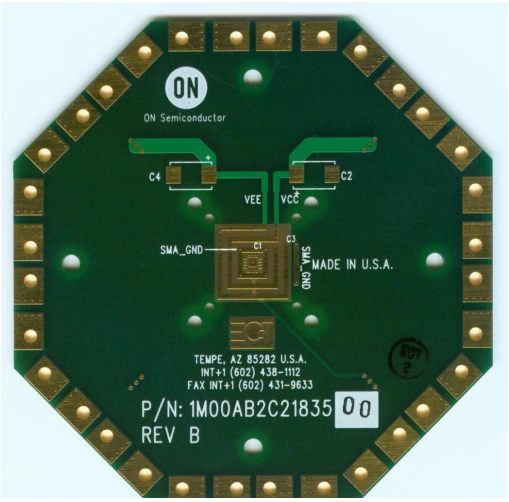
This user's manual provides detailed information on board contents, layout and its use. It should be used in conjunction with an appropriate **onsemi** device datasheet located at www.onsemi.com. The datasheet contains the technical device specifications.

Board Layout

The QFN16 Evaluation Board provides a high bandwidth, 50 Ω controlled impedance environment and is implemented in four layers. The first layer or primary trace layer is 0.008″ thick Rogers RO4003 material, and is designed to have equal electrical length on all signal traces from the device under test (DUT) pins to the SMA connectors. The second layer is the 1.0 oz copper ground plane and is primarily dedicated for the SMA connector ground plane. FR4 dielectric material is placed between the second and third layers and between third and fourth layers. The third layer is also 1.0 oz copper plane. A portion of this layer is designated for the device V_{CC} and DUTGND power planes. The fourth layer is the secondary trace layer.



Top View



Bottom View

Figure 1. Top and Bottom View of the 16 QFN Evaluation Board

© Semiconductor Components Industries, LLC, 2013

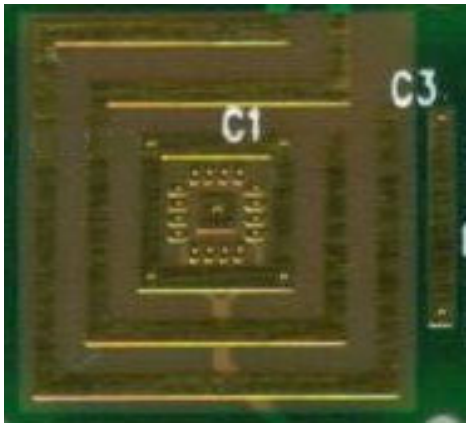


Figure 2. Enlarged Bottom View

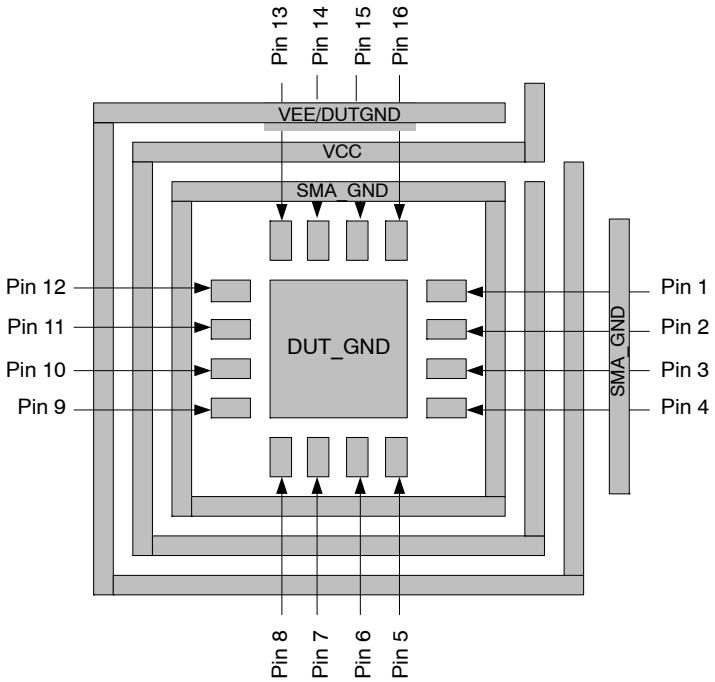


Figure 3. Enlarged Bottom View of the Evaluation Board

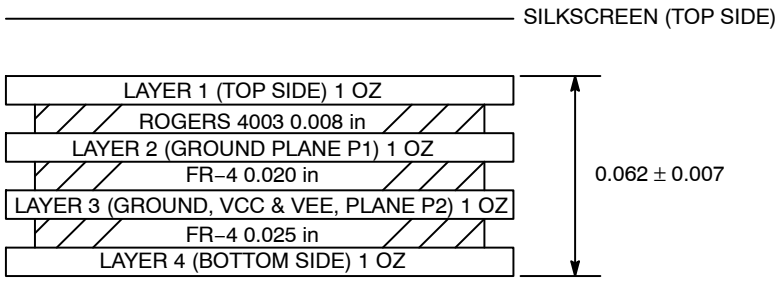
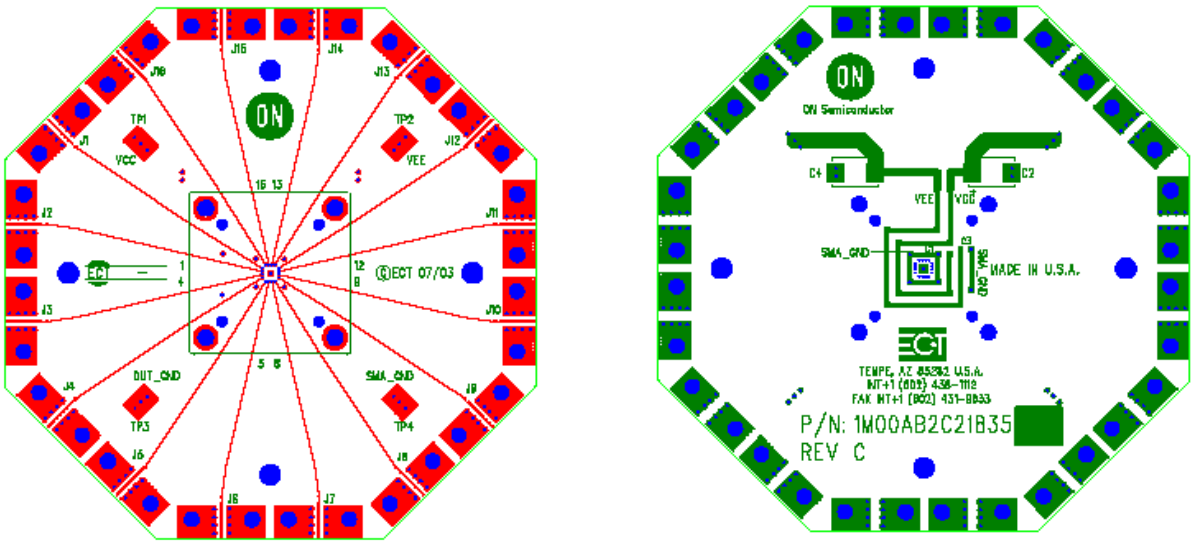


Figure 4. Evaluation Board Layout, 4 Layer

Share Feedback
Your Opinion Matters



Top View **Bottom View**

Figure 5. Evaluation Board Layout

Evaluation Board Assembly Instructions

The QFN−16 evaluation board is designed for characterizing devices in a 50 Ω laboratory environment using high bandwidth equipment. Each signal trace on the board has a via at the DUT pin, which provides an option of placing a termination resistor on the board bottom, depending on the input/output configuration (see Table 1, Configuration for Device: NB6N14S). Table 4 contains the Bill of Materials for this evaluation board.

The QFN16EVB was designed to accommodate a custom QFN−16 socket. Therefore, some external components are installed on the bottom side of the board.

Solder the Device on the Evaluation Board

The soldering of a device to the evaluation board can be accomplished by hand soldering or solder reflow techniques using solder paste. Make sure pin 1 of the device is located properly and all the pins are aligned to the footprint pads. Solder the QFN−16 device to the evaluation board. As mentioned earlier, many QFN16EVBs are dedicated with a device already installed, and can be ordered from onsemi.com at the specific device web page.

Connecting Power and Ground

On the top side of the evaluation board, solder the four surface mount test point clips (anvils) to the pads labeled V_{CC}, V_{EE}/DUTGND, SMAGND, and ExPad. ExPad is connected to the exposed flag of the QFN package. For proper operation, the exposed flag is typically recommended to be tied to V_{EE}/DUTGND, the negative supply of the device.

The positive power supply connector is labeled V_{CC}. Depending on the device, the negative power supply nomenclature is labeled either GND or V_{EE}. To help avoid confusion with the use of this board, the negative supply connector is labeled V_{EE}/DUTGND. SMAGND is the ground for the SMA connectors and is not to be confused with the device ground, V_{EE}/DUTGND. SMAGND and DUTGND can be connected in single-supply applications. The power pin layout and typical connection of the evaluation board is shown in Figure 6.

It is recommended to add bypass capacitors to reduce unwanted noise from the power supplies. Connect 0.1 μF capacitors from V_{CC} and V_{EE}/DUTGND to SMA_GND.

Output Loading/Termination

ECL/PECL/LVPECL Outputs

Most ECL outputs are open emitter and need to be DC loaded and AC terminated to V_{CC} − 2.0 V via a 50 Ω resistor. If no internal resistors are provided on the device, 0402 chip resistor pads are provided on the bottom side of the evaluation board to terminate the ECL driver. Solder the chip resistors to the bottom side of the board between the appropriate input device pads and the ground pads. If internal resistors are provided, the VT pins should be wired to SMAGND. (More information on termination is provided in AND8020).

For standard ECL lab setup and test, a split (dual) power supply is recommended enabling the 50 Ω internal impedance in the oscilloscope, or other measuring instrument, to be used as an ECL output load/termination. By offsetting V_{CC} = +2.0 V, SMAGND = V_{CC} − 2.0 V, (SMAGND is the system ground, 0V); V_{CC} is 2.0 V, and V_{EE}/DUTGND is −3.0 V, −1.3 V or −0.5 V; see Table 2, Power Supply Levels).

Share Feedback
Your Opinion Matters

CML Outputs

Likewise, CML outputs need to be terminated to V_{CC} via a 50 Ω resistor. If no internal resistors are provided on the device, 0402 chip resistor pads are provided on the bottom side of the evaluation board to terminate the CML driver. If internal resistors are provided, the V_T pins should be wired to V_{CC}.

For CML lab setup and test, operation with negative supply voltages is recommended to enable the 50 Ω internal impedance in the oscilloscope, or other measuring instrument, to be used as a CML output termination; (V_{CC} = 0 V, SMAGND = 0 V, and V_{EE}/DUTGND = −5.0 V, −3.3 V, −2.5 V, or −1.8 V).

LVDS Outputs

LVDS outputs are typically terminated with 100 Ω across the Q/$\overline{Q}$ output pair. The 100 Ω can be added on the QFN16EVB, but it is not provided on the board, since there are several user dependent LVDS output measurement techniques.

For LVDS lab setup and test, a single supply is typically used, ie. V_{CC} = 3.3 V and DUTGND = 0 V.

Installing the SMA Connectors

Each configuration indicates the number of SMA connectors needed to populate an evaluation board for a given device. Each input and output requires one SMA connector. Install all the required SMA connectors onto the board and solder the center signal conductor pin to the board on J1 through J16. Please note that the alignment of the signal connector pin of the SMA connector to the metal trace on the board can influence lab results. The launch and reflection of the signals are largely influenced by imperfect alignment and soldering of the SMA connector.

Validating the Assembled Board

After assembling the evaluation board, it is recommended to perform continuity checks on all soldered areas before commencing with the evaluation process. Time Domain Reflectometry (TDR) is another highly recommended validation test.

Share Feedback
Your Opinion Matters

NB6N14SMNGEVB ASSEMBLY

Table 1. CONFIGURATION FOR DEVICE: NB6N14S

	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
Device Pin #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SMA Connector	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No	Yes	Yes
Wire	No	No	No	No	No	No	V_{CC}	No	No	No	No	No	GND	V_{CC}	No	No

NOTE: DUTGND/V_{EE} = Exposed Pad and must be tied to DUTGND/V_{EE}.

CONFIGURATIONS

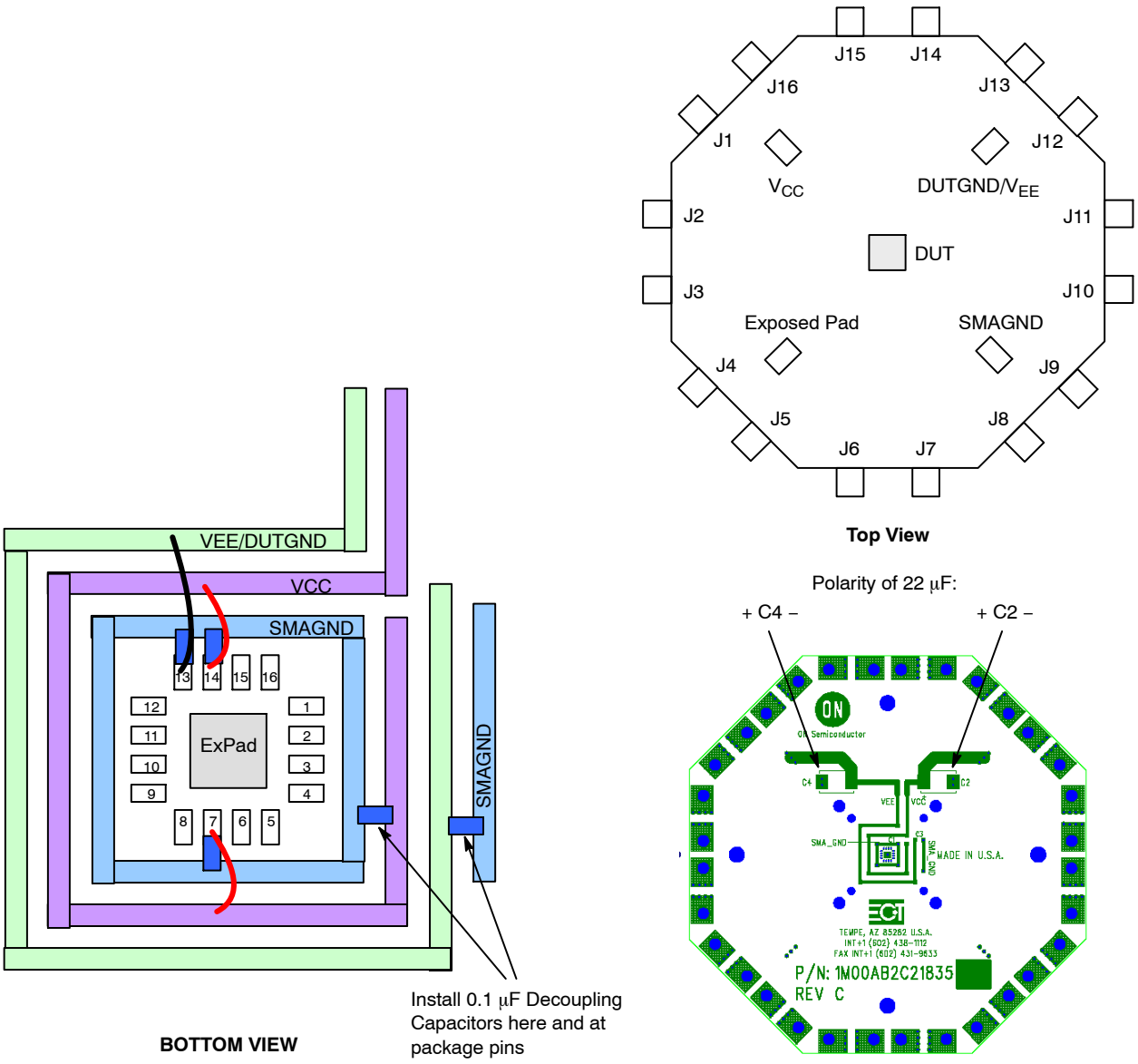
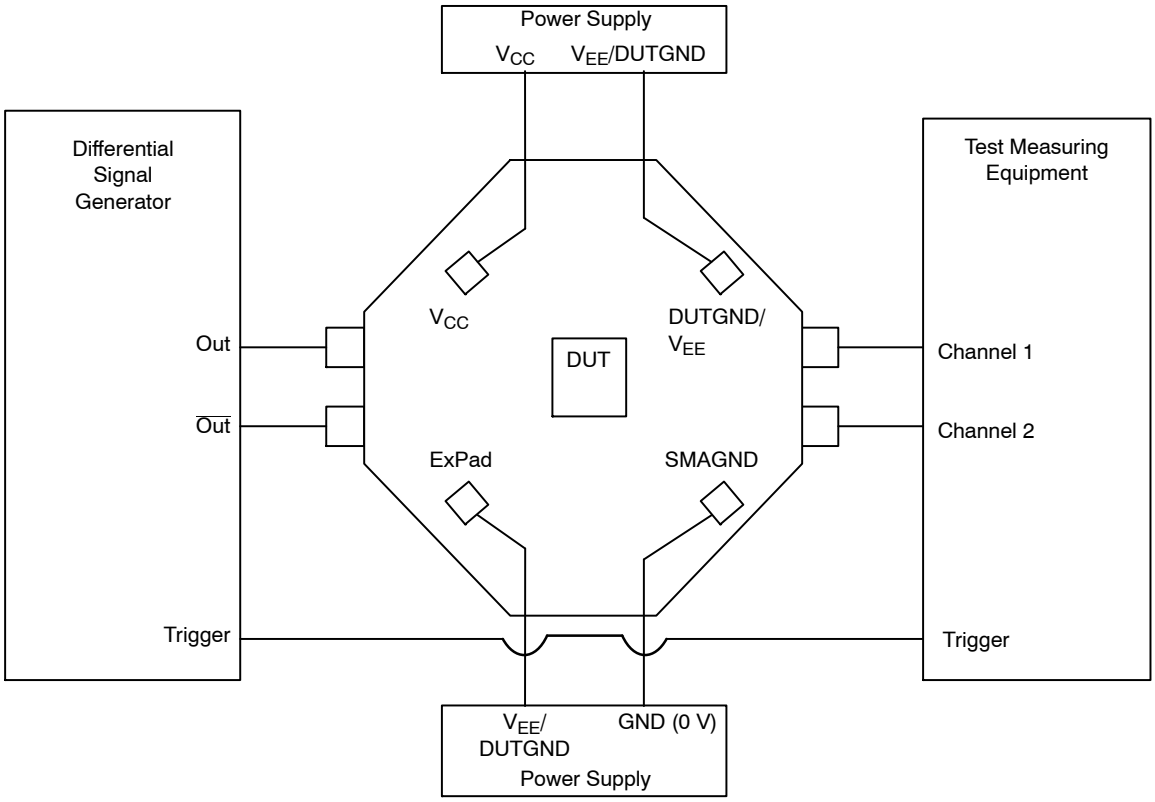


Figure 6. Power Supply Configuration for Device NB6N14S

Share Feedback
Your Opinion Matters

NB6N14SMNGEVB TEST



1. Connect appropriate power supplies to V_{CC}, V_{EE}/DUTGND, SMAGND, and ExPad (see Table 2).
2. Connect a signal generator to the input SMA connectors. Setup input signal according to the device data sheet.
3. Connect a test measurement device to the device's output SMA connectors.

NOTE: The test measurement device must contain 50 Ω termination.

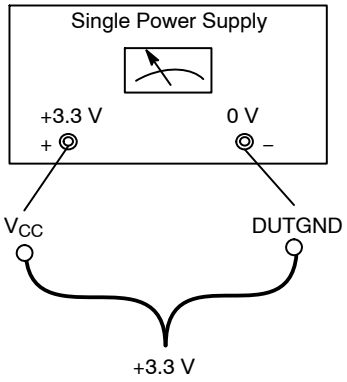
Figure 7. Basic Lab Setup (Typical)

Table 2. POWER SUPPLY LEVELS

Outputs	Power Supply	V_{CC}	V_{EE}/DUTGND	SMAGND	ExPad (typ)
LVDS	2.5 V	+2.5 V	0 V	0 V	V_{EE}/DUTGND
LVDS	3.3 V	+3.3 V	0 V	0 V	V_{EE}/DUTGND

Table 3. NB6xxxS, LVDS OUTPUTS POWER SUPPLY CONFIGURATION

Device Pin Power Supply Convertor	Power Supply
V_{CC}	V_{CC} = +3.3 V
SMAGND	0 V
DUTGND	DUTGND = 0 V



Single Power Supply Configuration

Figure 8. Single Power Supply Connections

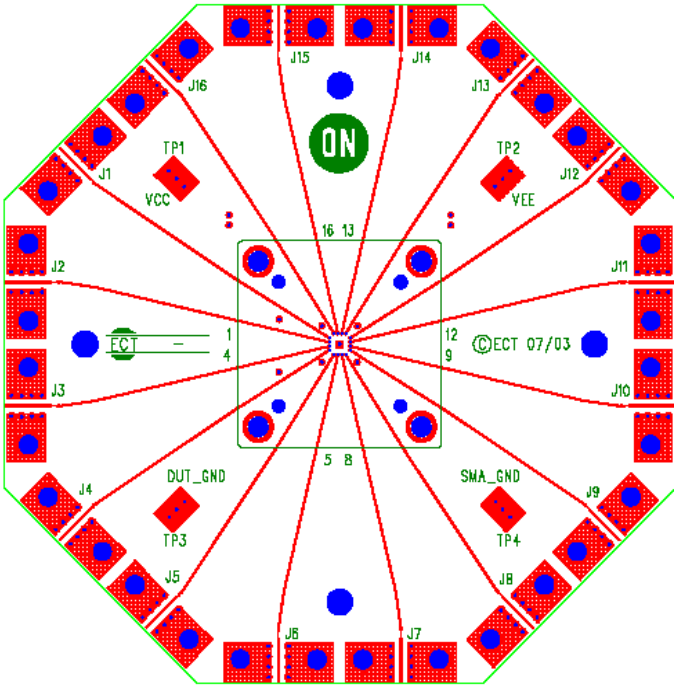
Share Feedback
Your Opinion Matters

Table 4. BILL OF MATERIALS

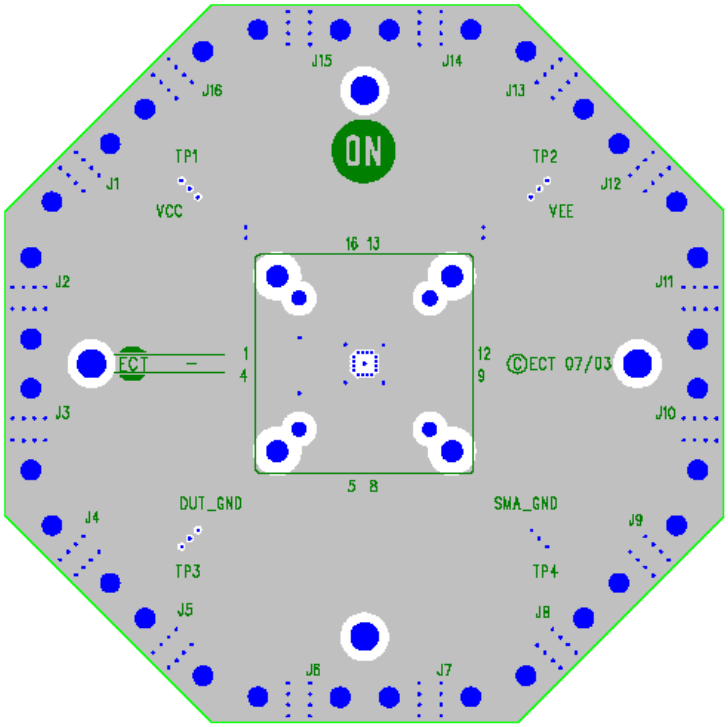
Components	Manufacturer	Description	Part Number	Qty	Web Site
SMA Connector	Rosenberger	SMA Connector, Side Launch, Gold Plated	32K243−40ME3	13	http://www.rosenberger.de http://www.rosenbergerna.com
Surface Mount Test Points	Keystone*	SMT Miniature Test Point	5015	4	http://www.keyelco.com
Chip Capacitor	Kemet*	0402 0.1 μF ±10%	C0402C105K9PACTU	3	http://www.kemet.com
		0603 0.1 μF ±10%	C0603C105K8PACTU	2	
		22 μF ±10%	T495C226K025ATE300	2	
Chip Resistor	Panasonic*	0402 50 Ω ±1% Precision Thick Film Chip Resistor	ERJ−2RKF49R9X	na	http://www.panasonic.com
Evaluation Board	**onsemi**	QFN 16 Evaluation Board	QFN16EVB	1	http://www.onsemi.com
Device Samples	**onsemi**	QFN 16 Package Device	NB6N14SMNG	1	http://www.onsemi.com

* Components are available through most distributors, i.e. www.newark.com, www.digikey.com

Share Feedback
Your Opinion Matters



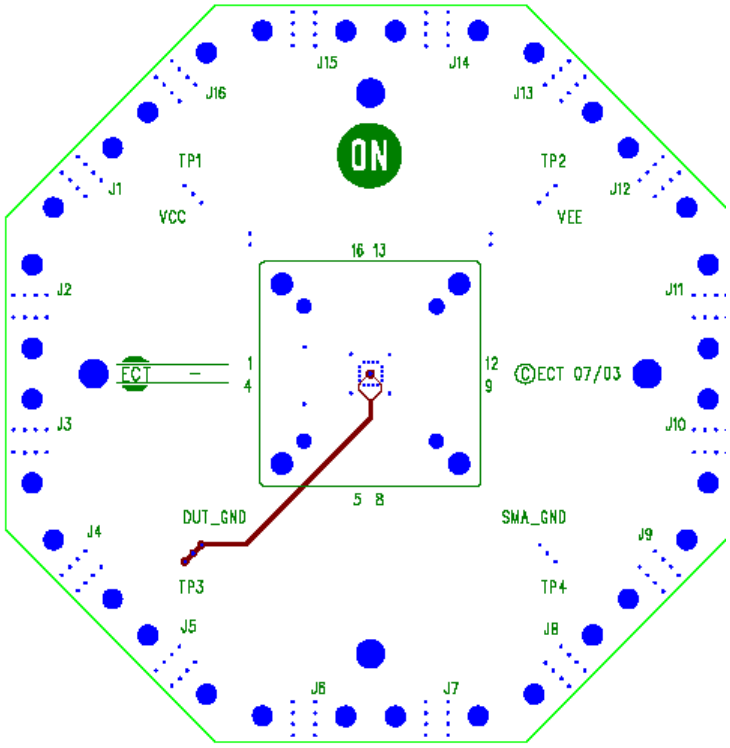
Top Layer



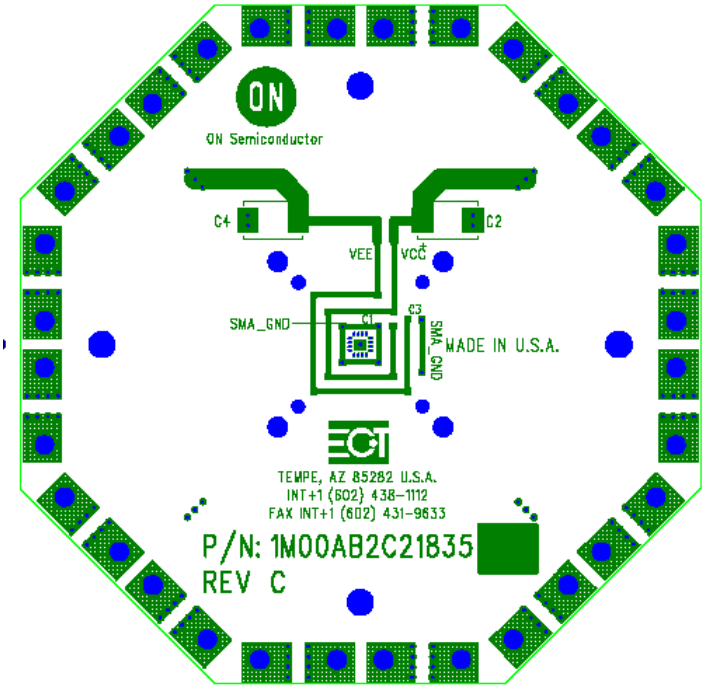
Second Layer (SMA_GND Plane)

Figure 9. Gerber Files

Share Feedback
Your Opinion Matters



Third Layer (DUT_GND Trace)



Bottom Layer

Figure 10. Gerber Files

Share Feedback
Your Opinion Matters

onsemi, ONSEMI, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

The evaluation board/kit (research and development board/kit) (hereinafter the "board") is not a finished product and is not available for sale to consumers. The board is only intended for research, development, demonstration and evaluation purposes and will only be used in laboratory/development areas by persons with an engineering/technical training and familiar with the risks associated with handling electrical/mechanical components, systems and subsystems. This person assumes full responsibility/liability for proper and safe handling. Any other use, resale or redistribution for any other purpose is strictly prohibited.

THE BOARD IS PROVIDED BY ONSEMI TO YOU "AS IS" AND WITHOUT ANY REPRESENTATIONS OR WARRANTIES WHATSOEVER. WITHOUT LIMITING THE FOREGOING, ONSEMI (AND ITS LICENSORS/SUPPLIERS) HEREBY DISCLAIMS ANY AND ALL REPRESENTATIONS AND WARRANTIES IN RELATION TO THE BOARD, ANY MODIFICATIONS, OR THIS AGREEMENT, WHETHER EXPRESS, IMPLIED, STATUTORY OR OTHERWISE, INCLUDING WITHOUT LIMITATION ANY AND ALL REPRESENTATIONS AND WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, NON−INFRINGEMENT, AND THOSE ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE CUSTOM OR TRADE PRACTICE.

onsemi reserves the right to make changes without further notice to any board.

You are responsible for determining whether the board will be suitable for your intended use or application or will achieve your intended results. Prior to using or distributing any systems that have been evaluated, designed or tested using the board, you agree to test and validate your design to confirm the functionality for your application. Any technical, applications or design information or advice, quality characterization, reliability data or other services provided by **onsemi** shall not constitute any representation or warranty by **onsemi**, and no additional obligations or liabilities shall arise from **onsemi** having provided such information or services.

onsemi products including the boards are not designed, intended, or authorized for use in life support systems, or any FDA Class 3 medical devices or medical devices with a similar or equivalent classification in a foreign jurisdiction, or any devices intended for implantation in the human body. You agree to indemnify, defend and hold harmless **onsemi**, its directors, officers, employees, representatives, agents, subsidiaries, affiliates, distributors, and assigns, against any and all liabilities, losses, costs, damages, judgments, and expenses, arising out of any claim, demand, investigation, lawsuit, regulatory action or cause of action arising out of or associated with any unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of any products and/or the board.

This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and may not meet the technical requirements of these or other related directives.

FCC WARNING − This evaluation board/kit is intended for use for engineering development, demonstration, or evaluation purposes only and is not considered by **onsemi** to be a finished end product fit for general consumer use. It may generate, use, or radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment may cause interference with radio communications, in which case the user shall be responsible, at its expense, to take whatever measures may be required to correct this interference.

onsemi does not convey any license under its patent rights nor the rights of others.

LIMITATIONS OF LIABILITY: **onsemi** shall not be liable for any special, consequential, incidental, indirect or punitive damages, including, but not limited to the costs of requalification, delay, loss of profits or goodwill, arising out of or in connection with the board, even if **onsemi** is advised of the possibility of such damages. In no event shall **onsemi**'s aggregate liability from any obligation arising out of or in connection with the board, under any theory of liability, exceed the purchase price paid for the board, if any.

The board is provided to you subject to the license and other terms per **onsemi**'s standard terms and conditions of sale. For more information and documentation, please visit www.onsemi.com.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales