

# NBA3N206SDGEVB

## NBA3N206SDGEVB Evaluation Board User's Manual



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### Introduction

The NBA3N206S is a 3.3 V differential Multipoint (M-LVDS) line Driver and Receiver. NBA3N206S supports Simplex or Half Duplex bus configurations.

The NBA3N206S has Type-2 receivers that detect the bus state with as little as 50 mV of differential input voltage over a common-mode voltage range of -1 V to 3.4 V. Type-2 receivers include an offset threshold of 0.1 V to provide a detectable voltage under open-circuit, idle-bus, and other fault conditions.

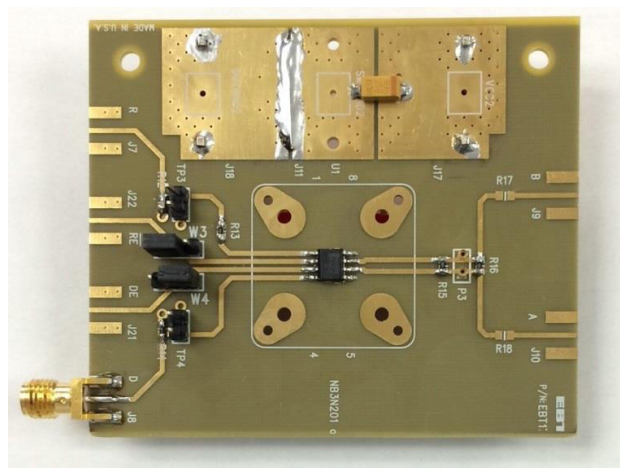
The NBA3N206SDGEVB evaluation board was developed to accommodate the NBA3N206S device. This evaluation board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the operation of the NBA3N206S.

### EVAL BOARD USER'S MANUAL

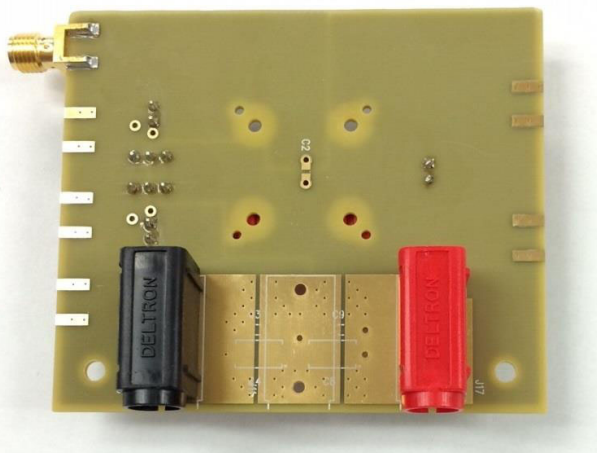
This manual should be used in conjunction with the device datasheet which contains full technical details on the device specifications and operation.

#### Evaluation Board User's Manual Contents:

- NBA3N206S Evaluation Board Information
- Board Features
- Board Layout Map
- Test and Measurement Setup Procedures
- Board Schematic and Bill of Materials



Top View



Bottom View

Figure 1. NBA3N206SDGEVB Evaluation Board

# NBA3N206SDGEVB

## Section 1: Board Features

- Board supplied includes an 8-Pin SOIC.
- Board is configured to operate from a single VCC supply and a single GND supply.
- Single-ended and differential inputs/outputs are accessed via SMA connectors or high impedance probes.
- Board may be configured for bus operation as:
  1. Point-to-Point with Simplex Single Termination
  2. Point-to-Point with Simplex Parallel Termination
  3. Multipoint Two-Node with Single Termination
  4. Multipoint Two-Node with Parallel Termination
- Two 100  $\Omega$  Parallel Termination resistors are mounted on each bus (Driver/Receiver) transceiver I/O pin pair. Resistors may be removed for added configuration flexibility.
- All layers are constructed with FR4 dielectric material.
- The first layer is the primary signal layer, including all of the differential inputs and outputs.
- The second layer is a ground plane. It is dedicated for the SMA ground plane.
- The third layer is a dedicated power plane. A portion of the 3<sup>rd</sup> layer is designated for the device VCC and DUTGND power planes.

## Layer Stack

The NBA3N206SDGEVB SOIC-8 Evaluation Board provides a high bandwidth, 50  $\Omega$  controlled trace impedance environment (100  $\Omega$  line-to-line differential) and is implemented in four layers.

- L1 (Top) Signal
- L2 SMA Ground
- L3 VCC and DUT Ground
- L4 (Bottom) Power Supply Bypass Capacitors, Control Pin Traces and Banana Jacks

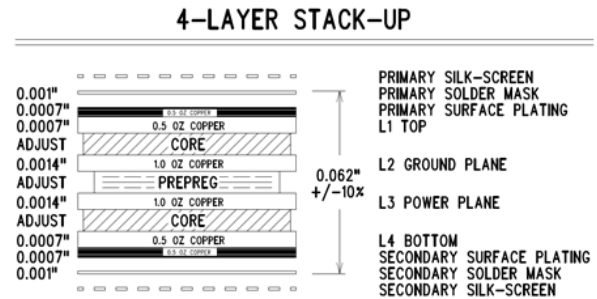


Figure 2. Four Layer Stack-up

## Section 2: Board Layout Map

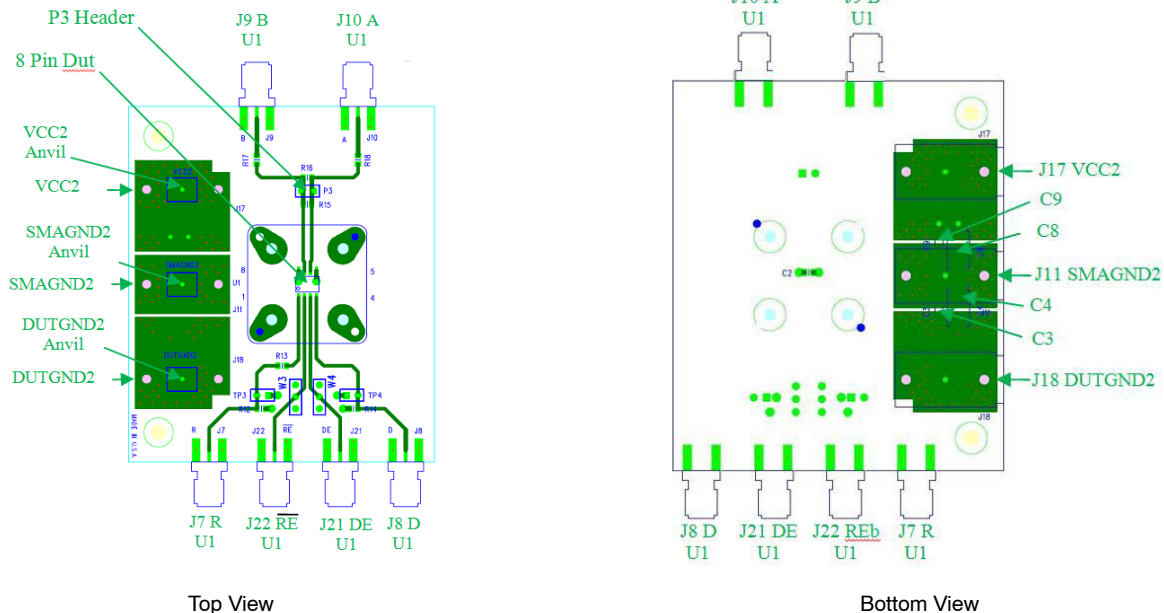


Figure 3. NBA3N206SDGEVB Evaluation Board

# NBA3N206SDGEVB

**Table 1. LOAD BOARD CONNECTIONS AND COMPONENTS**

| Board         | Transceiver | Device Pin   | Function                                                 |
|---------------|-------------|--------------|----------------------------------------------------------|
| VCC2          | U1 (8 Pin)  | U1 Pin 8     | VCC2 Power Supply connection point to U1                 |
| VCC2 Anvil    | U1 (8 Pin)  | U1 Pin 8     | Alternative connection point for VCC2                    |
| SMAGND2       | U1 (8 Pin)  | –            | U1 SMA (J7/8/9/10/21/22) ground shields connection point |
| SMAGND2 Anvil | U1 (8 Pin)  | –            | Alternative connection point for U1 SMA shields          |
| DUTGND2       | U1 (8 Pin)  | U1 Pin 5     | U1 DUT ground pin                                        |
| DUTGND2 Anvil | U1 (8 Pin)  | U1 Pin 5     | Alternative connection point for U1 DUT ground pin       |
| J7 R          | U1 (8 Pin)  | U1 Pin 1     | U1 R input (Note 1)                                      |
| J8 D          | U1 (8 Pin)  | U1 Pin 4     | U1 D input                                               |
| J9 B          | U1 (8 Pin)  | U1 Pin 7     | U1 B input/output (Note 1)                               |
| J10 A         | U1 (8 Pin)  | U1 Pin 6     | U1 B input/output (Note 1)                               |
| J21 DE        | U1 (8 Pin)  | U1 Pin 3     | U1 DE input (Note 1)                                     |
| J22 REb       | U1 (8 Pin)  | U1 Pin 2     | U1 REb input (Note 1)                                    |
| P3 Header     | U1 (8 Pin)  | U1 Pins 6, 7 | U2 Connection Header for A & B                           |
| TP3           | U1 (8 Pin)  | U1 Pin 1     | Test Point for U1 R input                                |
| TP4           | U1 (8 Pin)  | U1 Pin 4     | Test Point for U1 D input                                |
| W3 Pad        | U1 (8 Pin)  | U1 Pin 2     | Program point for U1 Reb                                 |
| W4 Pad        | U1 (8 Pin)  | U1 Pin 3     | Program point for U1 DE                                  |
| *R12          | U1 (8 Pin)  | U1 Pin 1     | U1 15pF R pin                                            |
| R13           | U1 (8 Pin)  | U1 Pin 1     | U1 0 $\Omega$ R pin                                      |
| R14           | U1 (8 Pin)  | U1 Pin 4     | U1 D input optional termination location                 |
| R15           | U1 (8 Pin)  | U1 Pins 6, 7 | U1 100 $\Omega$ termination location                     |
| R16           | U1 (8 Pin)  | U1 Pins 6, 7 | U1 100 $\Omega$ termination location                     |
| R17           | U1 (8 Pin)  | U1 Pins 7    | U1 0 $\Omega$ A pin                                      |
| R18           | U1 (8 Pin)  | U1 Pins 6    | U1 0 $\Omega$ B pin                                      |

\*Replaced with  $C_L=15\text{pF}$  capacitor

1. Not populated on board

## NBA3N206SDGEVB

### Section 3: Test and Management Setup Procedures

#### Basic Operation Setup

1. Set VCC to 3.3V
2. Set DE, Move Jumper to Logic High
3. Set REb, Move Jumper to Logic Low
4. Apply LVCMOS Input Signal to D. (See datasheet for appropriate levels)
5. Monitor Differential Bus Voltage  $V_{AB}$  with a *Differential Probe*
6. Monitor Receiver Output  $V_R$  with a *Hi-Z Probe*

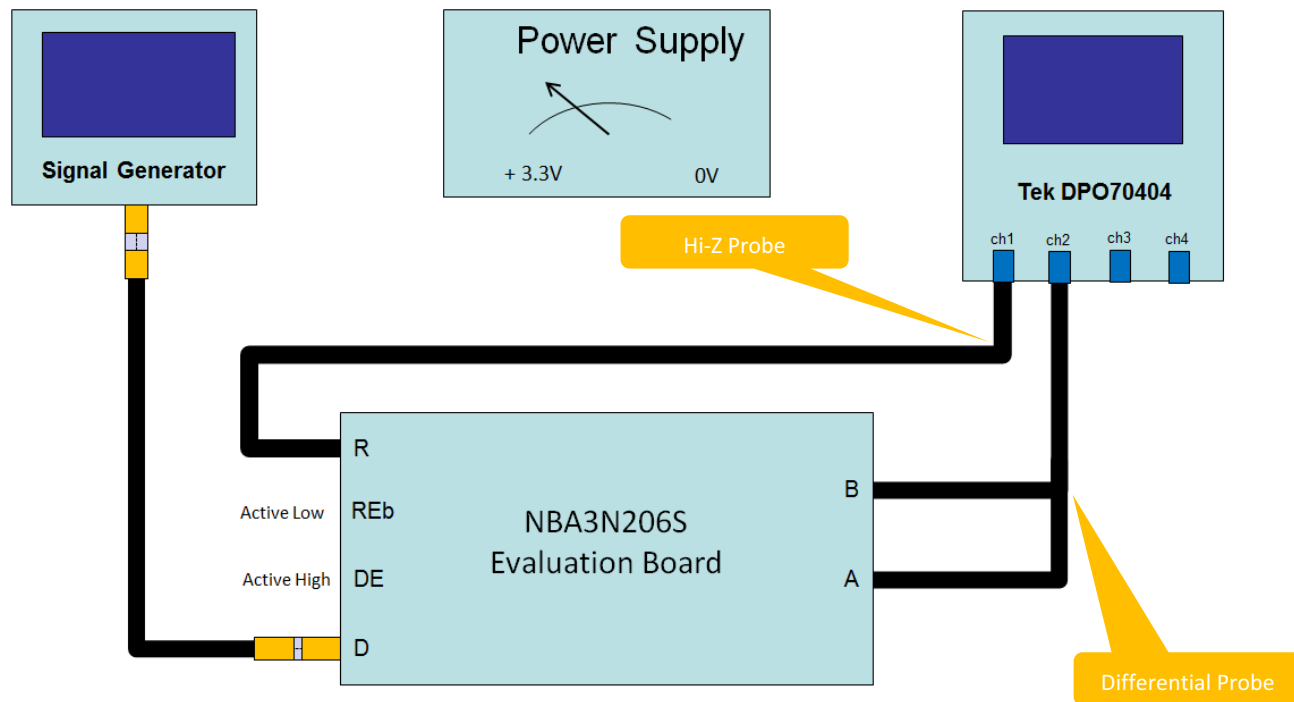


Figure 4. NBA3N206S Evaluation Board Test Block Diagram

#### Equipment Used (or equivalent)

1. Generator (HP 8133A or similar)
2. Oscilloscope (Tektronix TDS8000 or similar)
3. Power Supply (Agilent #6624A DC or similar)
4. Digital Voltmeter
5. Differential Probe
6. Hi-Z Probe

## Test Configurations

**Simplex Theory Configurations:** Data flow is unidirectional and Point-to-Point from one Driver to one Receiver. NBA3N206SDG devices provide a high signal current allowing long drive runs and high noise immunity. Single terminated interconnects yield high amplitude levels.

Parallel terminated interconnects yield typical MLVDS amplitude levels and minimize reflections. See Figures 5 and 6. NBA3N206SDG can be used as a driver or as a receiver.

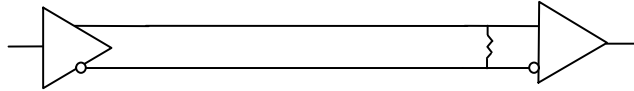


Figure 5. Point-to-Point Simplex Single Termination

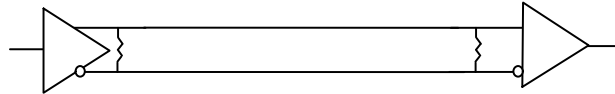


Figure 6. Parallel-Terminated Simplex

**Simplex Multidrop Theory Configurations:** Data flow is unidirectional from one Driver with one or more Receivers (Multiple boards required). Single terminated interconnects yield high amplitude levels. Parallel terminated interconnects yield typical MLVDS amplitude

levels and minimize reflections. Header P3 may be used as needed to interconnect transceivers to each other or to a bus. See Figures 1, 7, and 8. A NBA3N206SDG can be used as the driver or as a receiver.

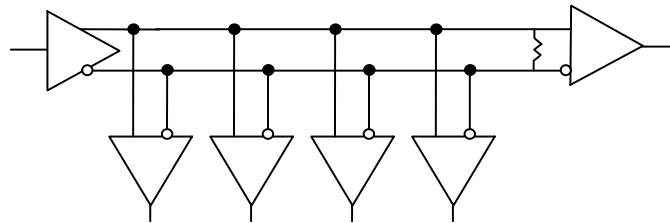


Figure 7. Multidrop or Distributed Simplex with Single Termination

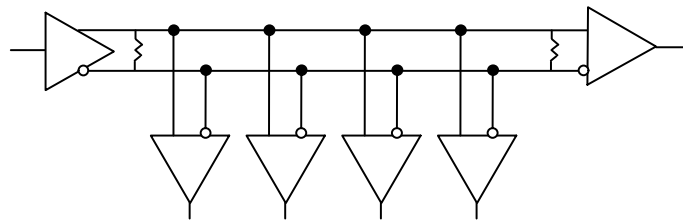


Figure 8. Multidrop or Distributed Simplex with Double Termination

**Half Duplex Multinode Multipoint Theory Configurations:** Data flow is unidirectional and selected from one of multiple possible Drivers to multiple Receives. One “Two Node” multipoint connection can be accomplished with a single board. Multipoint connection with more than two nodes require multiple boards. Parallel

terminated interconnects yield typical MLVDS amplitude levels and minimize reflections. Header P3 may be used as needed to interconnect transceivers to each other or to a bus. See Figure 9. NBA3N206SDG can be used as a driver or as a receiver.

## NBA3N206SDGEVB

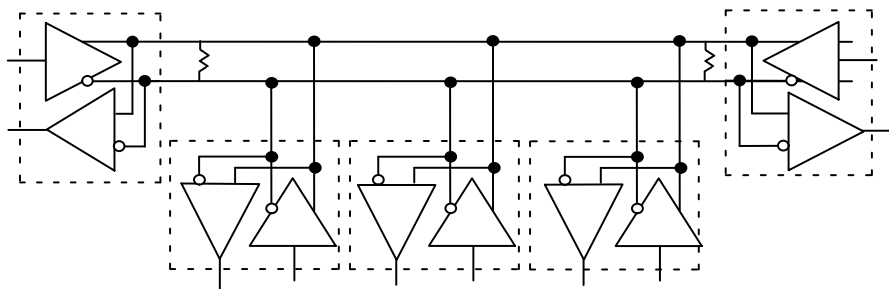


Figure 9. Multinode Multipoint Half Duplex (requires Double Termination)

### Output Waveforms

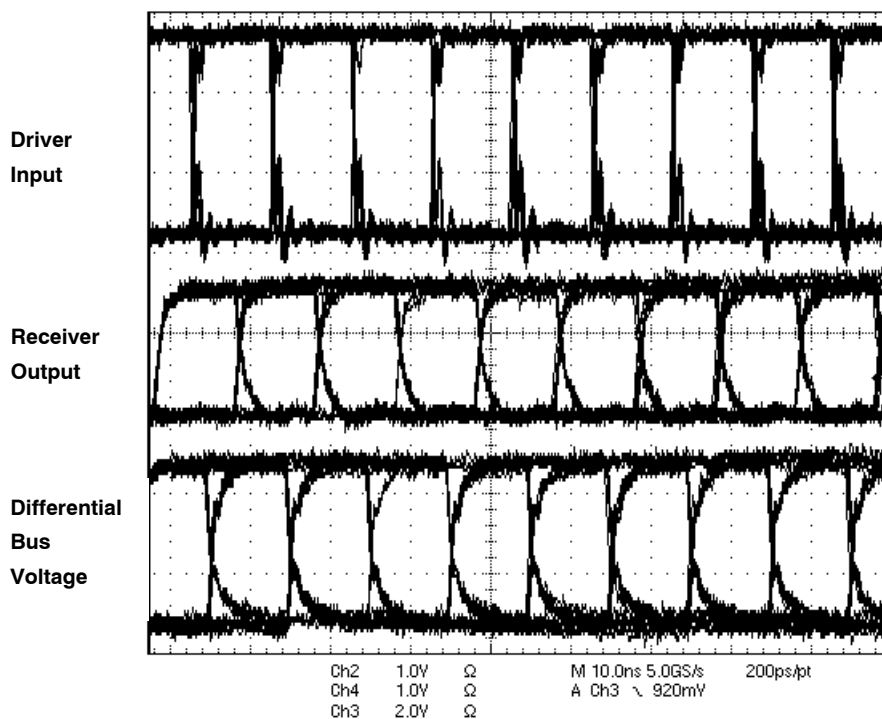


Figure 10. High Impedance Output Termination

Figure 10 shows typical NBA3N206S waveforms. The Driver Input is supplied by a 100 Mbps data signal via an HP8133A generator. The Receiver Output ( $V_R$ ) can be

monitored using a *Hi-Z probe*; the Differential Bus Voltage ( $V_{AB}$ ) can be monitored using a *Differential probe*.

# NBA3N206SDGEVB

## Section 4: Board Schematic and Bill of Materials

### Board Schematic

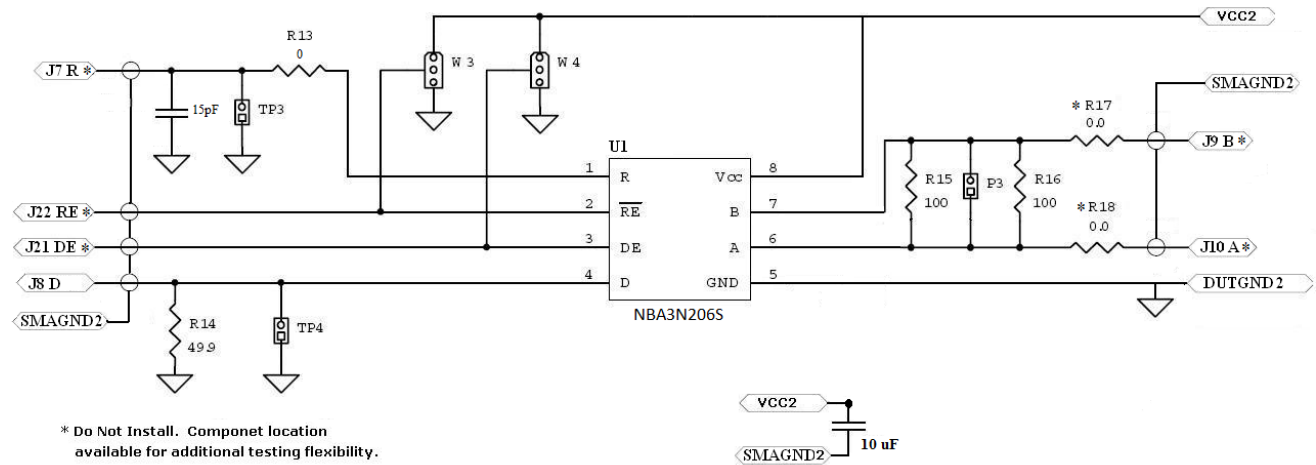


Figure 11. Board Schematic

Table 2. BILL OF MATERIALS AND LAMINATION STACKUP

| Component Designation  | Case | Value        | Manufacturer     | Part Number        | Description                        | Qty |
|------------------------|------|--------------|------------------|--------------------|------------------------------------|-----|
| U1                     |      |              | ON Semiconductor | NBA3N206S          |                                    | 1   |
| J18                    |      |              | Deltron          | 571-0100           | Banana Jacks – Black               | 1   |
| J17                    |      |              | Deltron          | 571-0500           | Banana Jacks – Red                 | 1   |
| J8                     |      |              | Johnson          | #142-0711-821      | SMA Connector Side Launch Narrow   | 1   |
| P3                     |      |              | AMP              | 4-103239-0x2       | Header (make from 4-103239-0)      | 1   |
| VCC2, SMAGND2, DUTGND2 |      |              | Keystone         | 5015               | Anvil Clips                        | 6   |
| W3, W4                 |      |              | FCI              | 68000-103HLF       | 3 Pin Header                       | 2   |
| TP3, TP4               |      |              | 3M               | 961102-6404-AR     | 2 Pin Header                       | 2   |
| R14                    | O603 | 50 $\Omega$  | Panasonic        |                    | Precision Thick Film Chip Resistor | 1   |
| R15, R16               | O603 | 100 $\Omega$ | Panasonic        |                    | Precision Thick Film Chip Resistor | 2   |
| R13, R17, R18          | O603 | 0 $\Omega$   | Panasonic        |                    | Precision Thick Film Chip Resistor | 1   |
| C4                     |      | 10 $\mu$ F   | KEMET            | C1210X106K3RACTU   | Chip Capacitor                     | 1   |
| C11                    | 0603 | 15 pF        | Murata           | GRM1555C1E150JA01D | Chip Capacitor                     | 1   |

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