

MT9P401 Evaluation Board User's Manual



EVAL BOARD USER'S MANUAL

The evaluation boards are designed to demonstrate the features of ON Semiconductor's image sensors products. This headboard is intended to plug directly into the Demo 2X system. Test points and jumpers on the board provide access to clock, I/Os and other miscellaneous signals.

- Clock Input
 - ◆ Default – 24 MHz crystal oscillator
 - ◆ Optional Demo 2X controlled MClk
- Two Wire Serial Interface
 - ◆ Selectable base address
- Parallel Interface
- MIPI Interface
- ROHS Compliant

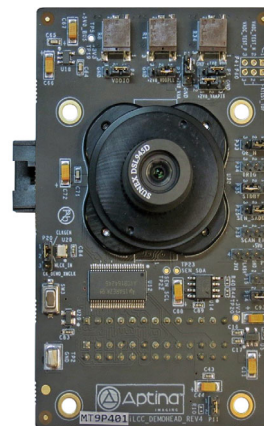


Figure 1. MT9P401 Evaluation Board

The schematic diagram illustrates the power and signal connections for the MT9P001 48ILCC MI5100, C18C sensor module. The sensor is connected to a 5V_BUS, a 3.3V power supply, and an adjustable power supply. The sensor is connected to a Level Translator, a 24MHz oscillator, a Reset IC, an I2C Level Translator, and an EEPROM. The sensor is also connected to a Header Jumper Connector and an RJ45 module.

Power Connections:

- 5V_BUS:** Connected to the sensor's VDDIO, VDDIO_LS, and VDDIO.
- 3.3V:** Connected to the sensor's +3V3, +VDDIO_LS, and +VDDIO_LS.
- Adjustable Power Supply:** Connected to the sensor's VDDIO, VDDIO_LS, and VDDIO.

Signal Connections:

- Level Translator:** Connected to the sensor's LV, FV, PIXEL_CLK, and Dou[0.11].
- 24MHz Oscillator:** Connected to the sensor's CK_SEN_MCLK.
- Reset IC:** Connected to the sensor's SEN_RST_N.
- I2C Level Translator:** Connected to the sensor's SEN_I2C.
- EEPROM:** Connected to the sensor's +3V3 and Default Address (0xA8).
- Header Jumper Connector:** Connected to the sensor's RST/OE/TRIG/SCAN_EN/FLASH/STDBY/ATEST.
- RJ45:** Connected to the sensor's CLK_P/CLK_N and DATA_P/DATA_N.

Figure 2. Block Diagram of MT9P401I12STCH-B-GEVB

MT9P401I12STCH-B-GEVB

Top View

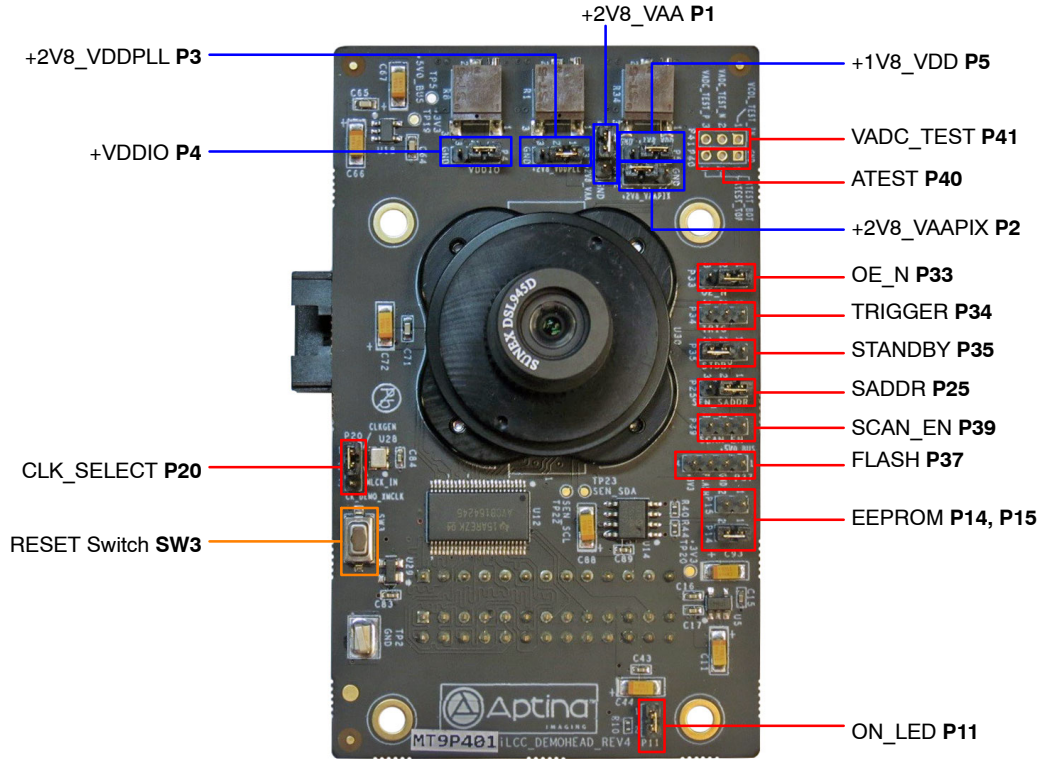


Figure 3. Top View of Evaluation Board – Default Jumpers

Bottom View

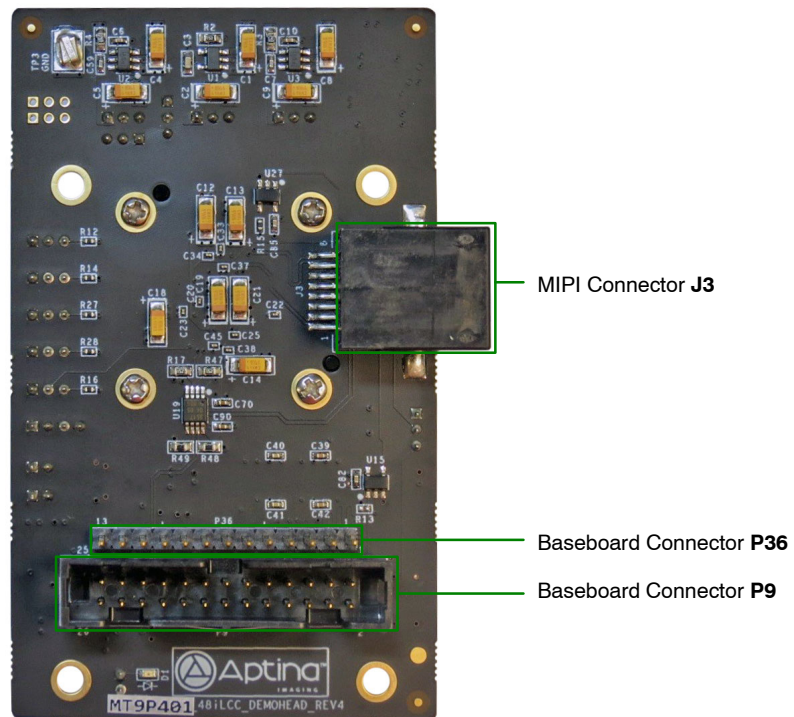


Figure 4. Bottom View of the Evaluation Board – Connector

Jumper Pin Locations

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.

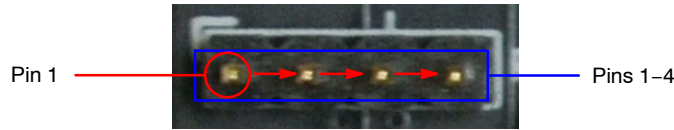


Figure 5. Pin Locations for a Single Jumper.
Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right

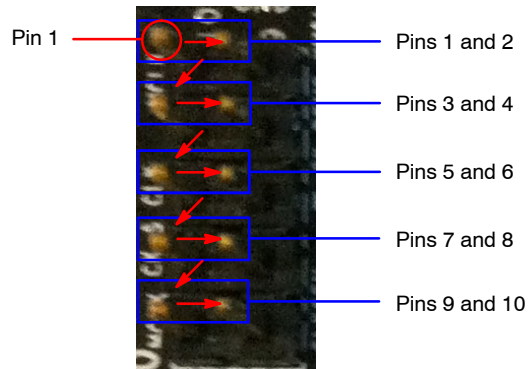


Figure 6. Pin Locations and Assignments of Grouped Jumpers.
Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture

Jumper/Header Functions & Default Positions

Table 1. JUMPERS AND HEADERS

Jumper/Header No.	Jumper/Header Name	Pins	Description
P1	+2V8_VAA	1-2 (Default)	Connects to on-board +2V8_VAA power supply
		2-3	External power supply connection
P2	+2V8_VAAPIX	1-2 (Default)	Connects to on-board +2V8_VAAPIX power supply
		2-3	External power supply connection
P3	+2V8_VDDPLL	1-2 (Default)	Connects to on-board +2V8_VDDPLL power supply
		2-3	External power supply connection
P4	+VDDIO	1-2 (Default)	Connects to on-board +VDDIO power supply
		2-3	External power supply connection
P5	+1V8_VDD	1-2 (Default)	Connects to on-board +1V8_VDD power supply
		2-3	External power supply connection
P11	LED_ON	1-2 (Default)	Connects to on-board LED to indicate power on

MT9P401I12STCH-B-GEVB

Table 1. JUMPERS AND HEADERS (continued)

Jumper/Header No.	Jumper/Header Name	Pins	Description
P14, P15	EEPROM ADDR	P14 Closed, P15 Open (Default)	EEPROM Address set to 0xA8
		P14 Open, P15 Open	EEPROM Address set to 0xAC
		P14 Open, P15 Closed	EEPROM Address set to 0xA4
		P14 Closed, P15 Closed	EEPROM Address set to 0xA0
P20	CLK_SELECT	1–2 (Default)	Master Mode on-board oscillator
		2–3	Master Mode Demo 2X clock
P25	SADDR	1–2 (Default)	I ² C Address set to 0x90
		2–3	I ² C Address set to 0xBA
P33	OE_N	1–2 (Default)	Parallel interface output
		2–3	Non-parallel interface output
P34	TRIGGER	Open (Default)	External connection to snapshot trigger at Pin 2
P35	STANDBY	2–3 (Default)	Set to Normal Mode
		1–2	Set to Standby Mode
P37	FLASH	Open (Default)	External connection to snapshot flash at Pin 3
P40	ATEST	2	ATEST_BOT
		3	ATEST_TOP
P41	VADCTEST	1	VADC_TEST_IN
		2	VADC_TEST_N
		3	VADC_TEST_P
SW3	RESET	N/A	When pushed, 240 ms reset signal will be sent to MT9P401

Interfacing to ON Semiconductor Demo 2X Baseboard

The ON Semiconductor Demo 2X baseboard has a similar 26-pin connector and 13-pin connector which mate

with P9 and P36 of the headboard. The four mounting holes secure the baseboard and the headboard with spacers and screws.

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