

NCV7424V1GEVB



NCV7424 Quad LIN Transceiver Evaluation Board User's Manual

ON Semiconductor®

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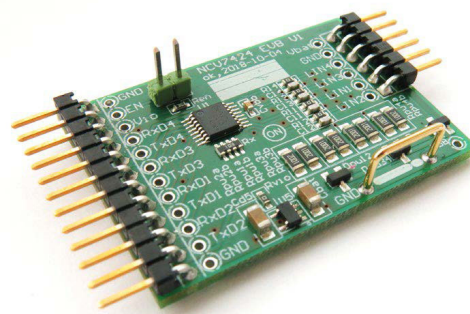
EVAL BOARD USER'S MANUAL

INTRODUCTION

This document describes the evaluation board for the ON Semiconductor four channel LIN transceiver NCV7424. The board provides basic connections for a device evaluation.

EVALUATION BOARD FEATURES

- Two one-row pin header providing access to all the device pins, enables easy insertion of the evaluation board into a more complex application setup.
- On-board 5 V LDO for RxD1–4 pull-up resistors and EN input
- Standard LIN master terminations
- Position for optional ESD protection



NCV7424V1GEVB
Evaluation Board

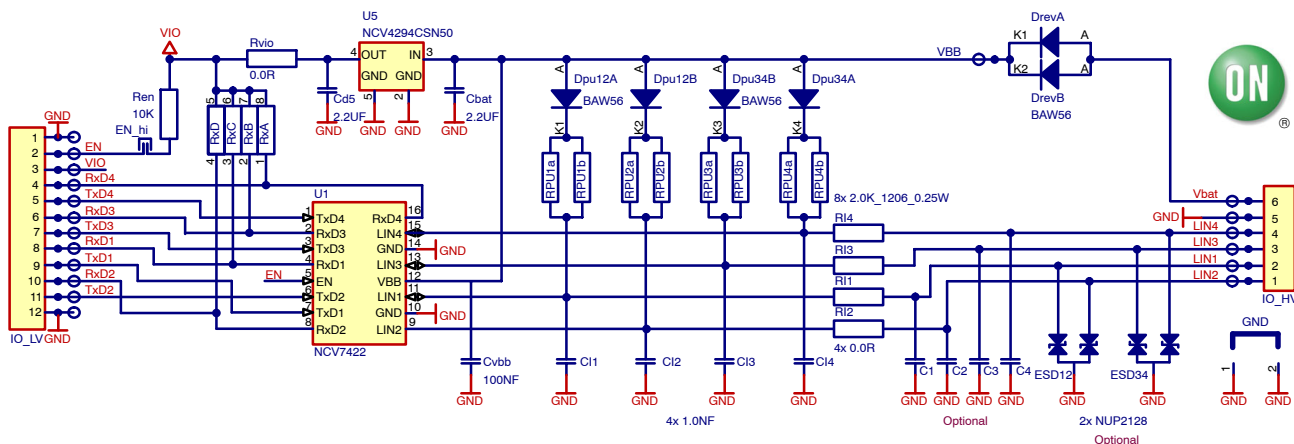


Figure 1. NCV7424 Evaluation Board Schematic

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Table 1. ABSOLUTE MAXIMUM RATINGS

Rating	Pins	Min	Max	Unit
Battery supply voltage	Vbat	-45	45	V
Digital inputs/outputs supply voltage	VIO (Rvio not used)	-0.3	7	V
Digital inputs/outputs voltage	TxD1-2, RxD1-2, EN	-0.3	7	V
LIN bus line voltage	LIN1-4	-45	45	V
NCV7424 junction temperature		-40	+150	°C
Board temperature		-40	+125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. RECOMMENDED BOARD OPERATING CONDITIONS

Rating	Pins	Min	Max	Unit
Battery supply voltage	Vbat	5	18	V
Digital inputs/outputs supply voltage	VIO (Rvio not used)	2.8	5.5	V
Digital inputs/outputs voltage	TxD1-4, RxD1-4, EN	0	VIO	V
LIN bus line voltage	LIN1, LIN2	0	Vbat	V
NCV7424 junction temperature		-40	+150	°C
Board temperature		-40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

OPERATIONAL GUIDELINES

NCV7424 evaluation board allows easy evaluation of NCV7424 four channel LIN transceiver. It provides connection to all the device's pins as well as positions for all the necessary master/slave LIN bus external components.

Configurations and assembly options are listed in Table 3. For more information please check NCV7424 transceiver datasheet at www.onsemi.com.

Table 3. ASSEMBLY OPTIONS AND CONFIGURATIONS

Component	Master (Default)	Slave	Function
Dpu12, Dpu34	BAW56	-	Master pull-up diodes
Rpu1-4a/b	2.0k	-	Master pull-up resistors
Cl1-4	1nF	220pF	LIN bus capacitors
C1-4	-	-	LIN bus capacitors
RI1-4	0R		LIN bus serial impedance
ESD1-4	optional		LIN bus ESD protections
Rvio	0R		Connection on-board LDO to TxD1/2 and EN1/2 pull-up resistors. If removed, external supply can be used (connected to VIO).
EN_hi	Closed		EN1/2 pin connections: Open = EN weak internal pull-down = Sleep mode Closed = EN pulled up to VIO (5 V by default) = Normal mode

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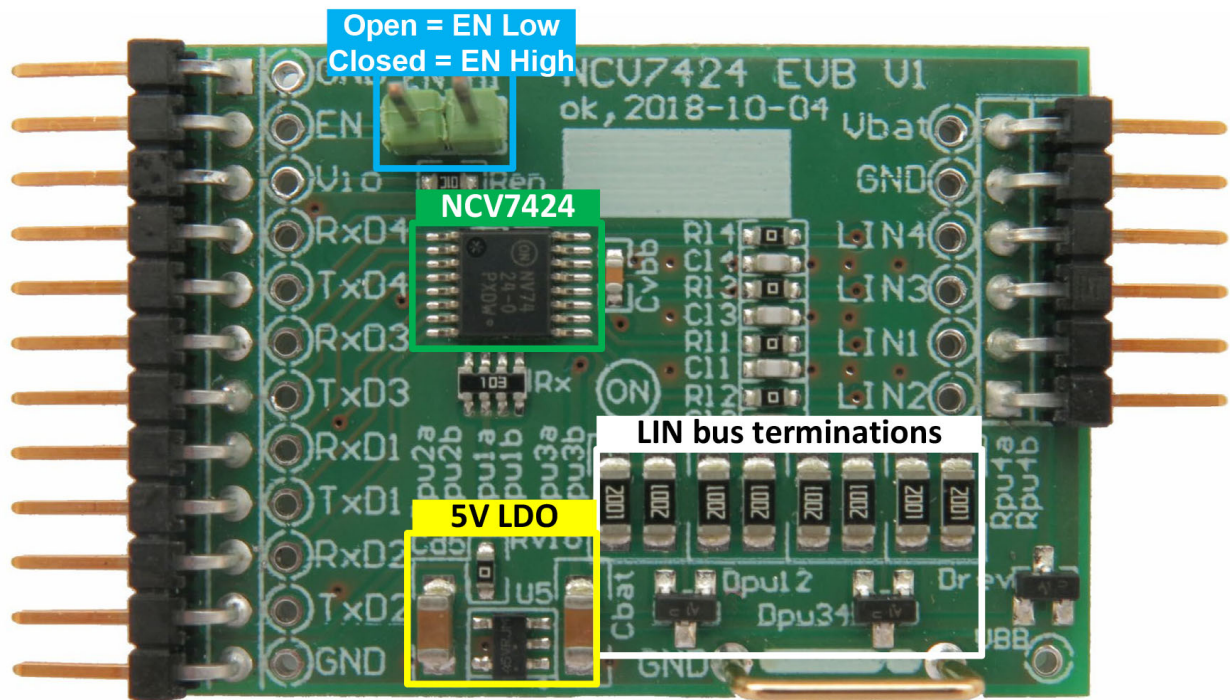


Figure 2. NCV7424 Evaluation Board Picture, Top Side

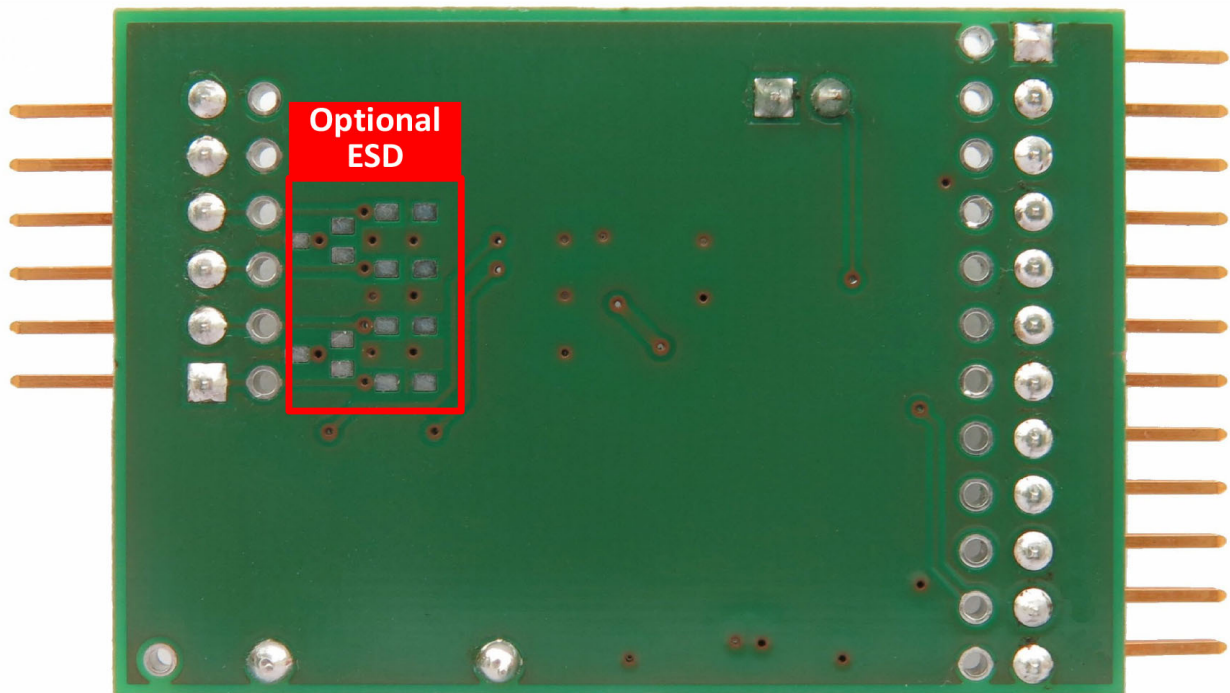


Figure 3. NCV7424 Evaluation Board Picture, Bottom Side

NCV7424V1GEVB

PCB DRAWINGS

Composite Drawings

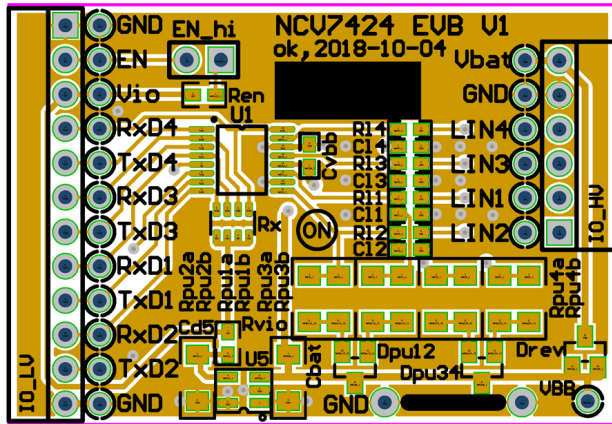


Figure 4. NCV7424 EVB PCB Top Drawing

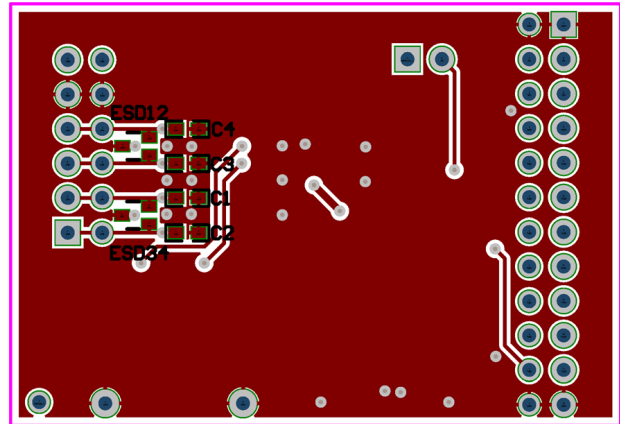


Figure 5. NCV7424 EVB PCB Bottom Drawing (Bottom View)

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