

# NCP45492IMNGEVB

## NCP45492 Evaluation Board User's Manual

### Introduction

This user's manual provides detailed information regarding the configuration and use of the NCP45492IMNGEVB Evaluation board. The evaluation board serves as a demonstration of NCP45492 general functionality for single chip mode featuring power monitoring of 4 channels. The evaluation board also provides a means of quick prototyping for specific applications.

### Features

- NCP45492
- Connectors for 4 High Current Supplies and Loads
- Configuration Options for Shunt Current and Gain Settings
- Appropriate Test Loops for Easy Evaluations

### QUICK START

#### Recommended Equipment

Before beginning, the following equipment is needed:

- 4 DC Power Supplies (2 capable of at least 7 V, 2 capable of at least 13 V to support current evaluation board setup)
- 4 DC Loads (up to at least 2 A)
- Function Generator
- Oscilloscope
- Digital Multi-meter
- SMA to BNC Cables Recommended for Connection to DIFF\_OUTN, DIFF\_OUTP, and MUX\_SEL

#### Board Setup

The assembled evaluation board targets Bus Voltages and Shunt Currents shown in Tables 1 and 2. VBUS1 ties to both channel 1 and channel 3 bus voltage inputs. VBUS2 ties to both channel 2 and channel 4 bus voltage inputs. Refer to the schematic and layout diagrams found in [Appendix A](#) and [Appendix B](#) respectively as needed.

**Table 1. BUS VOLTAGE SETUP**

| Channel   | Target Bus Voltage | Bus Divider |
|-----------|--------------------|-------------|
| 1 (VBUS1) | 12 V               | 1/60 V/V    |
| 2 (VBUS2) | 6 V                | 1/30 V/V    |
| 3 (VBUS1) | 12 V               | 1/60 V/V    |
| 4 (VBUS2) | 6 V                | 1/30 V/V    |



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**Table 2. SHUNT CURRENT SETUP**

| Channel | Shunt Current | Shunt Gain |
|---------|---------------|------------|
| Load 1  | 0.5 A         | 400 mV/A   |
| Load 2  | 5 A           | 40 mV/A    |
| Load 3  | 0.5 A         | 400 mV/A   |
| Load 4  | 5 A           | 40 mV/A    |

The specific resistor configuration populated on the board facilitate these gain settings. The nominal differential amplifier gain is 2 V/V. Therefore, the expected differential output for any channels voltage or current can be calculated as follows:

- For Bus Voltage:

$$\text{Diff Output} = \text{Bus Voltage} \cdot \frac{R4}{R4 + R3} \cdot 2 \quad (\text{eq. 1})$$

- For Load Current:

$$\text{Diff Output} = \text{Load Current} \cdot \text{Channel Shunt Gain} \cdot 2$$

$$\text{Diff Output} = I_{\text{Load}} \cdot \frac{R2 + R_{\text{sense}}}{R1} \cdot 2 \quad (\text{eq. 2})$$

These gain settings can be adjusted by changing the bus divider resistors, and the shunt current network resistors as desired.

#### Board Connections & Jumper Settings

The following board to bench equipment connections are required for demonstration of 4 channel power monitoring. Make all board connections with supplies and loads disabled. Take adequate precautions when working with high current and high voltage applications. Table 3 below defines all default board connections and their purpose.

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**Table 3. EVALUATION BOARD DEFAULT CONNECTIONS**

| Connection           | Connect To...                                | Purpose                                       |
|----------------------|----------------------------------------------|-----------------------------------------------|
| VBUS1 (banana)       | 12 V supply                                  | Provides channel 1 and channel 3 bus voltages |
| VBUS2 (banana)       | 6 V supply                                   | Provides channel 2 and channel 4 bus voltages |
| LOAD1 & GND (banana) | 0.5 A load current (24 $\Omega$ 1W resistor) | Provides channel 1 load current               |
| LOAD2 & GND (banana) | 2 A load current (3 $\Omega$ 12 W resistor)  | Provides channel 2 load current               |
| LOAD3 & GND (banana) | 0.5 A load (24 $\Omega$ 1W resistor)         | Provides channel 3                            |
| LOAD4 & GND (banana) | 2 A load current (3 $\Omega$ 12 W resistor)  | Provides channel 4 load current               |
| VCC & GND            | 3.3 V                                        | Provides part supply                          |
| MUX_SEL (sma)        | 3.3 V to 0 V signal generator                | Channel mux select input                      |
| EN (sma/header)      | 3.3 V to 0 V signal generator or tied to GND | Enable input. Active low                      |
| DIFF_OUT_P (sma)     | Oscilloscope                                 | Differential output (positive)                |
| DIFF_OUT_N (sma)     | Oscilloscope                                 | Differential output (negative)                |

**NOTES:**

1. All connections to the board have an accompanying ground connection. Use all ground connections with the evaluation board being the center of a star ground to avoid ground loops.
2. Connect to DIFF\_OUT\* signals with either 2 SMA to BNC cables to an oscilloscope (where the subtraction of the 2 signals give the differential voltage), or connect to the DIFF\_OUT\* test loops with a twisted pair or differential probe. Connecting in this manner will mitigate noise via EMI.
3. SH\_INx inputs need to be driven to a voltage between VCC and 26 V, even for unused channels. Jumpers 1, 2, 5, and 8 provide a means to connect unused channels to VCC. If a channel is not in use, the jumper should be switched to the VCC position and the SH\_Ox jumper should be removed to float the SH\_Ox pin.

Table 4 below defines all default jumper connections and their purpose.

**Table 4. DEFAULT JUMPER DEFINITION**

| Jumper | Default Setting | Function                                                                   |
|--------|-----------------|----------------------------------------------------------------------------|
| J1     | Shorted [1,2]   | Connects channel 1 bus voltage. [2,3] connection sets bus voltage to 3.3 V |
| J2     | Shorted [1,2]   | Connects channel 1 bus voltage. [2,3] connection sets bus voltage to 3.3 V |
| J5     | Shorted [1,2]   | Connects channel 1 bus voltage. [2,3] connection sets bus voltage to 3.3 V |
| J8     | Shorted [1,2]   | Connects channel 1 bus voltage. [2,3] connection sets bus voltage to 3.3 V |
| J3     | Shorted         | SH_O2                                                                      |
| J4     | Shorted         | SH_O1                                                                      |
| J6     | Shorted         | SH_O3                                                                      |
| J7     | Shorted         | SH_O4                                                                      |
| J20    | Shorted [1,2]   | SKIP input connection                                                      |
| J21    | Open            | MODE_SEL input connection                                                  |
| J10    | Open            | SMD jumper that can be shorted to tie EN to GND                            |

**NCP45492IMNGEVB**

## Testing Procedure

The NCP45492IMNGEVB comes fully assembled and tested. Follow the steps below to verify board operation. Refer to the schematic and layout diagrams found in [Appendix A](#) and [Appendix B](#) respectively as needed.

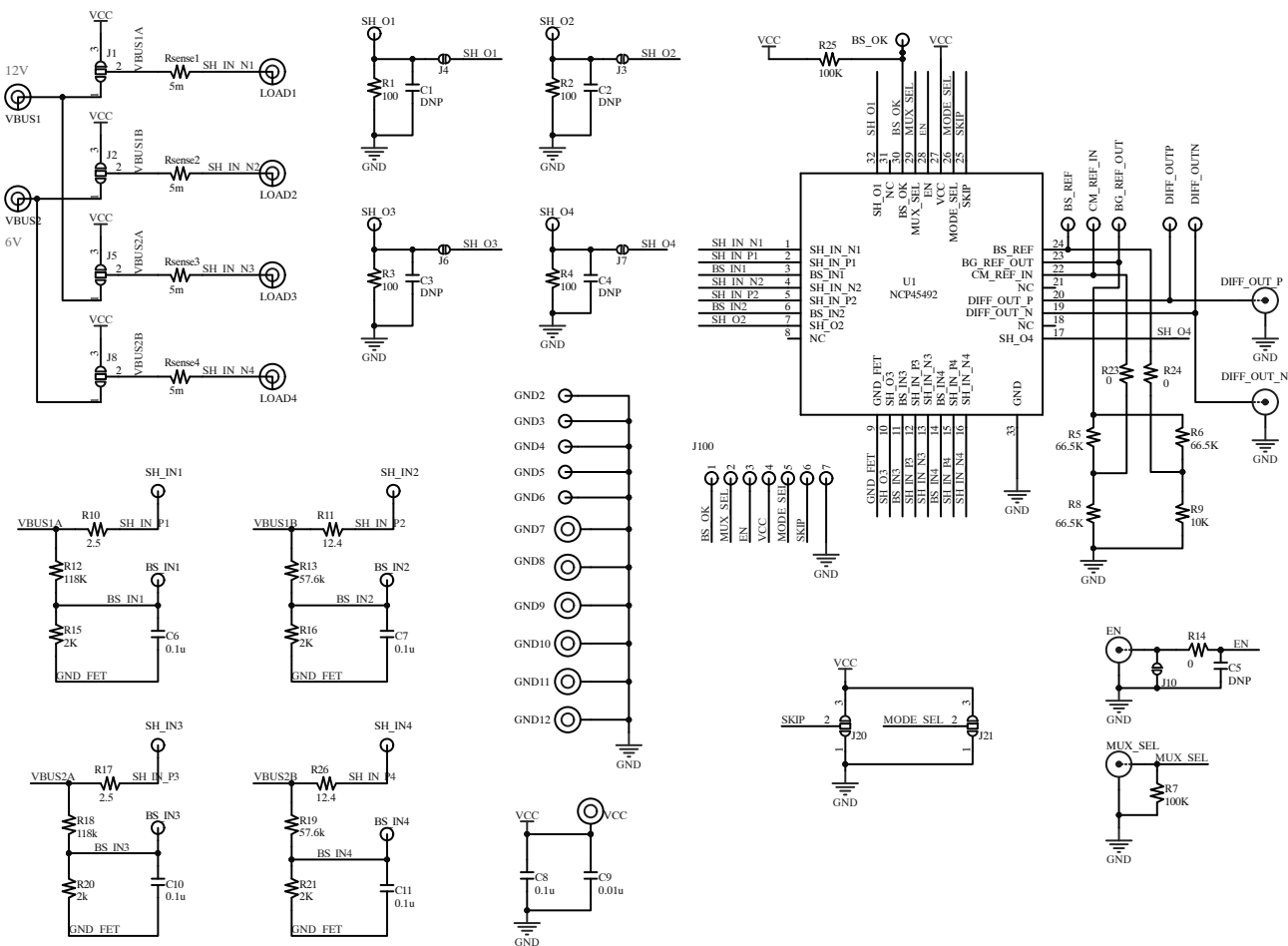
1. Apply power to VBUS inputs (6 V and 12 V supply).
2. Apply load currents for all channels.
3. Apply 3.3 V VCC power.
4. Apply MUX\_SEL signal. (Square wave 50% duty cycle, 100 kHz or faster, VCC to 0 V)
  - a. 8 cycles will read out voltage and current data for all 4 channels.
  - b. Continuous cycles on MUX\_SEL will read out bus voltage and current data continuously, repeating channels 1–4.

5. Observe the following:
  - a. 1.3 V on BG\_REF\_OUT
  - b. 650 mV on CM\_REF\_IN
  - c. 170 mV on BS\_REF
  - d. Bus voltages and currents represented on DIFF\_OUTP and DIFF\_OUTN with oscilloscope.

## PCB Layout

Care must be taken in PCB layout regarding a few specific nodes for proper operation of the NCP45492. Connections to the external sense resistor for each channel must be treated as a 4 wire Kelvin connection. The SH\_IN\_Nx and the SH\_IN\_Px (connected through R1) must connect directly to the sense resistor leads for each respective channel. These should also be large traces to avoid error in the shunt current measurement. See [Appendix C](#) for the example layout of the evaluation board.

## APPENDIX A – EVALUATION BOARD SCHEMATIC



### Figure 1. NCP45492 Evaluation Board Schematic

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## APPENDIX B – BILL OF MATERIALS

**Table 5. BILL OF MATERIALS**

| Designator                                                                                                                                                                           | Footprint      | Value           | Quantity | Digikey P/N          |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|-----------------|----------|----------------------|
| BG_REF_OUT, BS_IN1, BS_IN2, BS_IN3, BS_IN4, BS_OK, BS_REF, CM_REF_IN, DIFF_OUTN, DIFF_OUTP, GND2, GND3, GND4, GND5, GND6, SH_IN1, SH_IN2, SH_IN3, SH_IN4, SH_O1, SH_O2, SH_O3, SH_O4 | Test_Point     | Test loop       | 23       | 36-5009-ND           |
| C1, C2, C3, C4, C5                                                                                                                                                                   | SMD_0805       | No placement    | 5        | N/A                  |
| C6, C7, C8, C10, C11                                                                                                                                                                 | SMD_0805       | 0.1 $\mu$ F     | 5        | 490-8049-1-ND        |
| C9                                                                                                                                                                                   | SMD_0805       | 0.01 $\mu$ F    | 1        | 1276-1015-2-ND       |
| DIFF_OUT_N, DIFF_OUT_P, EN, MUX_SEL                                                                                                                                                  | SMB_V-RJ45     | SMB/SMA Strai   | 4        | WM5543-ND            |
| GND7, GND8, GND9, GND10, GND11, GND12, LOAD1, LOAD2, LOAD3, LOAD4, VBUS1, VBUS2, VCC                                                                                                 | Bannana_Connec | Banana Con      | 13       | J587-ND              |
| J1, J2, J5, J8, J20, J21                                                                                                                                                             | 10th" header   | 3 pins          | 6        | 732-5316-ND          |
| J3, J4, J6, J7, J10, J100                                                                                                                                                            | 10th" header   | 10" header      | 6        | 732-5315-ND          |
| R12, R18                                                                                                                                                                             | SMD_1206       | 118 k $\Omega$  | 2        | P118KFCT-ND          |
| R15, R20, R16, R21                                                                                                                                                                   | SMD_1206       | 2 k $\Omega$    | 4        | P2.0KBCCT-ND         |
| Rsense1, Rsense2, Rsense3, Rsense4                                                                                                                                                   | SMD_1206       | 5 m $\Omega$    | 4        | RHM.005ALCT-ND       |
| R1, R2, R3, R4                                                                                                                                                                       | SMD_1206       | 100 $\Omega$    | 4        | P100BCCT-ND          |
| R5, R6, R8                                                                                                                                                                           | SMD_1206       | 66.5 k $\Omega$ | 3        | 311-66.5KFRCT-ND     |
| R9                                                                                                                                                                                   | SMD_1206       | 10 k $\Omega$   | 1        | RNCP1206FTD10K0CT-ND |
| R14, R23, R24                                                                                                                                                                        | SMD_1206       | 0 $\Omega$      | 3        | HCJ1206ZT0R00CT-ND   |
| R7, R25                                                                                                                                                                              | SMD_1206       | 100 k $\Omega$  | 2        | RHM100KICT-ND        |
| R13, R19                                                                                                                                                                             | SMD_1206       | 57.6 k $\Omega$ | 2        | P57.6KAACT-ND        |
| R11, R26                                                                                                                                                                             | SMD_1206       | 12.4 $\Omega$   | 2        | 311-12/4FRCT-ND      |
| R10, R17                                                                                                                                                                             | SMD_1206       | 2.5 $\Omega$    | 2        | 541-2.49UCT-ND       |
| U1                                                                                                                                                                                   | NCP45492       | N/A             | 1        | NCP45492             |

# NCP45492IMNGEVB

## APPENDIX C – NCP45492 EVALUATION BOARD LAYOUT

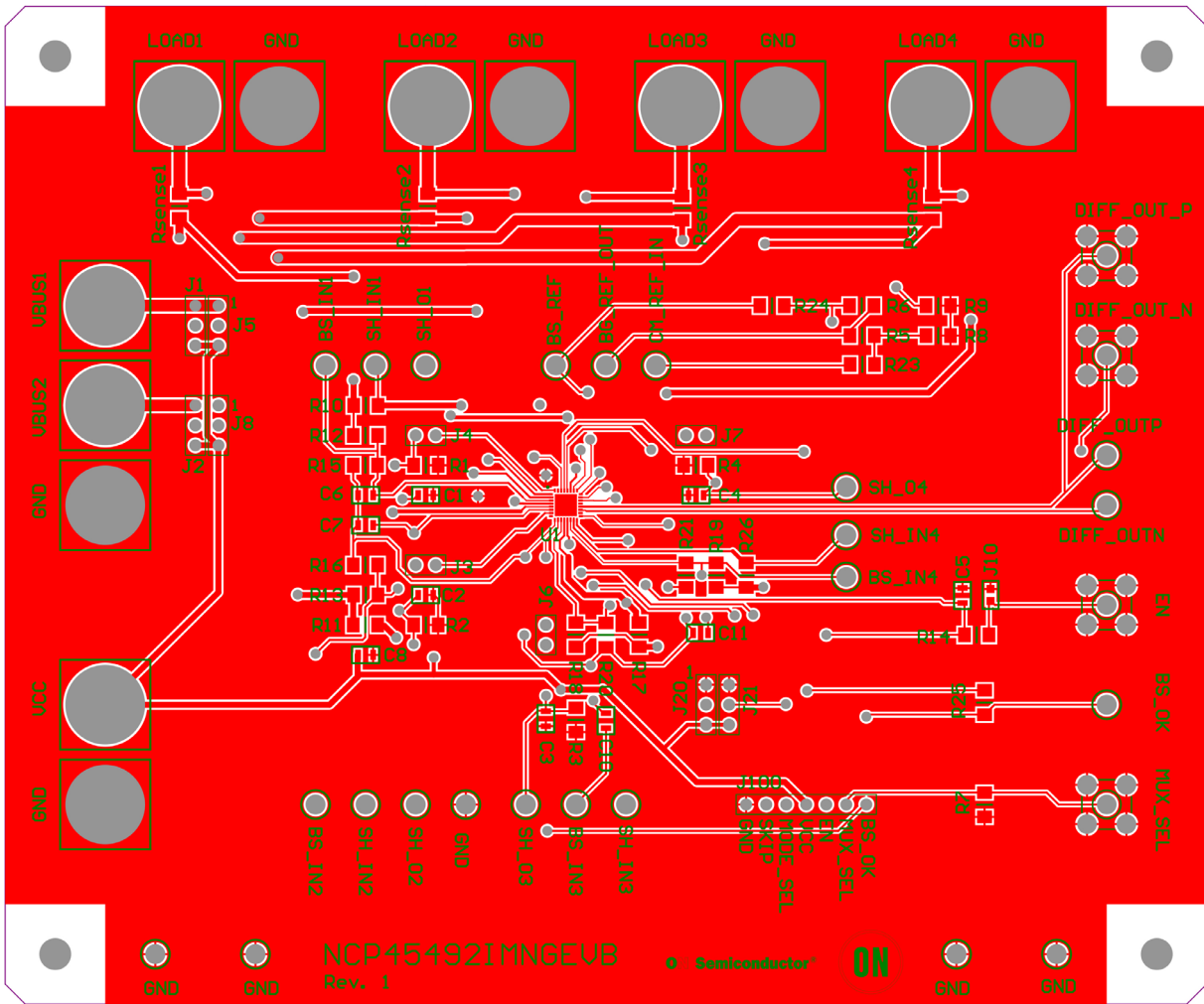


Figure 2. PCB Front (Top Metallization)

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