onsemi



SOT-223 (TO-261) CASE 318E-04 ISSUE R

SEE DETAIL A

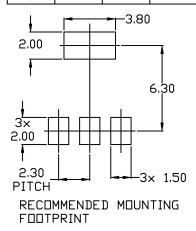
FRONT VIEW

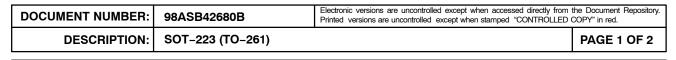
DATE 02 OCT 2018



- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
- 4. DATUMS A AND B ARE DETERMINED AT DATUM H.
- AI IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- 6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS & AND &1.

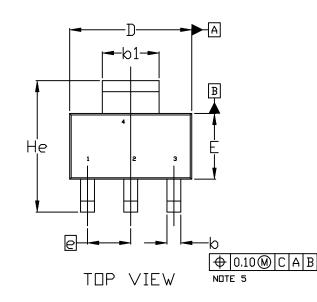
	MILLIMETERS			
DIM	MIN.	NDM.	MAX.	
A	1.50	1.63	1.75	
A1	0.02	0.06	0.10	
b	0.60	0.75	0.89	
b1	2.90	3.06	3.20	
с	0.24	0.29	0.35	
D	6.30	6.50	6.70	
E	3.30	3.50	3.70	
e	2.30 BSC			
L	0.20			
L1	1.50	1.75	2.00	
He	6.70	7.00	7.30	
θ	0*		10*	

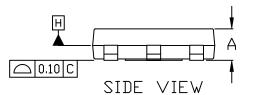


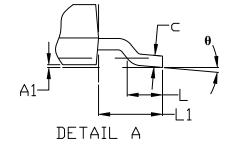


onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SCALE 1:1







© Semiconductor Components Industries, LLC, 2018

SOT-223 (TO-261) CASE 318E-04 **ISSUE R**

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: Pin 1. INPUT 2. Ground 3. Logic 4. Ground	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	Style 12: Pin 1. Input 2. Output 3. NC 4. Output	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

GENERIC **MARKING DIAGRAM***



- = Assembly Location А
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code .
- = Pb-Free Package
- (Note: Microdot may be in either location) *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.		
DESCRIPTION:	SOT-223 (TO-261)		PAGE 2 OF 2	

onsemi and ONSEMi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.