NCS32100 PCB Reference Design DRC Guidelines

TND6427/D

Stack−up Requirements *(4−Layer Board)*

As shown in Figure 1, layers M1 and M2 are used for the sensor coils. These two layers should be close together since the loops jump from M1 to M2 as the loop around the stator board. The core should be a minimum of 1 mm thick or greater. This provides isolation between the sensor fields and the NCS32100 electronics. M1, M2, M3, and M4 must not have any continuous fill metal planes. Planes of metal in close proximity to the excitation coils on layer M1 and M2 will load the excitation.

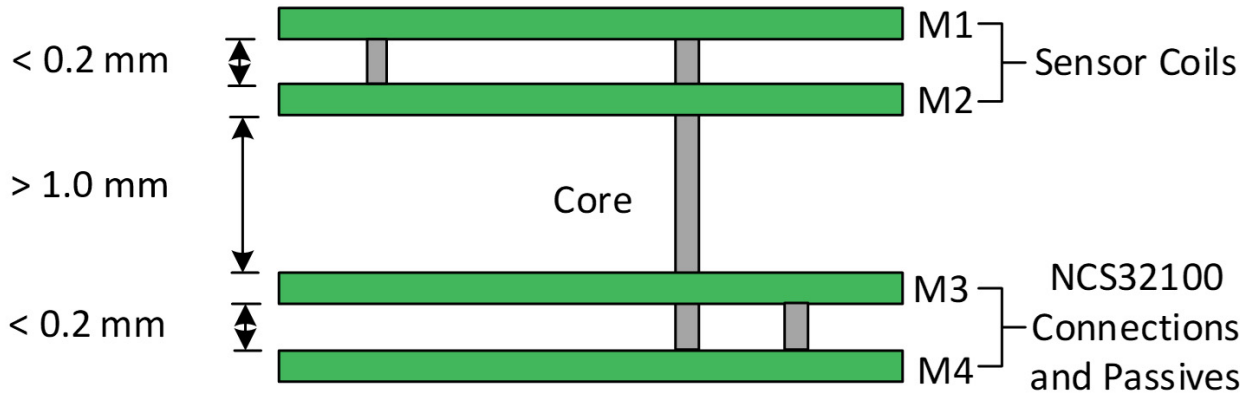

Figure 1. 4 − Layer Stackup

Blind vias are used between M1 and M2 to connect sensor coil loops. Blind vias are used between M3 and M4 for routing connections to the NCS32100 device. All layer vias are used to connect the sensor coils through to the NCS32100 (do not use all layer vias otherwise).

Table 1. BOARD MATERIAL SPECIFICATIONS

Layers	4*
Solder Mask	Top and bottom
Material	FR−4
Copper Weight	½ oz − 2 oz
Silk Screen	Only required on bottom

Table 2. DRC RULES

Min Trace	0.1 mm
Min Space	0.1 mm
SME Pad	0.1 mm
Via annular Ring	0.2 mm
Smallest Drill Hole Size	0.1 mm
Slots	None
Via Fill	Not required

Passive Component Placement

For the NCS32100 power pins, all decoupling capacitors should be placed as close as possible to the NCS32100. The idea is to minimize the amount of trace length needed to connect from the capacitors to the NCS32100 pins, as is common in most PCB design.

Sensor Coil Connections

When connecting the Coarse and Fine coils to the REC pins on the NCS32100, care should be taken to keep these traces at approximately the same length, while also keeping them as short as possible. When possible, route the traces to be perpendicular (or orthogonal) to the excitation coil.

Ground / Power / VBAT Routing

When routing ground/power / VBAT, ensure that these traces are routed as close as possible to one another from the connector/source, until they must diverge. The trace widths should be the same, and should not exceed 0.2 mm.

Ground Loops

The ideal layout will not have any ground loops present at the NCS32100, as ground loops can cause the 4.4 MHz excitation frequency to be unevenly coupled to the coils on the stator. This coupling shows up in the form of DC offset after the demodulation of the coil signals. Some DC offset is unavoidable, but too much DC offset can cause problems with calibration and accuracy.

Ensuring that all ground connections originate from the NCS32100 thermal pad (except for the one ground connection coming the connector/source to the thermal pad), and no redundant ground connections are made, DC ground loops will not be present.

AC ground loops cannot be entirely eliminated, since capacitors look like a low resistance path for the 4.4 MHz excitation frequency. As mentioned earlier, ensure that all capacitors are placed as closely as possible to the NCS32100 to reduce possible AC loops.

Data Lines

Do not route data line across the NCS32100. For example, do not place a via at DATA0 – DATA3, and route underneath the thermal pad of the NCS32100. This can cause unwanted coupling. Instead, route these data lines away from the NCS32100.

2−Layer Board

As shown in Figure 2 it is also possible to design a two−layer stator board (M1 and M2), where only the coils and a connector are needed. This is a useful design if there is a separate board for the NCS32100 (and supporting components) that connects like a mezzanine, and can remove the need for using blind vias. Use caution to be sure that there are not continuous metal planes on the separate board that might interfere with the excitation coil coupling.

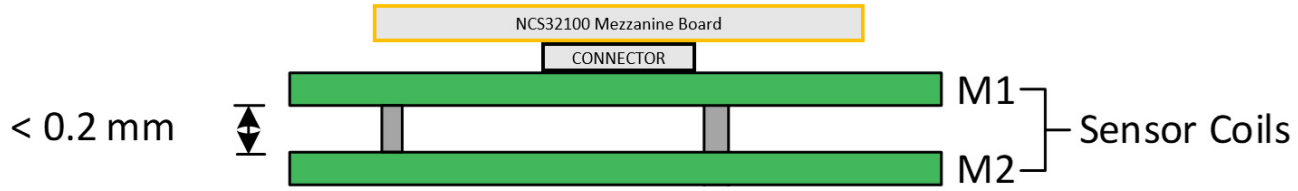

Figure 2.

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