Self-Service PLECS Model Generator (SSPMG)

User Guide

Outline of User Guide

1	Introduction to Self-Service PLECS Model Generator: What is it and What are the benefits
2	Step by Step Tool Flow
3	Deploying PLECS Models in Elite Power Simulator and PLECS Stand Alone

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PLECS Basics

- PLECS is a system level simulator that facilitates the modeling and simulation of complete systems with optimized device models for maximum speed and accuracy. PLECS is not a SPICE-based circuit simulator, where the focus is on low-level behavior of circuit components .
- Power transistors are treated as simple switches that can be easily configured to demonstrate losses associated with conduction and switching transitions.
- The PLECS models, referred to as “thermal models”, are composed of lookup tables for conduction and switching losses, along with a thermal chain in the form of a Cauer or Foster equivalent network.
- During simulation, PLECS interpolates and/or extrapolates using the loss tables to get the bias point conduction and switching losses for the circuit operation. Access the onsemi Elite Power Simulator powered by plecs

www.onsemi.com/elite-power-simulator

onsemi's State-of-the-Art PLECS Models:

- Typical industry PLECS models are composed of measurement-based loss tables that are consistent with datasheets provided by the manufacturer.

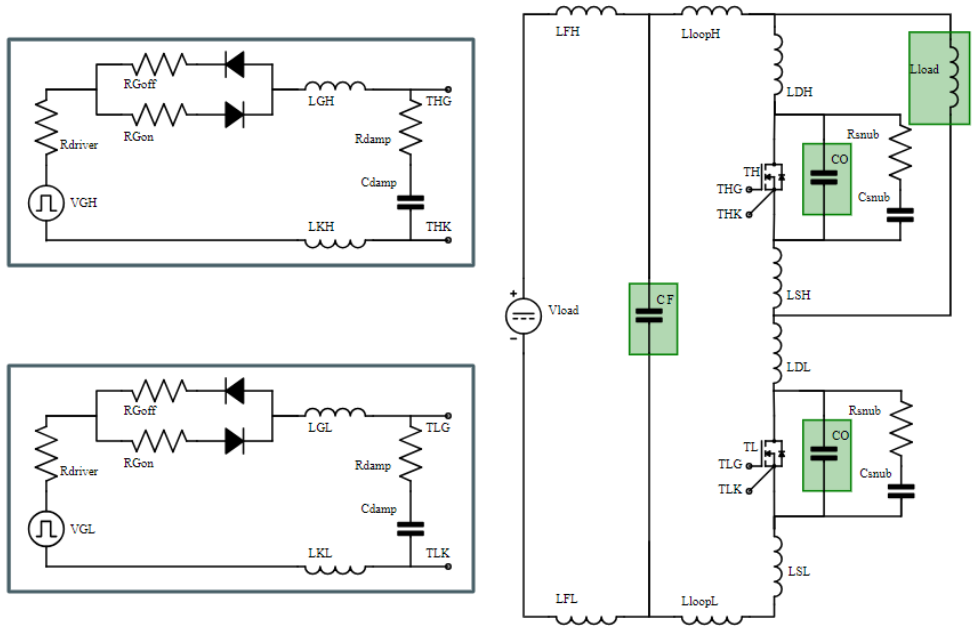
  There are four major problems with this approach:

  1. The switching energy loss data is dependent on the parasitics of the measurements set ups and circuits.
  2. The conduction and switching energy loss data is limited and thus is often not dense enough to ensure accurate interpolation and minimal extrapolation by PLECS.
  3. The loss data is based on nominal semiconductor process conditions only.
  4. The switching energy loss data comes from datasheet double pulse generated loss data. This means the PLECS models are only valid for hard switching topology simulation. The models are highly inaccurate if used in soft switching topology simulation.

- onsemi's Self-Service PLECS Model Generator (SSPMG) provides solutions to all four problems.
- Ultimate power is delivered to the user to build PLECS models tailored for the user's application. Unleash the power here: www.onsemi.com/self-plecs-generator

Measurement Parasitics Influence on Switching Performance

Switching Schematic with Parastics



Example Datasheet

Parameter	Switching Loss
Eon [uJ]	490
Eoff [uJ]	221
Etotal [uJ]	711

≠

Customer Application

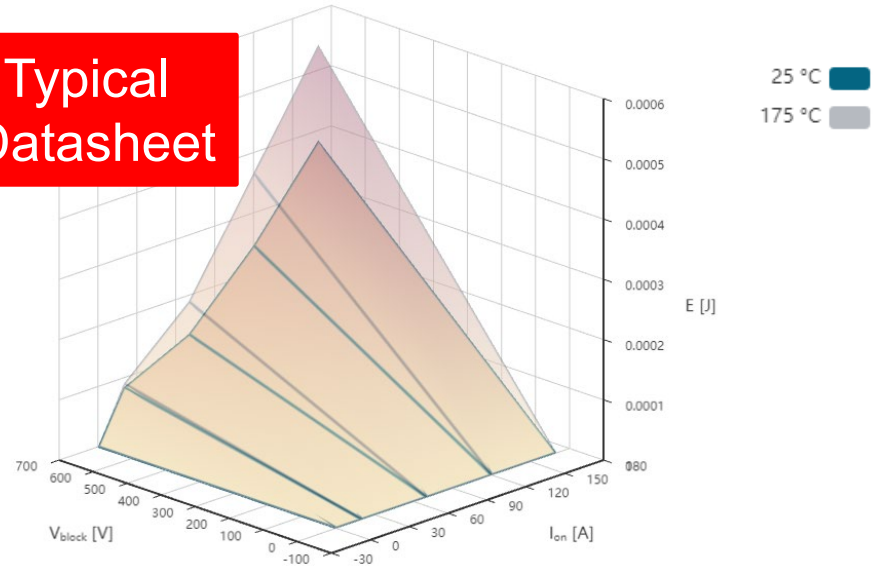
Parameter	Switching Loss
Eon [uJ]	415
Eoff [uJ]	231
Etotal [uJ]	646

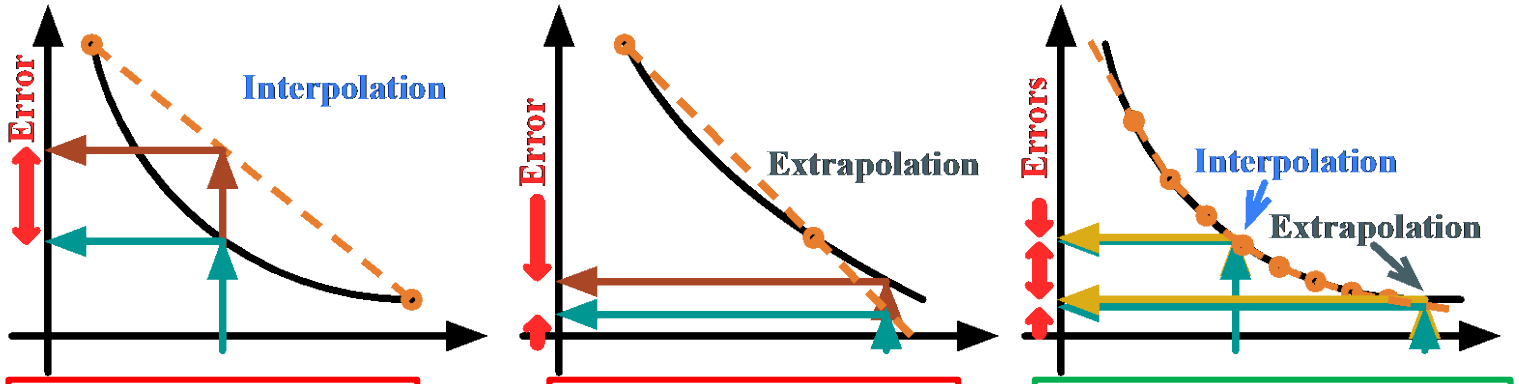
- Crucial to understand that the lab test circuit's passives, parasitics, gate driver performance, etc. all affect losses.
- Where does this leave the user for a PLECS model? The user application will surely have a different environment than any of the component supplier's lab and board setups.

Loss Table Density and Limits Influence Results

- Datasheet data is often not dense enough to ensure accurate interpolation by PLECS in nonlinear environments.
- Datasheet data limits often do not bound the entire operating range causing highly inaccurate extrapolation by PLECS.

Typical Datasheet



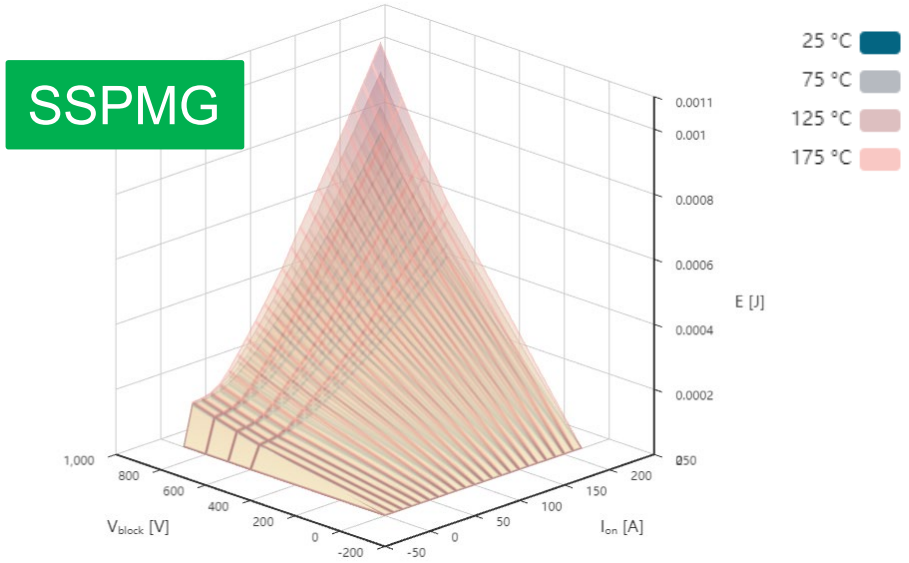


Interpolation with small data set

Extrapolation with small data set

Interpolation & Extrapolation with large data set

SSPMG



Corner PLECS Models

- Conventional PLECS models based on measurements are only valid for the typical or nominal process case in manufacturing. onsemi has developed accurate corner PLECS models based on real manufacturing distribution.
- Physics dictates that worst case conduction and switching losses do not happen simultaneously for example.
- Depending on the application, the influence of conduction and switching energy losses on the overall system performance will vary. The onsemi corner PLECS models provide the user the flexibility to investigate the entire correlated space.
- Corner models currently available for EliteSiC and T10M 40V products. More T10 and FS7 IGBT corner models are coming soon.
- Accurate corner and statistical modeling covered in detail in
  - SiC MOSFET Corner and Statistical SPICE Model Generation – Proceeding of International Symposium on Power Semiconductor Devices and ICs (ISPSD), pp. 154-147, September 2020

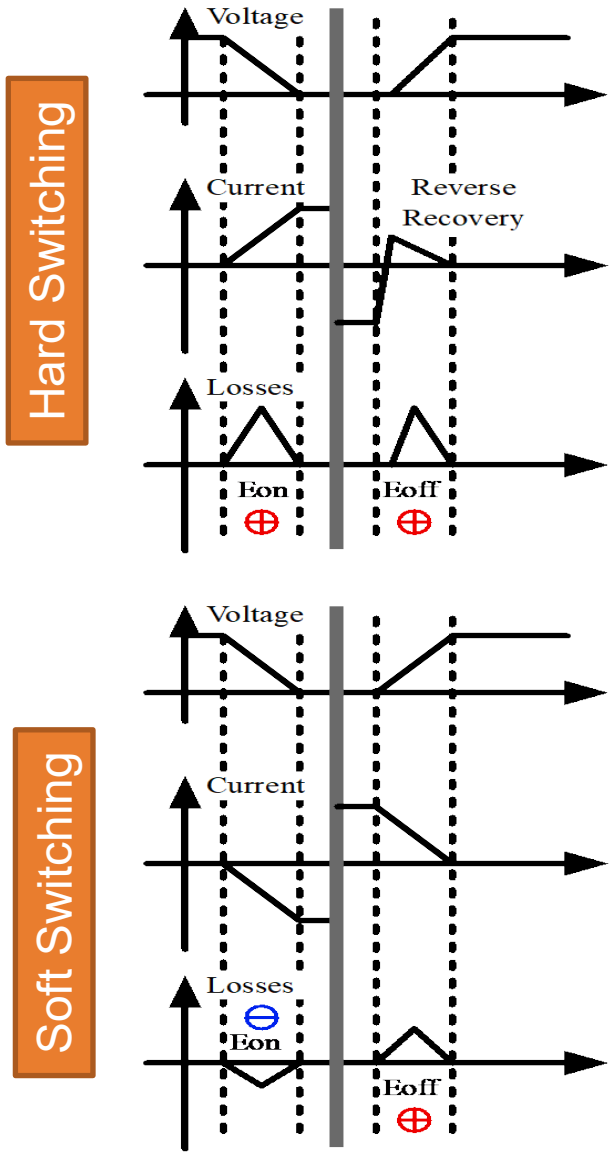
Process Condition	R_{DSon}, V_{th}, BV	Capacitance, Device RG	Conduction Loss	Switching Energy Loss
Nominal	Nominal	Nominal	Nominal	Nominal
Best Case Conduction Loss, Worst Case Switching Loss	Low	High	Low	High
Worst Case Conduction Loss, Best Case Switching Loss	High	Low	High	Low

Full Switching Energy Losses

Full Switching Simulation*

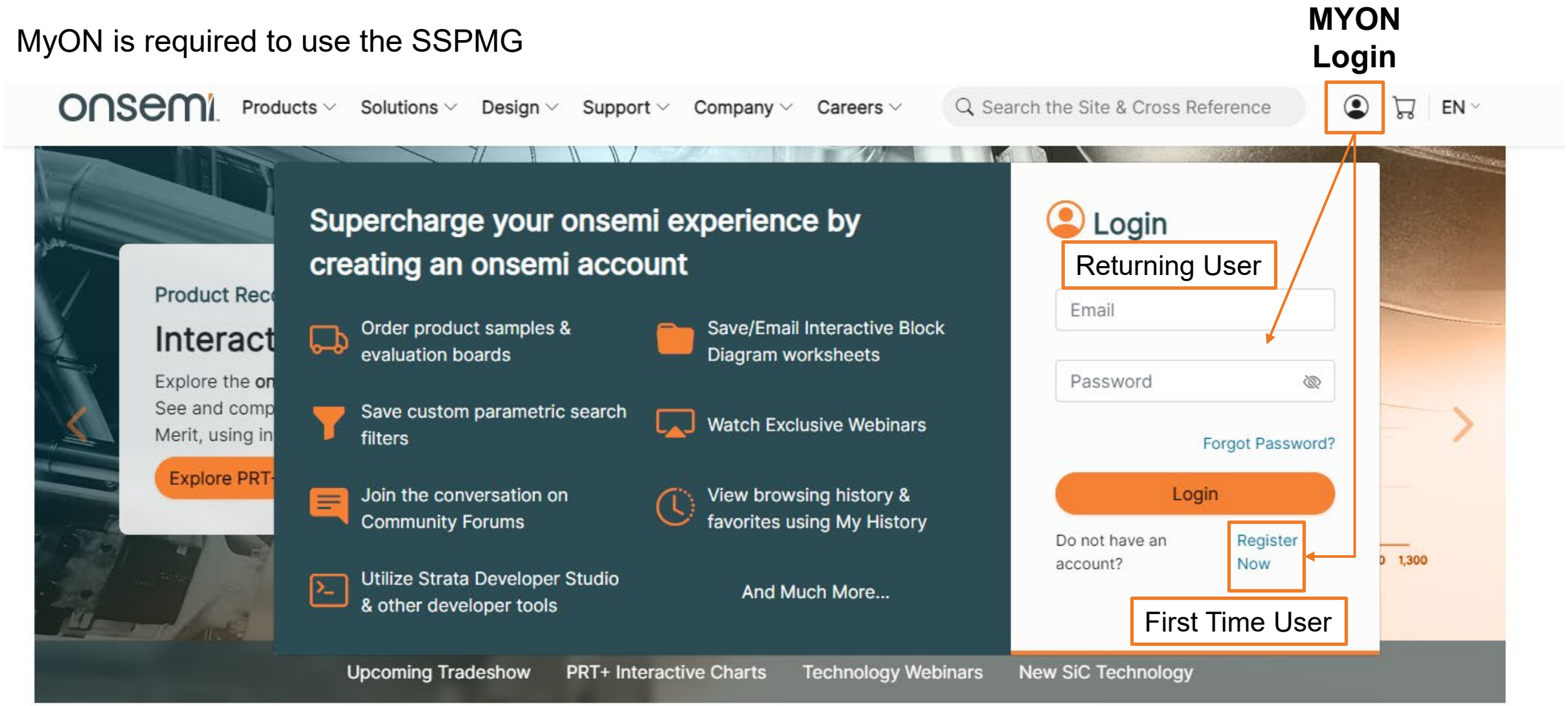
onsemi provides **industry first** Full Switching PLECS models **valid for hard, soft, and partial soft switching** including Synchronous Rectifier Operations. Example Full Switching topologies include DC-DC LLC and CLLC Resonant, Dual Active Bridge, and Phase Shifted Full Bridge.

*The Double Pulse Test is **NOT** representative of Soft Switching. Using double pulse switching energy losses in the simulation of a Soft Switching Topology is highly inaccurate.



Access SSPMG with MYON Account

MyON is required to use the SSPMG



Outline of User Guide

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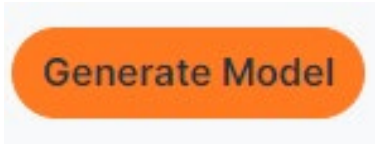
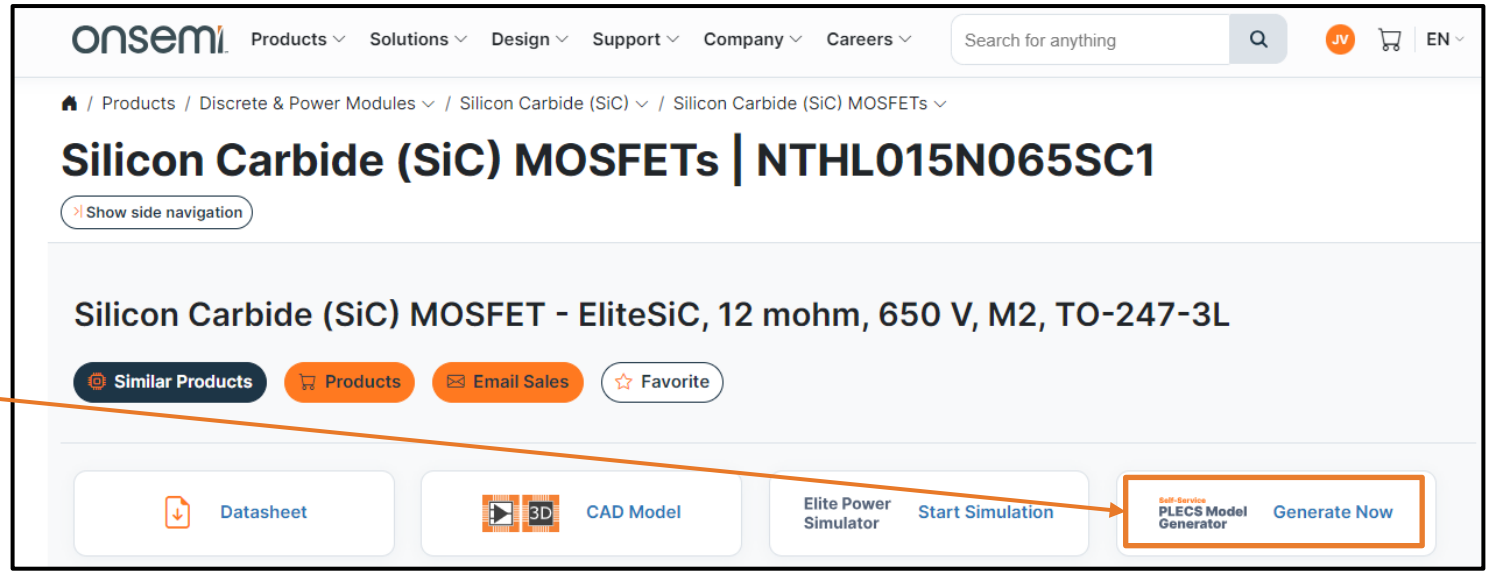
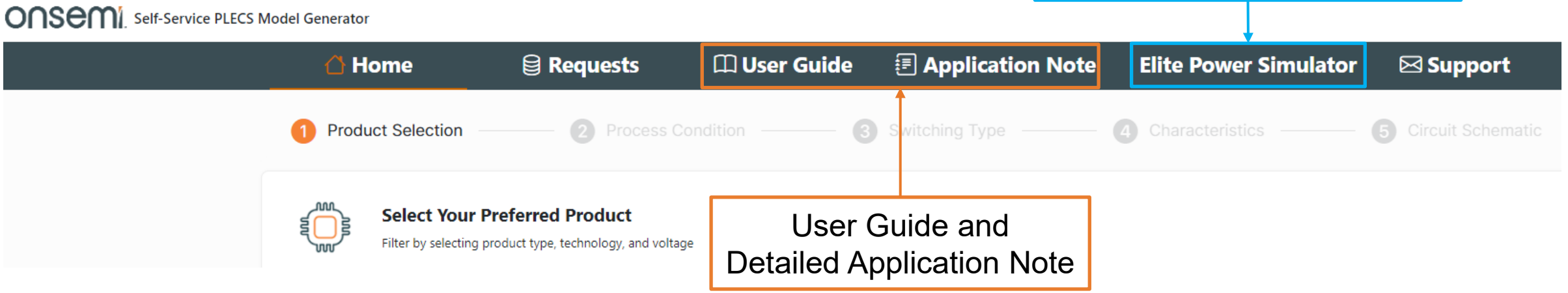
Getting Started

Go to landing page www.onsemi.com/self-plecs-generator and select Generate Model OR find SSPMG link on product pages.



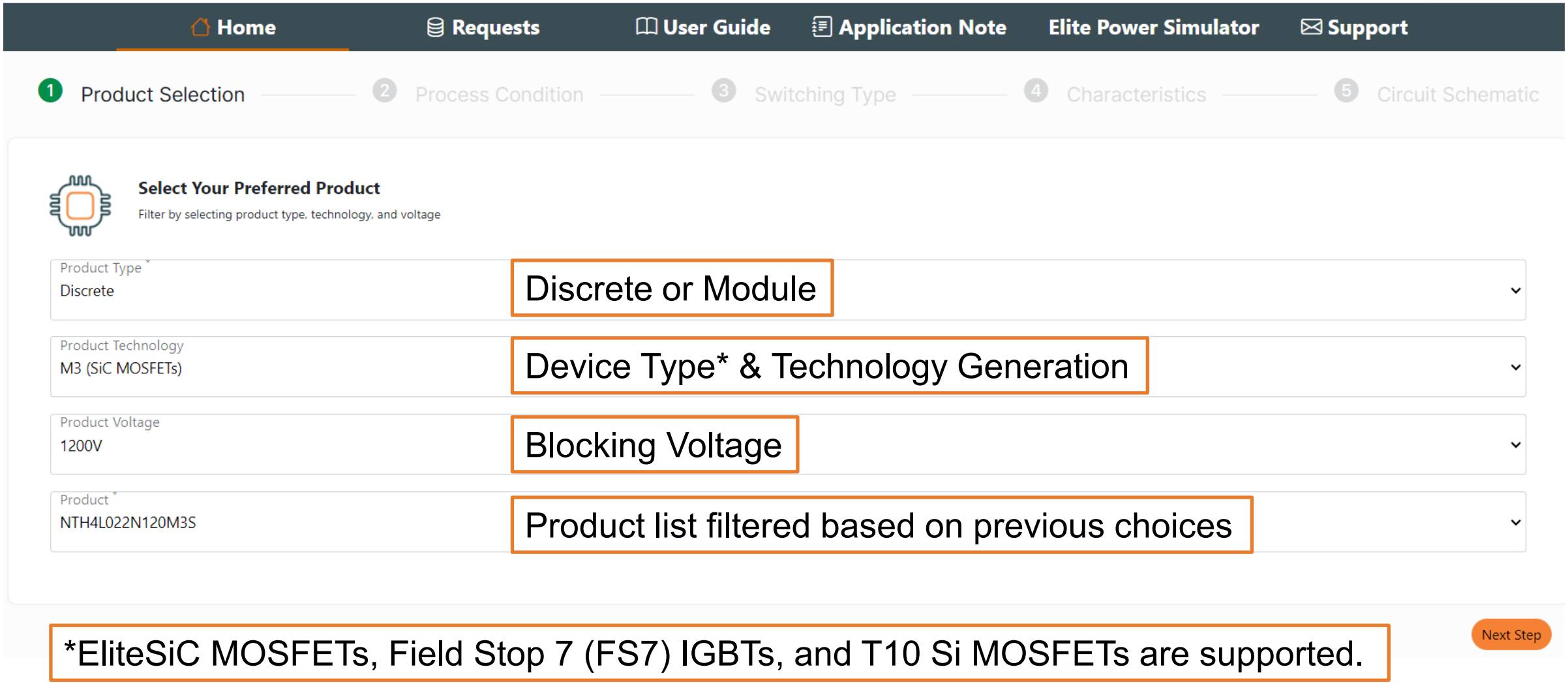


Link to Elite Power Simulator



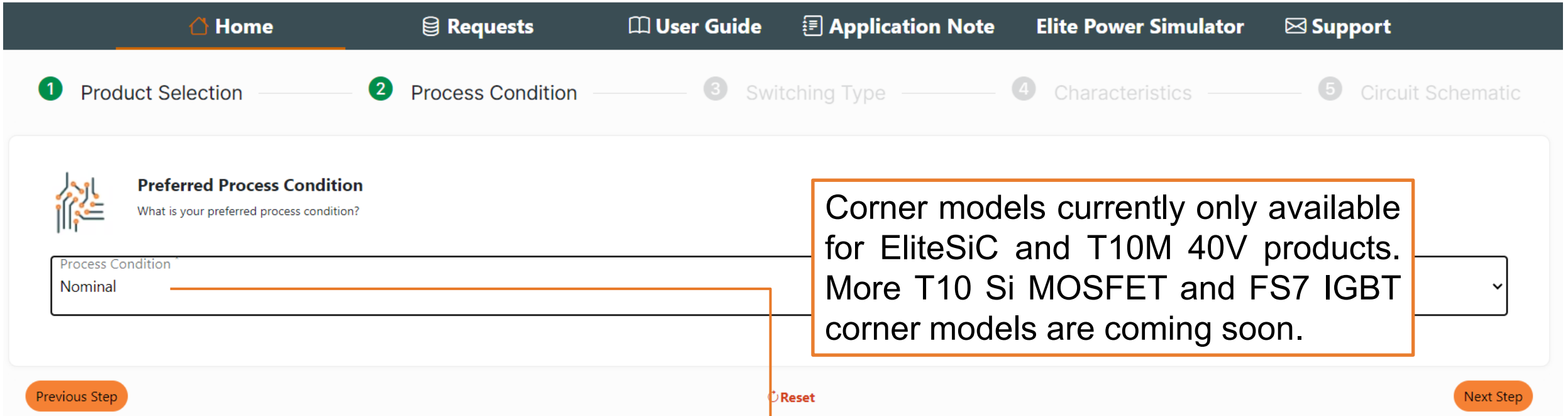
User Guide and Detailed Application Note

Step 1: Select Product



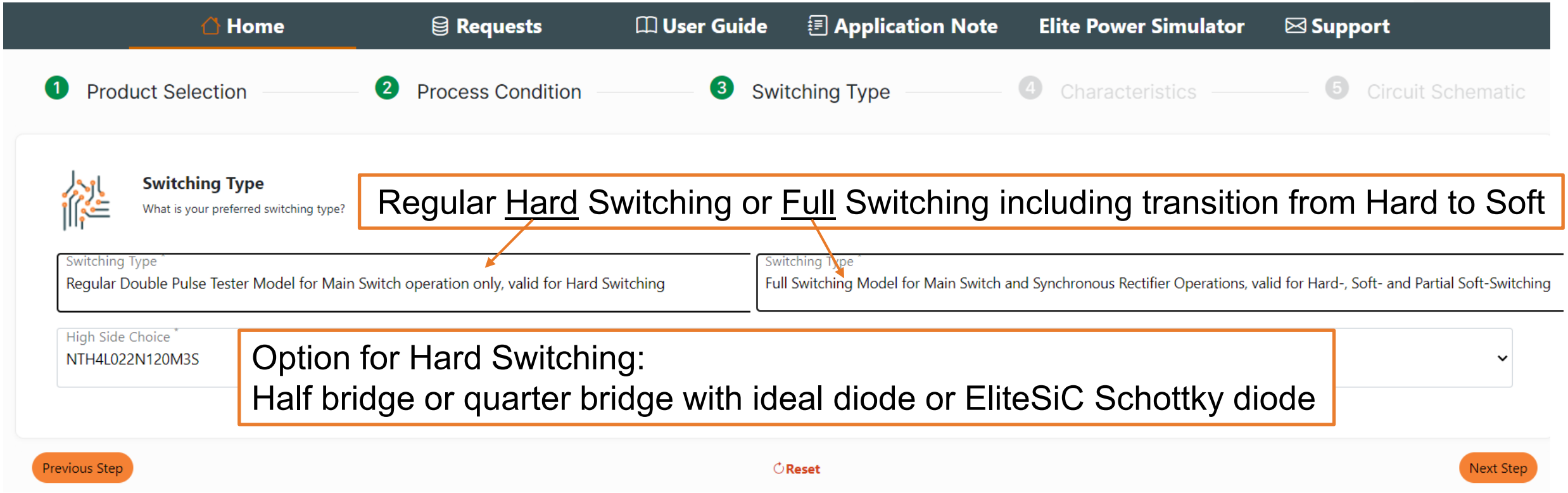
*EliteSiC MOSFETs, Field Stop 7 (FS7) IGBTs, and T10 Si MOSFETs are supported.

Step 2: Set Process Condition



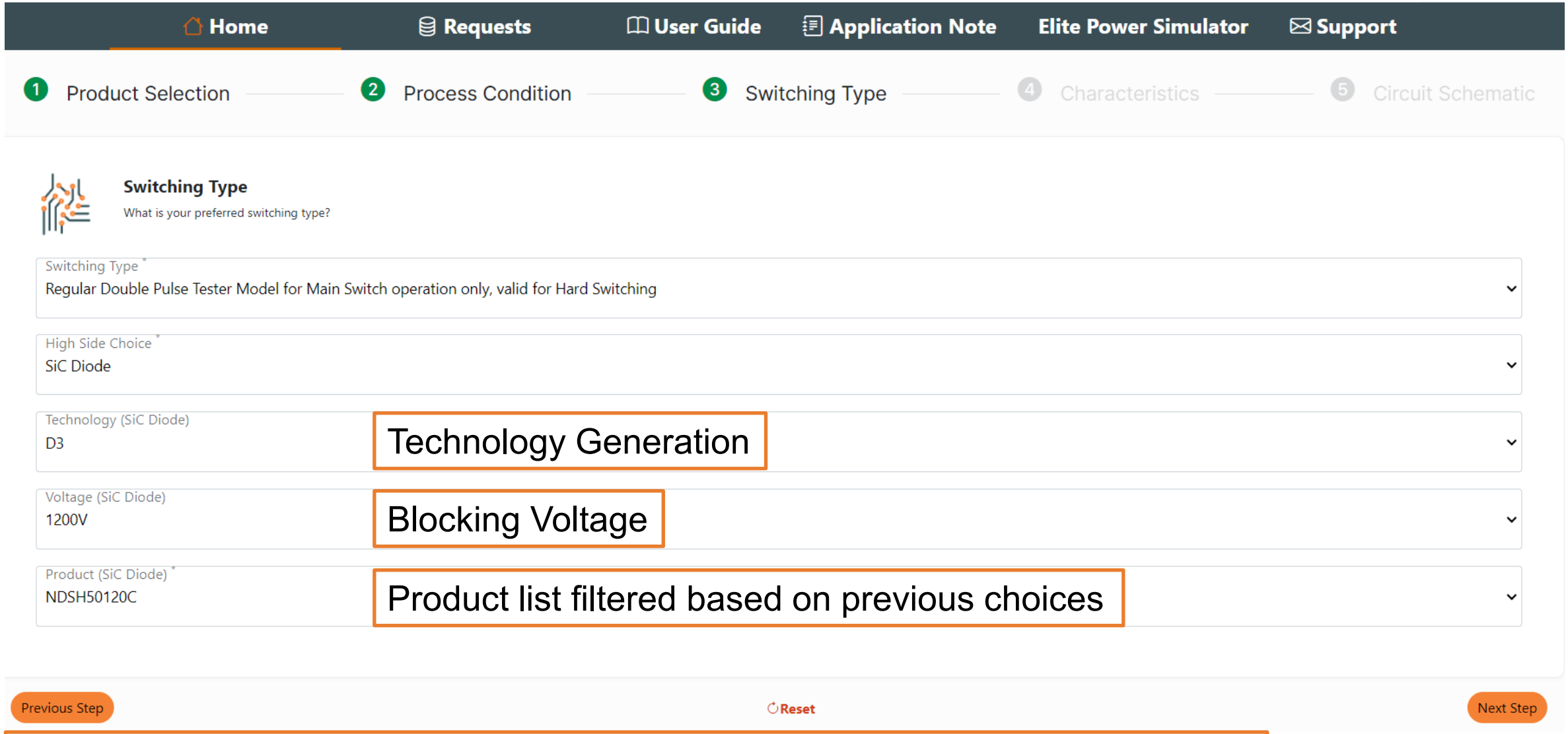
Process Condition	R_{DSon}, V_{th}, BV	Capacitance, Device RG	Conduction Loss	Switching Energy Loss
Nominal	Nominal	Nominal	Nominal	Nominal
Best Case Conduction Loss, Worst Case Switching Loss	Low	High	Low	High
Worst Case Conduction Loss, Best Case Switching Loss	High	Low	High	Low

Step 3: Set Switching Type



- Choose the switching type based on the intended application or topology.
- If hard switching chosen, user has choice for high side device to be in half bridge configuration or quarter bridge with ideal diode or EliteSiC Schottky diode on the high side.
- Full Switching is valid for hard, soft, and partial soft switching. Example Full Switching topologies include DC-DC LLC and CLLC Resonant, Dual Active Bridge, and Phase Shifted Full Bridge.
- Subsequent step 4 “Characteristics” change slightly based on the Switching Type.

Step 3: Quarter Bridge with EliteSiC Schottky Diode



- User should make sure EliteSiC Schottky diode current rating is suitable with the low side switch.

Step 4: Set Characteristics (Hard Switching)

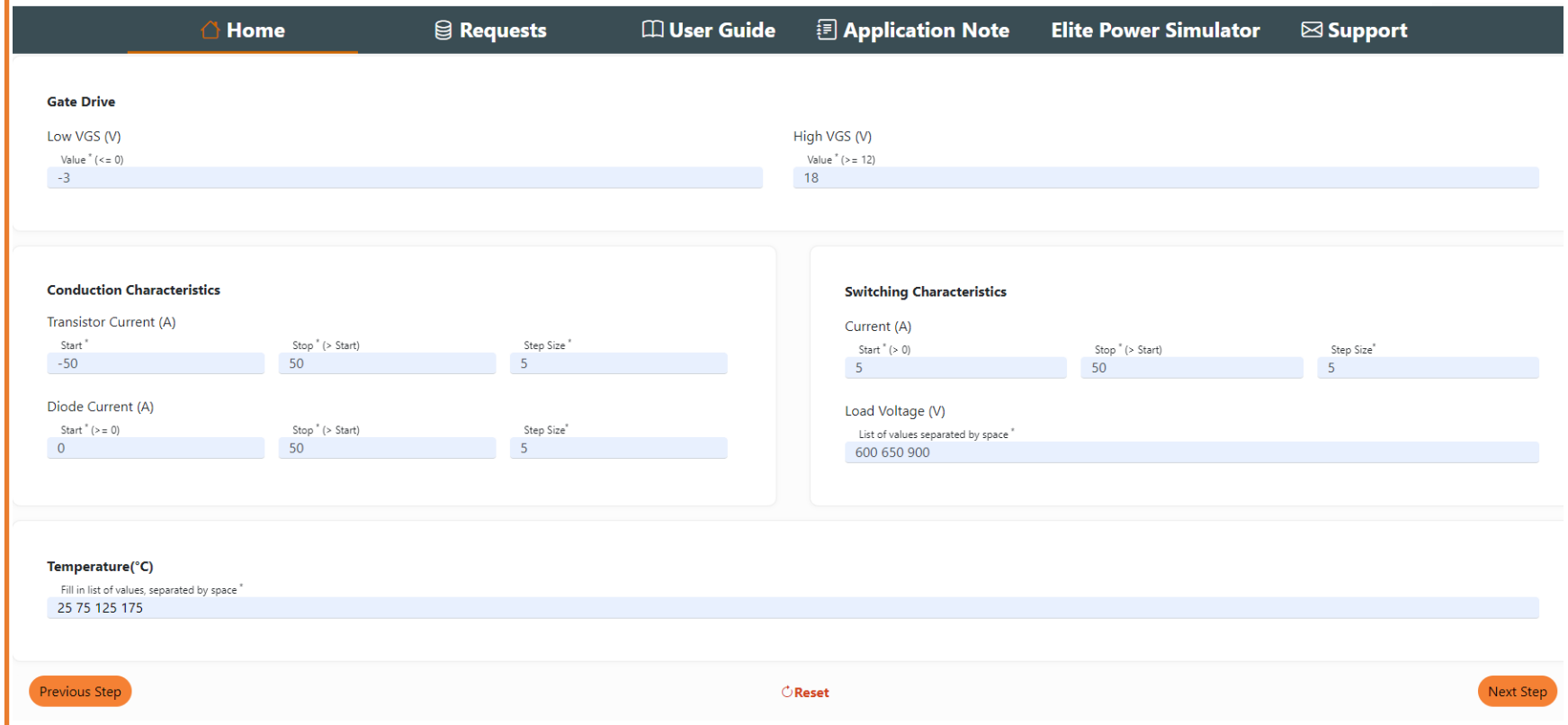
- Drain current can be in 1st and/or 3rd quadrant, so positive and/or negative.
- Diode Current is for diode forward conduction mode at the low VGS condition. Values are given in absolute scale.
- Default Gate Drive conditions are the recommended values. User can change Low and High VGS within a specified range that ensures proper device operation.
- If

(Stop-Start)/(Step Size) != Integer then last point=Stop. Example:

Start=1 Stop=9 Step Size=3

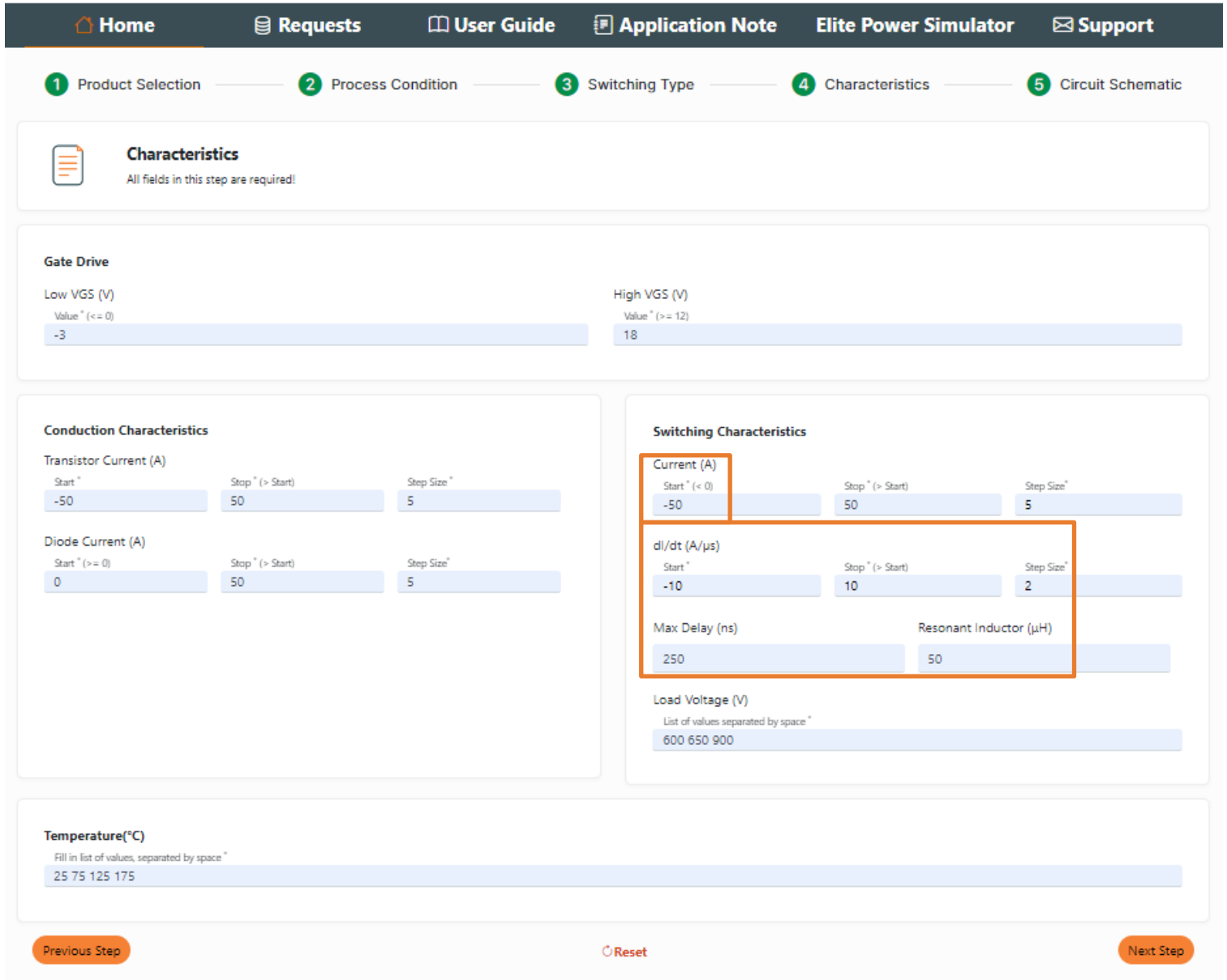
Simulated points are: 1 4 7 9

Descriptive fields guide user.



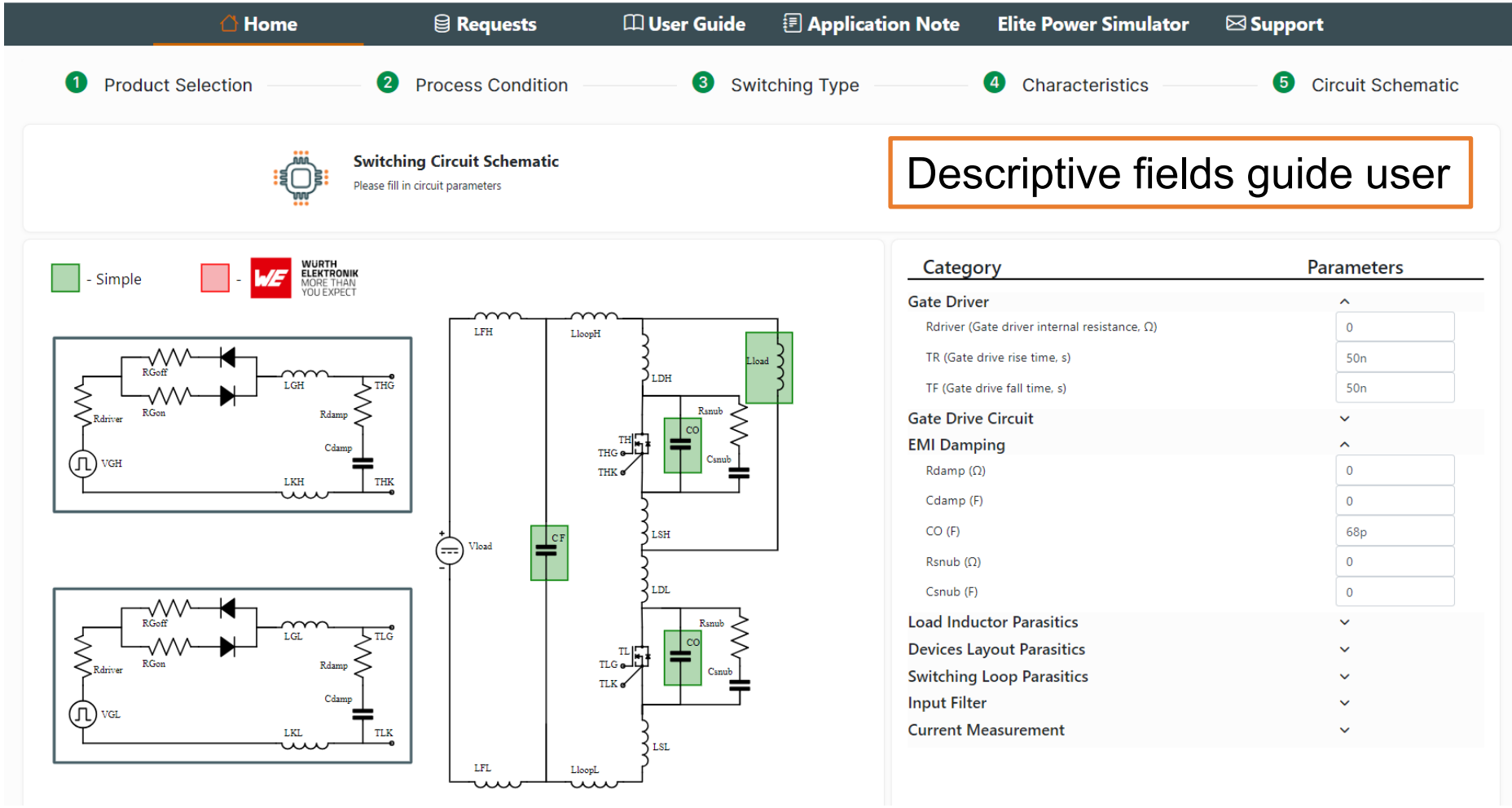
Step 4: Set Characteristics (Full-Soft Switching)

- Full Switching Changes:
  - Drain current is 1st and 3rd quadrant, so positive and negative when a switching event happens
- Full Switching Additions:
  - **dI/dt**: in the resonant inductor when the switching event happens. This dI/dt is directly linked to the resonant inductor voltage by the Faraday's law of induction E=L*di/dt. "didt" is a PLECS circuit parameter passed into the PLECS model to evaluate the losses in soft switching.
  - **Max Delay:** maximum dead time allowed between high side and low side switches for the resonant transition to occur
  - **Resonant Inductor**



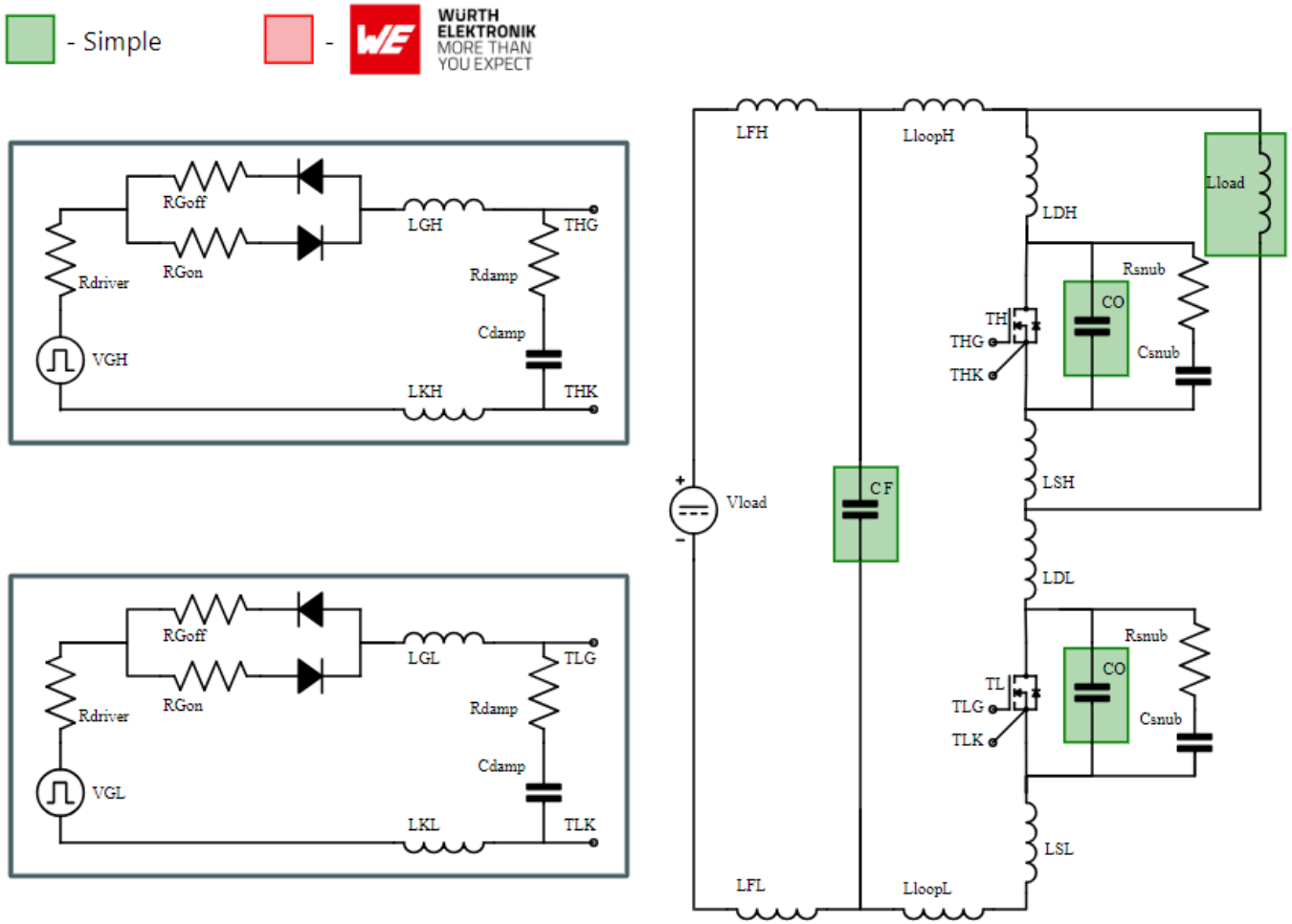
Step 5: Circuit Schematic (Half Bridge Discrete)

- Table of parameters matches circuit schematic.
- Default parameters are generally 0, allowing user to just enter needed values.
- Min and Max Gate Resistance parameter facilitate RG scaling in the PLECS model.
- Gate drive signal can be modeled through Rdriver, TF, and TR.
- Several passives can be set directly from Würth Elektronik component library. (See next slides)

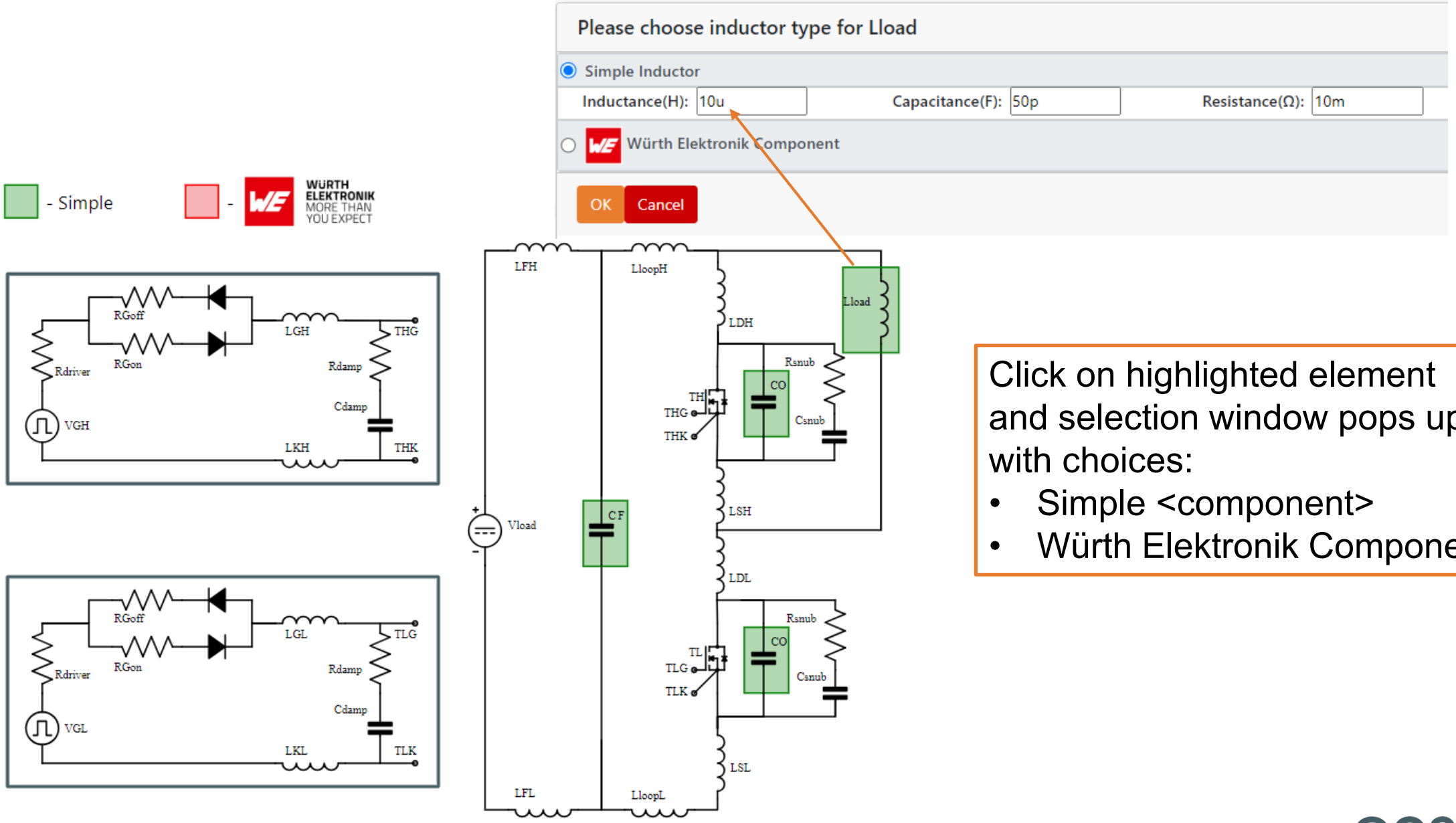


Würth Elektronik Components

- User can directly choose Würth Elektronik components for several passive elements in the switching circuit.
- Green box around the element denotes the standard value.
- Red box denotes an element was set through the Würth Elektronik library.
- The highlighted elements are clicked on directly to make the choice.



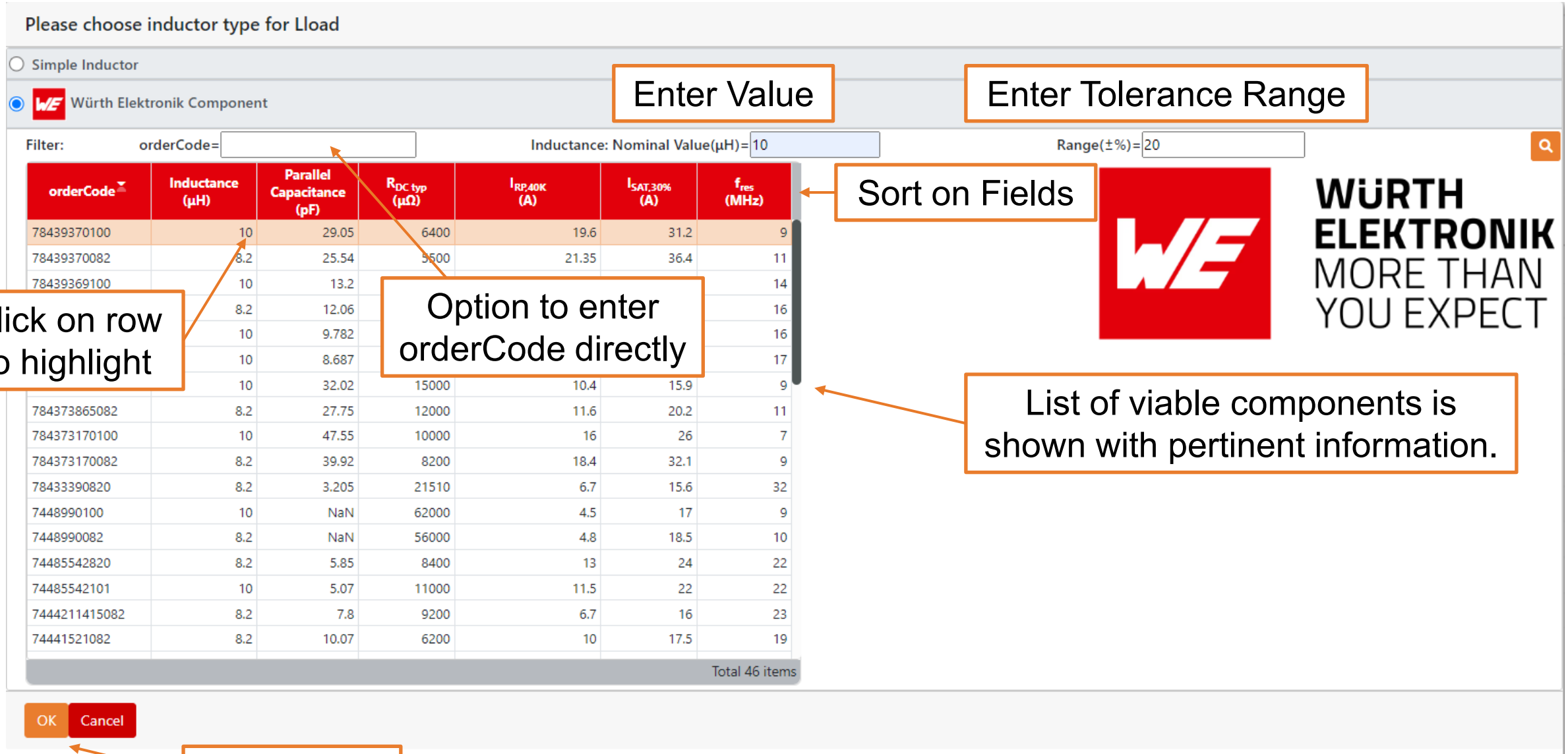
Würth Elektronik Components



Click on highlighted element and selection window pops up with choices:

- Simple <component>
- Würth Elektronik Component

Würth Elektronik Components



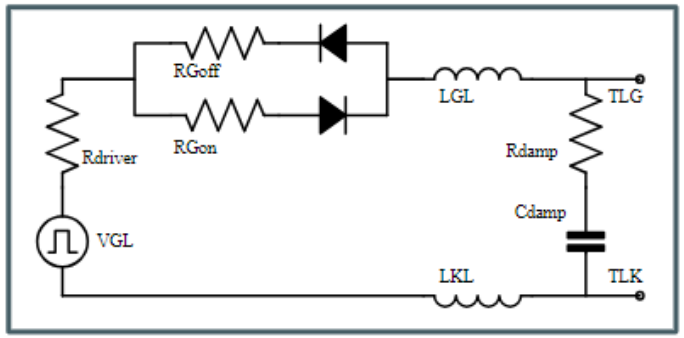
orderCode	Inductance (µH)	Parallel Capacitance (pF)	$R_{DC\ typ}$ (µΩ)	$I_{RP,40K}$ (A)	$I_{SAT,30\%}$ (A)	f_{res} (MHz)
78439370100	10	29.05	6400	19.6	31.2	9
78439370082	8.2	25.54	5500	21.35	36.4	11
78439369100	10	13.2				14
	8.2	12.06				16
	10	9.782				16
	10	8.687				17
	10	32.02	15000	10.4	15.9	9
784373865082	8.2	27.75	12000	11.6	20.2	11
784373170100	10	47.55	10000	16	26	7
784373170082	8.2	39.92	8200	18.4	32.1	9
78433390820	8.2	3.205	21510	6.7	15.6	32
7448990100	10	NaN	62000	4.5	17	9
7448990082	8.2	NaN	56000	4.8	18.5	10
74485542820	8.2	5.85	8400	13	24	22
74485542101	10	5.07	11000	11.5	22	22
7444211415082	8.2	7.8	9200	6.7	16	23
74441521082	8.2	10.07	6200	10	17.5	19

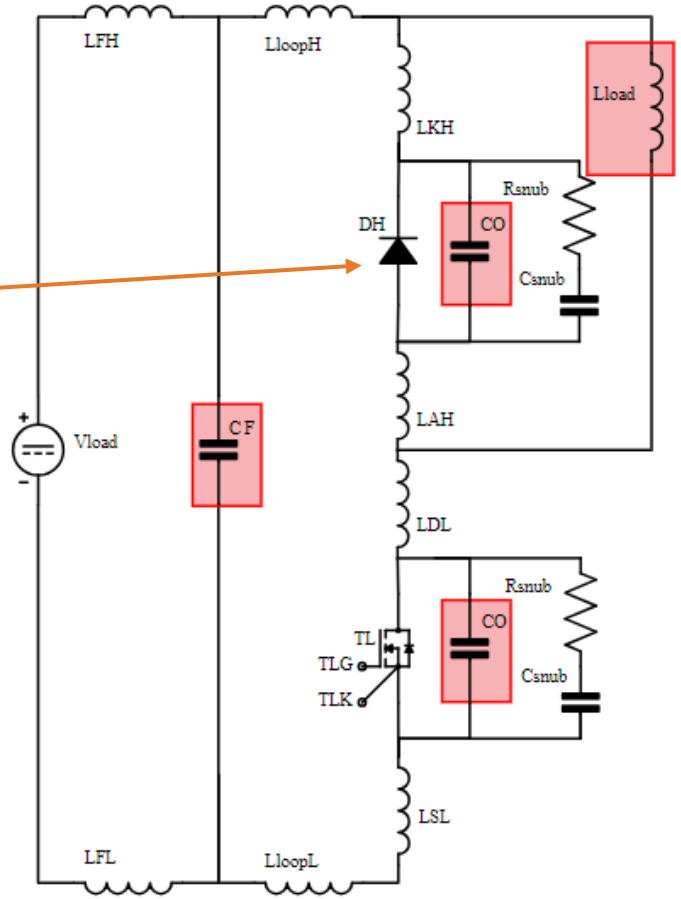
Total 46 items

Step 5: Circuit Schematic (Quarter Bridge Discrete)

- Simple
- WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

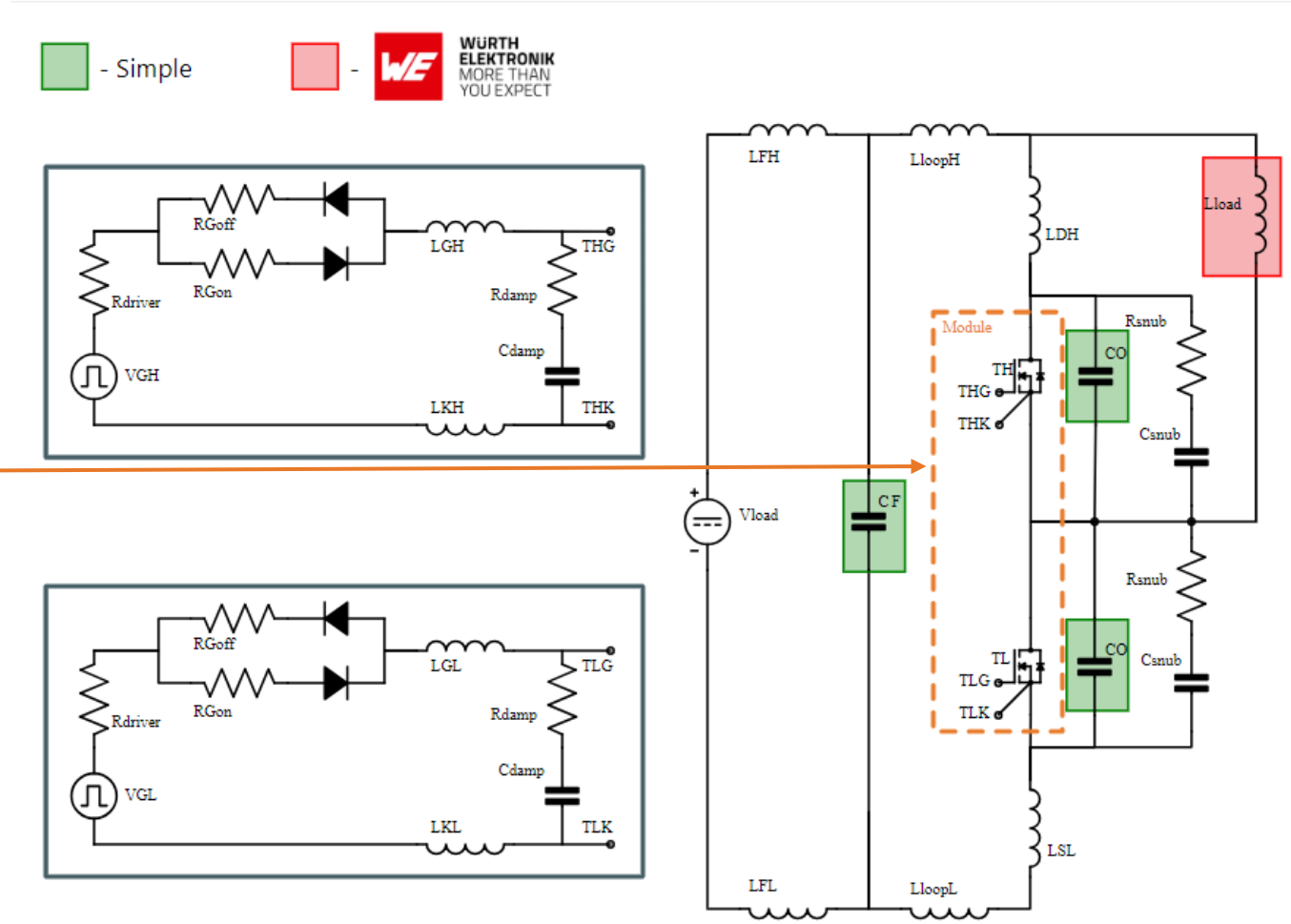
- High side choice can be:
  - Ideal diode with capacitance=0
  - EliteSiC Schottky diode





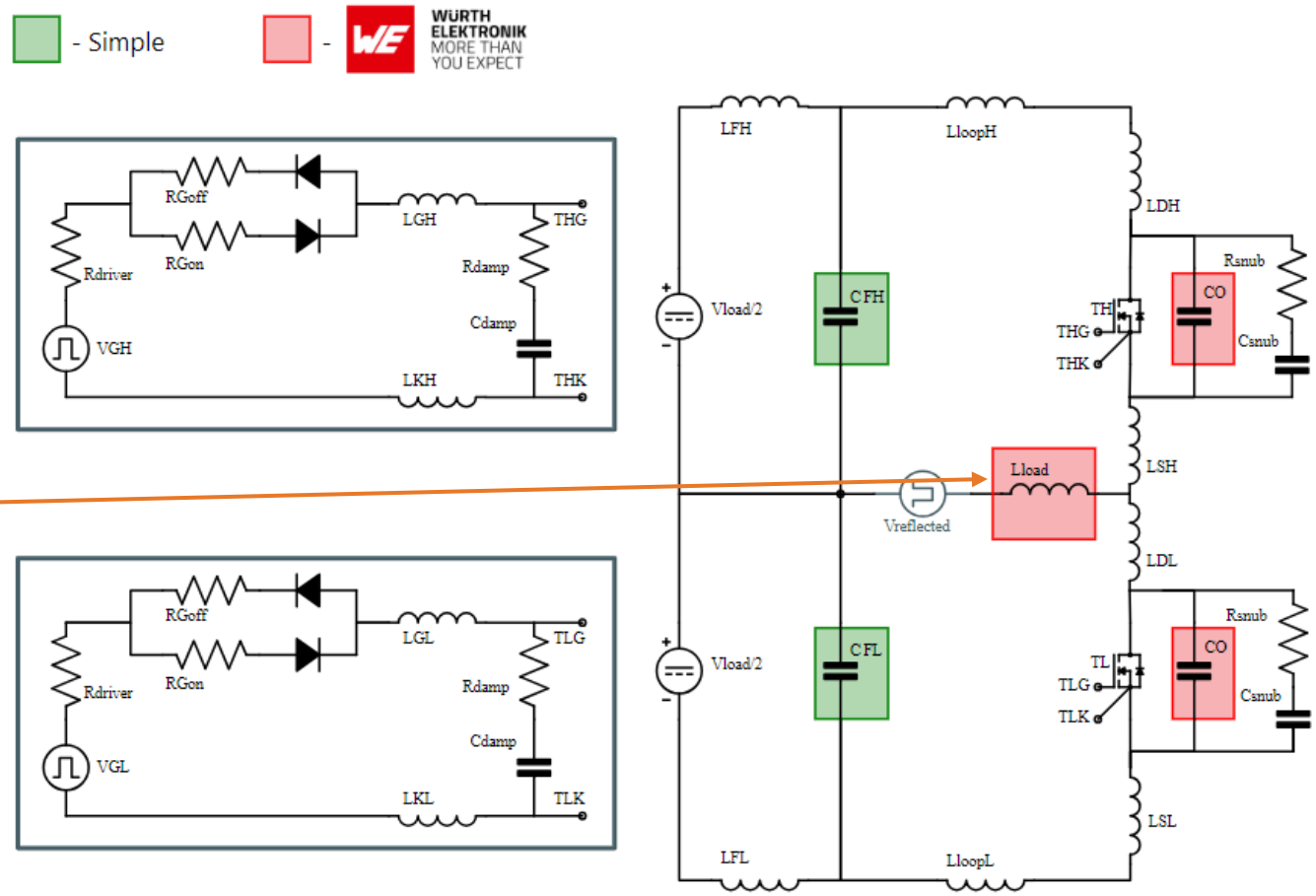
Step 5: Circuit Schematic (Half Bridge Module)

- All module parasitics are included in power module SPICE model.
- Remaining parameters are the same as discrete version.



Step 5: Circuit Schematic (Full-Soft Switching)

- Lload corresponds to Resonant Inductor.



Step 5: Circuit Parameters – Full list

Input Filter	
RCF (Ω)	0.2m
LCF (H)	2n
CF (F)	3n
LFH (H)	5n
RLFH (Ω)	0.1m
LFL (H)	5n
RLFL (Ω)	0.1m

Devices Layout Parasitics	
LDH (H)	2n
RDH (H)	0.1m
LSH (H)	2n
RSH (Ω)	0.1m
RDL (Ω)	0.1m
LDL (H)	2n
LSL (H)	2n
RSL (Ω)	0.1m

Switching Loop Parasitics	
RloopH (Ω)	0.1m
LloopH (H)	2n
RloopL (Ω)	0.1m
LloopL (H)	2n

Load Inductor Parasitics	
Rload (Ω)	5m
Cload (F)	22p

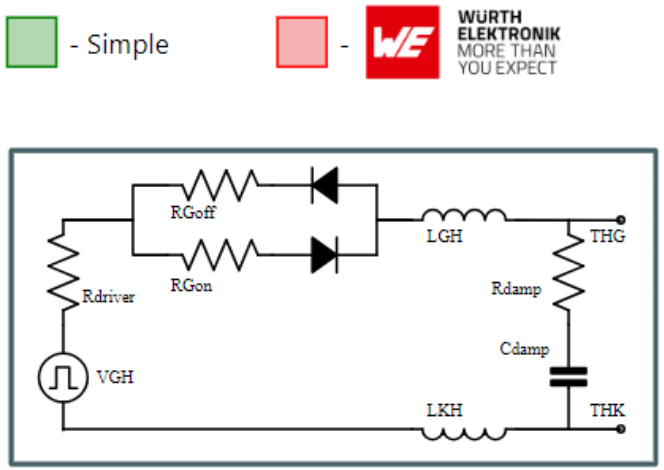
EMI Damping	
Rdamp (Ω)	100
Cdamp (F)	47p
CO (F)	100p
Rsnub (Ω)	1
Csnub (F)	200p

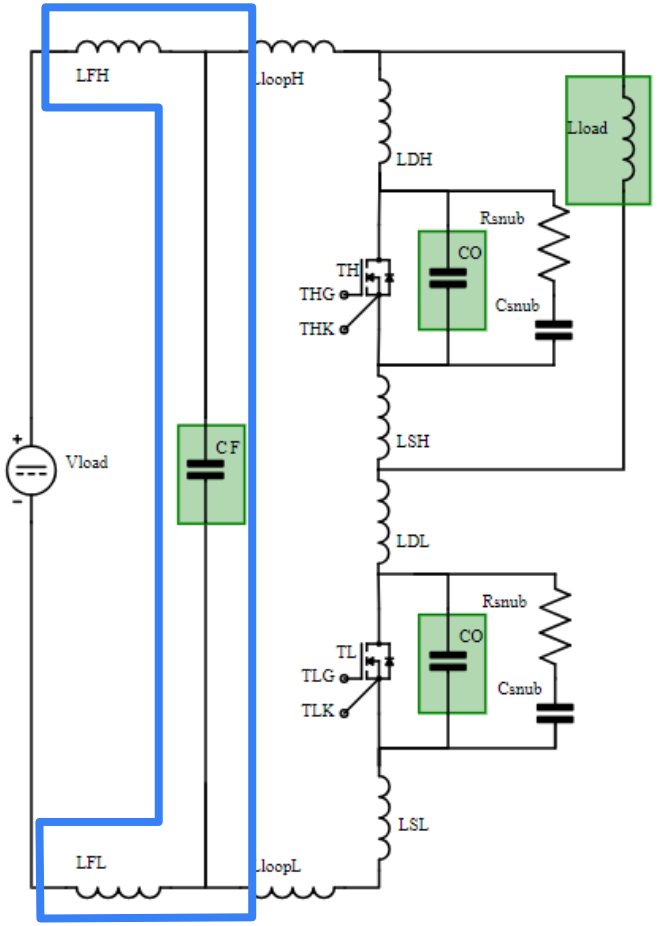
Current Measurement	
Rshunt (Ω)	1m
Rshunt Location	RSL

Gate Drive Circuit	
RGoff (Default OFF Gate Resistance, Ω)	2
RGon (Default ON Gate Resistance, Ω)	2
RGoffMIN (Min OFF Gate Resistance, Ω)	2
RGoffMAX (Max OFF Gate Resistance, Ω)	10
RGonMIN (Min ON Gate Resistance, Ω)	2
RGonMAX (Max ON Gate Resistance, Ω)	10
LGH (H)	5n
LKH (H)	5n
LGL (H)	5n
LKL (H)	5n

Gate Driver	
Rdriver (Gate driver internal resistance, Ω)	1
TR (Gate drive rise time, s)	50n
TF (Gate drive fall time, s)	50n

Step 5 : Input Filter Parameters





Input Filter	
RCF (Ω)	0.2m
LCF (H)	2n
CF (F)	3n
LFH (H)	5n
RLFH (Ω)	0.1m
LFL (H)	5n
RLFL (Ω)	0.1m

LFx (with RLFx as series resistance) is the PCB leakage inductance or a discrete filtering inductor.

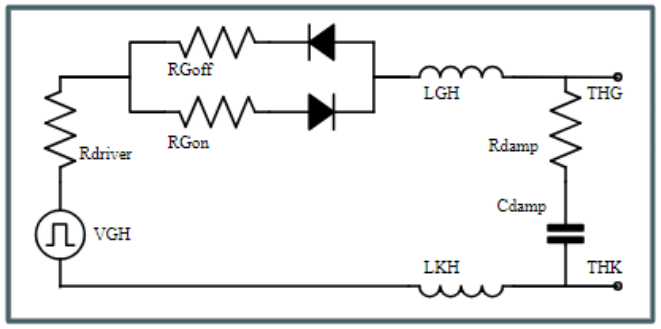
The simple filter capacitor or decoupling capacitor CF includes ESL(LCF) and ESR(RCF) parameters.

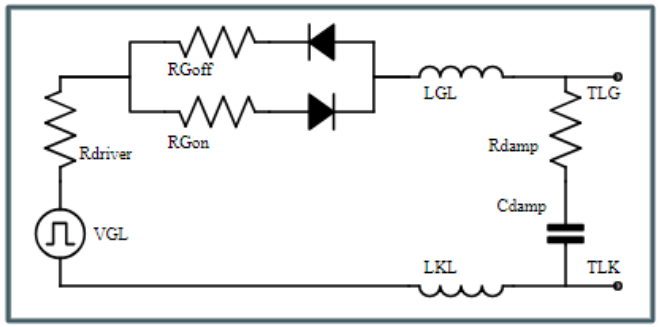
Alternatively, Würth capacitors can be chosen with fully characterized parasitics.

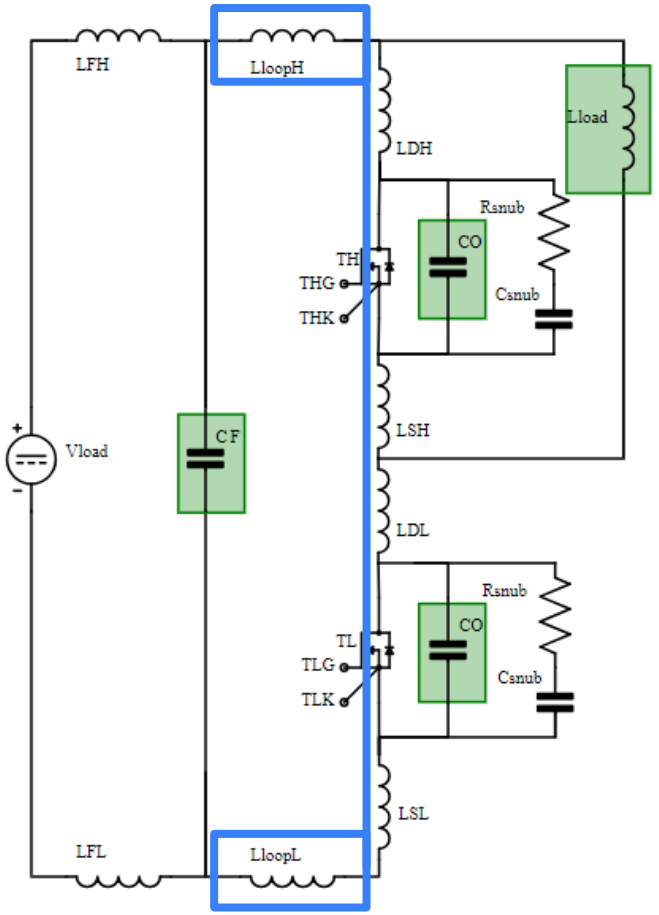
Step 5 : Switching Loop Leakage Inductances

- Simple

- WÜRTH ELEKTRONIK MORE THAN YOU EXPECT







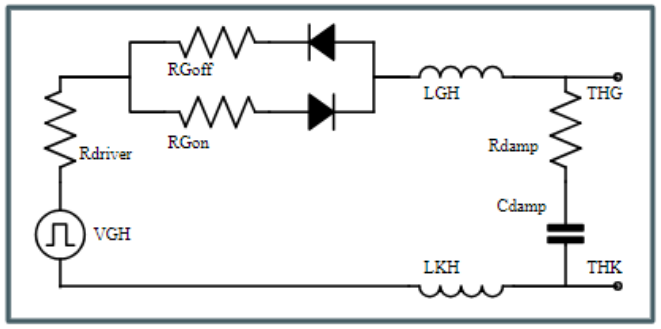
Switching Loop Parasitics	
RloopH (Ω)	0.1m
LloopH (H)	2n
RloopL (Ω)	0.1m
LloopL (H)	2n

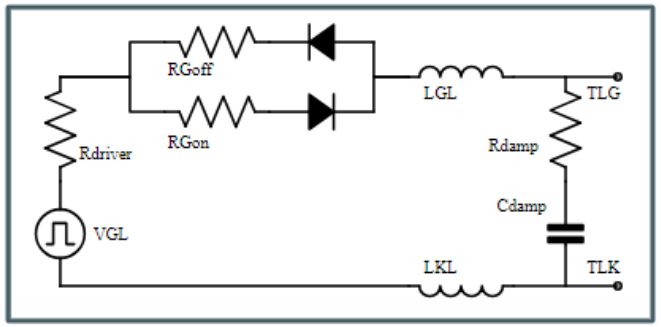
The switching loop inductance (in between the decoupling capacitor and the switching cell) is represented by Lloopx (with Rloopx as series resistance) on the positive and negative branch.

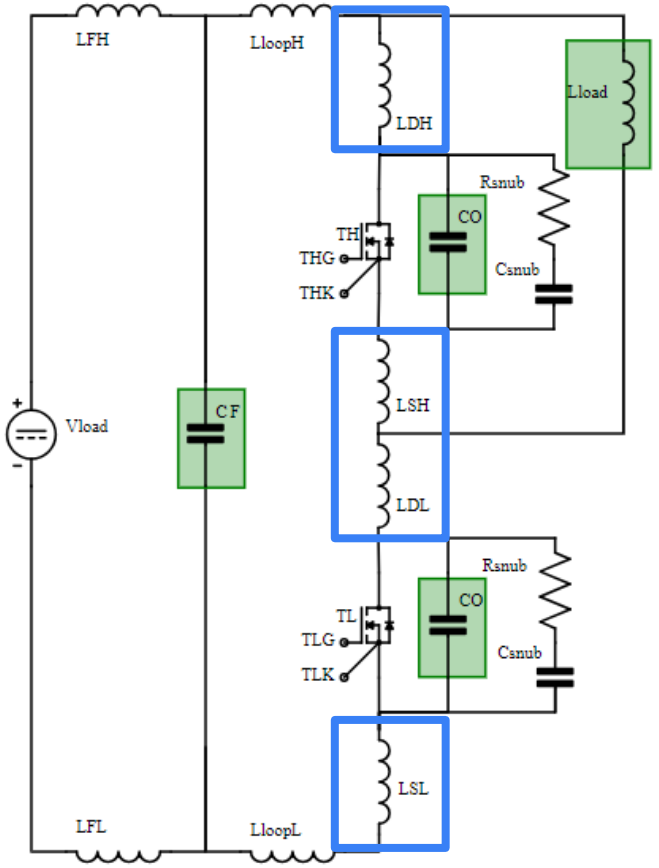
Step 5 : Interconnections leakage inductances

- Simple

- WÜRTH ELEKTRONIK MORE THAN YOU EXPECT



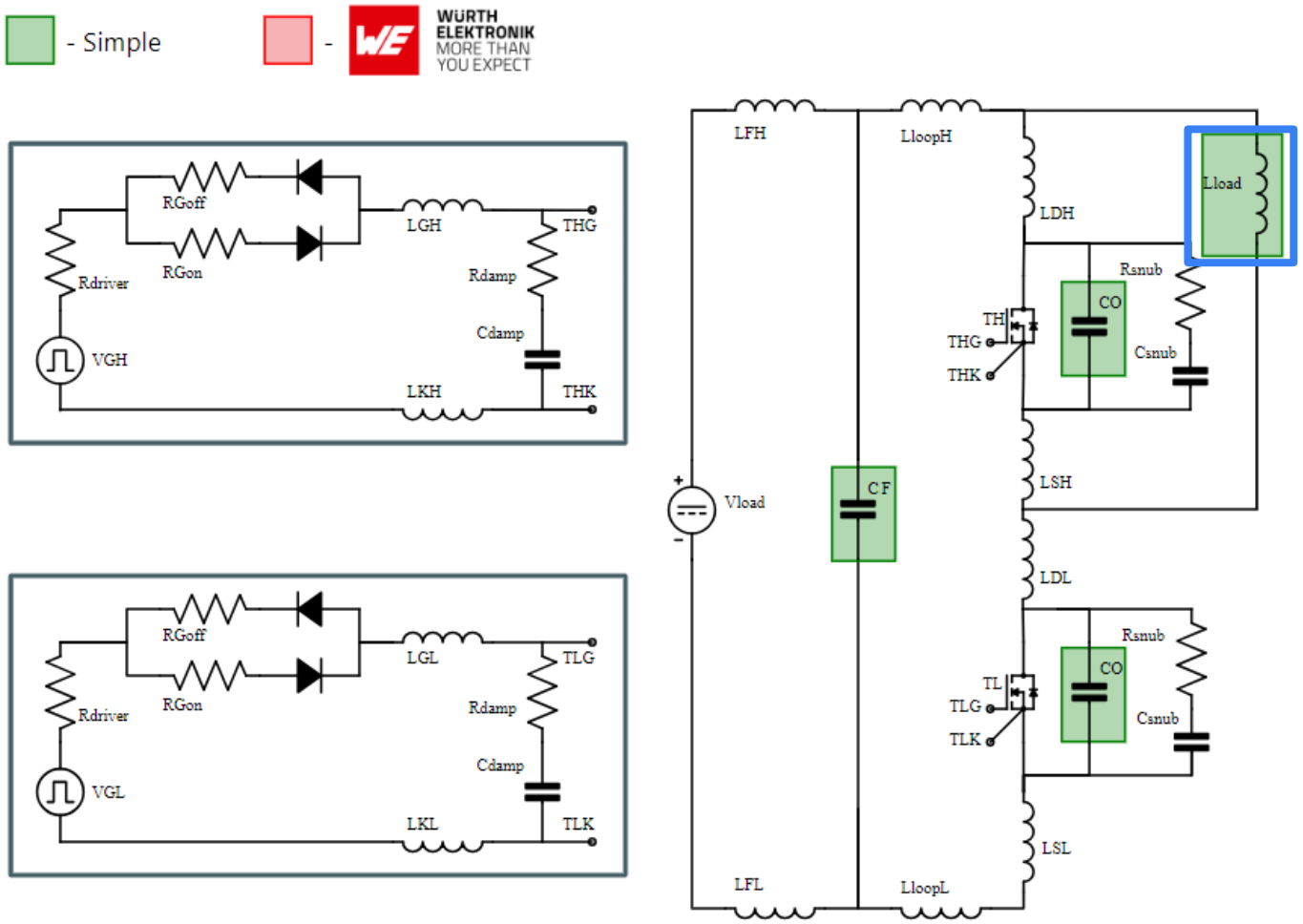




Devices Layout Parasitics	
LDH (H)	2n
RDH (H)	0.1m
LSH (H)	2n
RSH (Ω)	0.1m
RDL (Ω)	0.1m
LDL (H)	2n
LSL (H)	2n
RSL (Ω)	0.1m

Drain and Source interconnections can also be modeled by inductances (with series resistances). There are 4 in total for the two switching devices.

Step 5 : Load parameters



Load Inductor Parasitics	
Rload (Ω)	5m
Cload (F)	22p

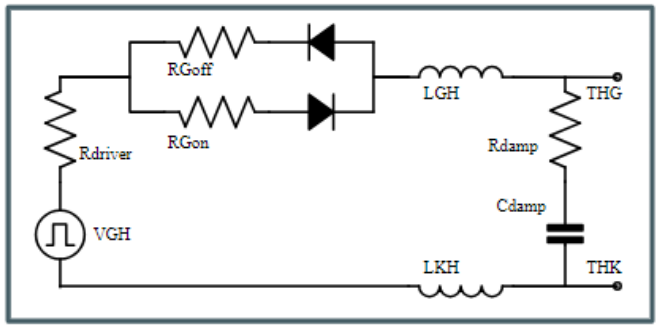
For simple inductor, the inductor quality or performances are defined by an equivalent series resistance (Rload) and an equivalent parallel parasitic capacitor (Cload).

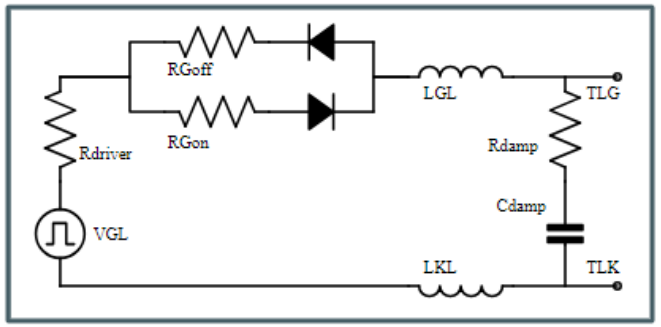
Alternatively, Würth inductors can be chosen with fully characterized parasitics.

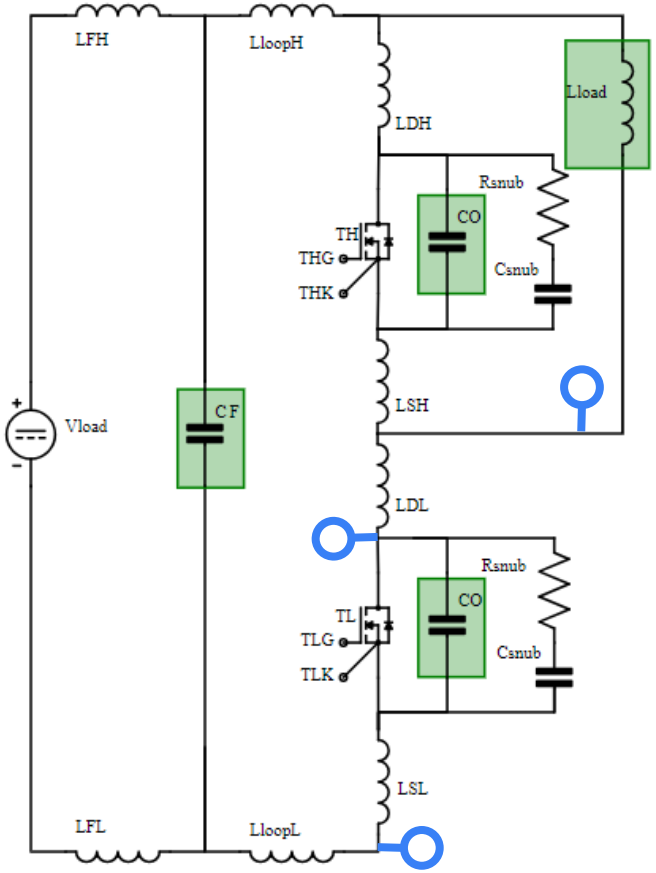
Step 5 : Current Sense parameters

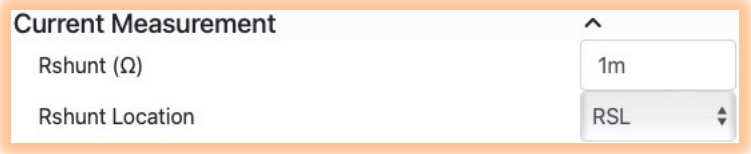
- Simple

- WÜRTH ELEKTRONIK MORE THAN YOU EXPECT









A current sense measurement based on a shunt resistor can be included in the loop in various places:

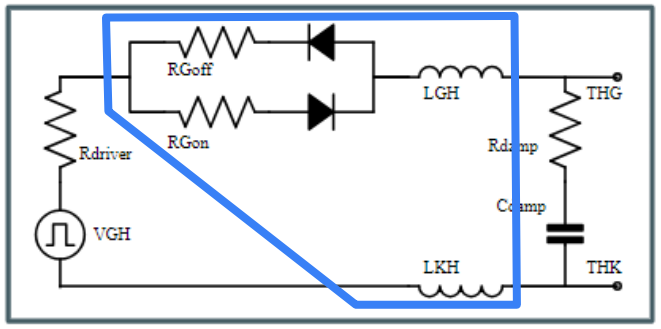
- in switching device Drain,
- in switching device Source
- in switching inductor

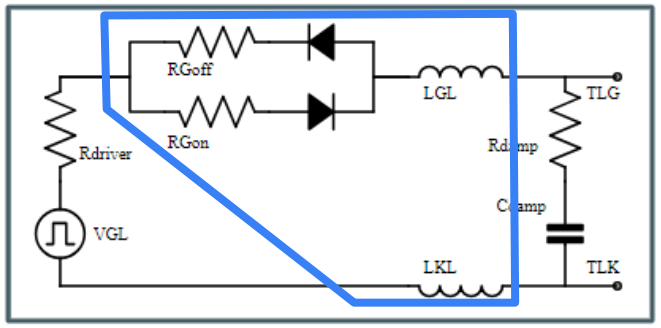
If the shunt is in either the device drain or source, the interconnection series resistance can be increased accordingly.

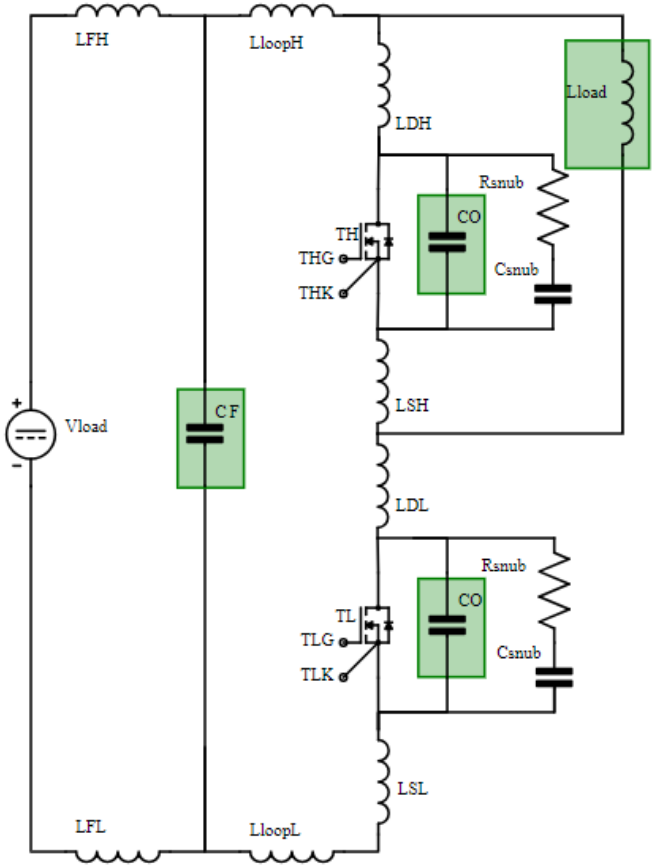
Step 5 : Gate Drive Circuit parameters

- Simple

- WÜRTH ELEKTRONIK MORE THAN YOU EXPECT







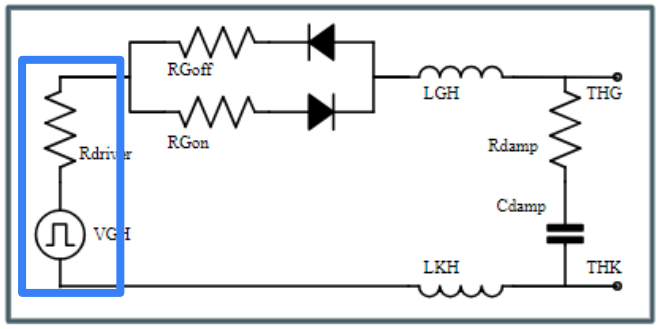
Gate Drive Circuit	
RGoff (Default OFF Gate Resistance, Ω)	2
RGon (Default ON Gate Resistance, Ω)	2
RGoffMIN (Min OFF Gate Resistance, Ω)	2
RGoffMAX (Max OFF Gate Resistance, Ω)	10
RGonMIN (Min ON Gate Resistance, Ω)	2
RGonMAX (Max ON Gate Resistance, Ω)	10
LGH (H)	5n
LKH (H)	5n
LGL (H)	5n
LKL (H)	5n

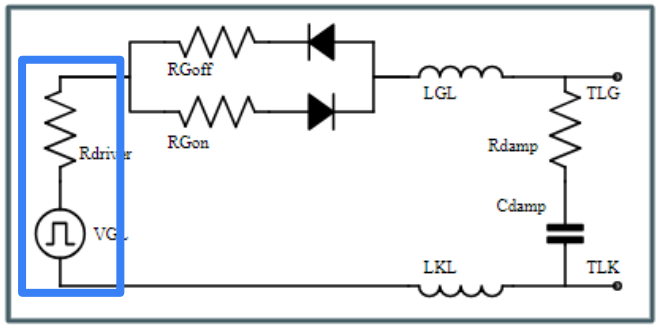
The gate drive circuit includes two parasitic inductances LGx and LKx for interconnection and split gate resistors (RGon and RGoff) to control turn-on and turn-off speed.

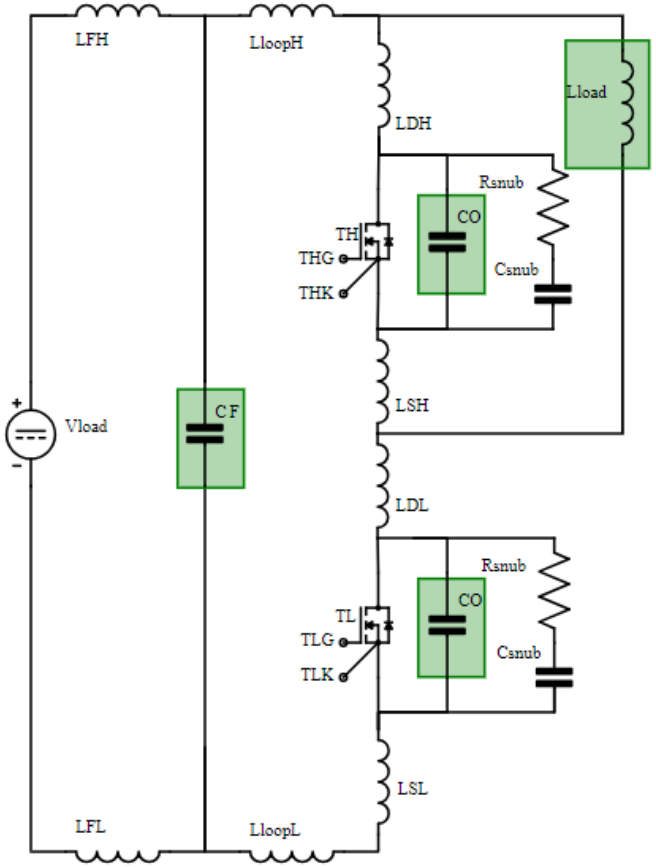
Step 5 : Driver extra parameters

- Simple

- WÜRTH ELEKTRONIK MORE THAN YOU EXPECT





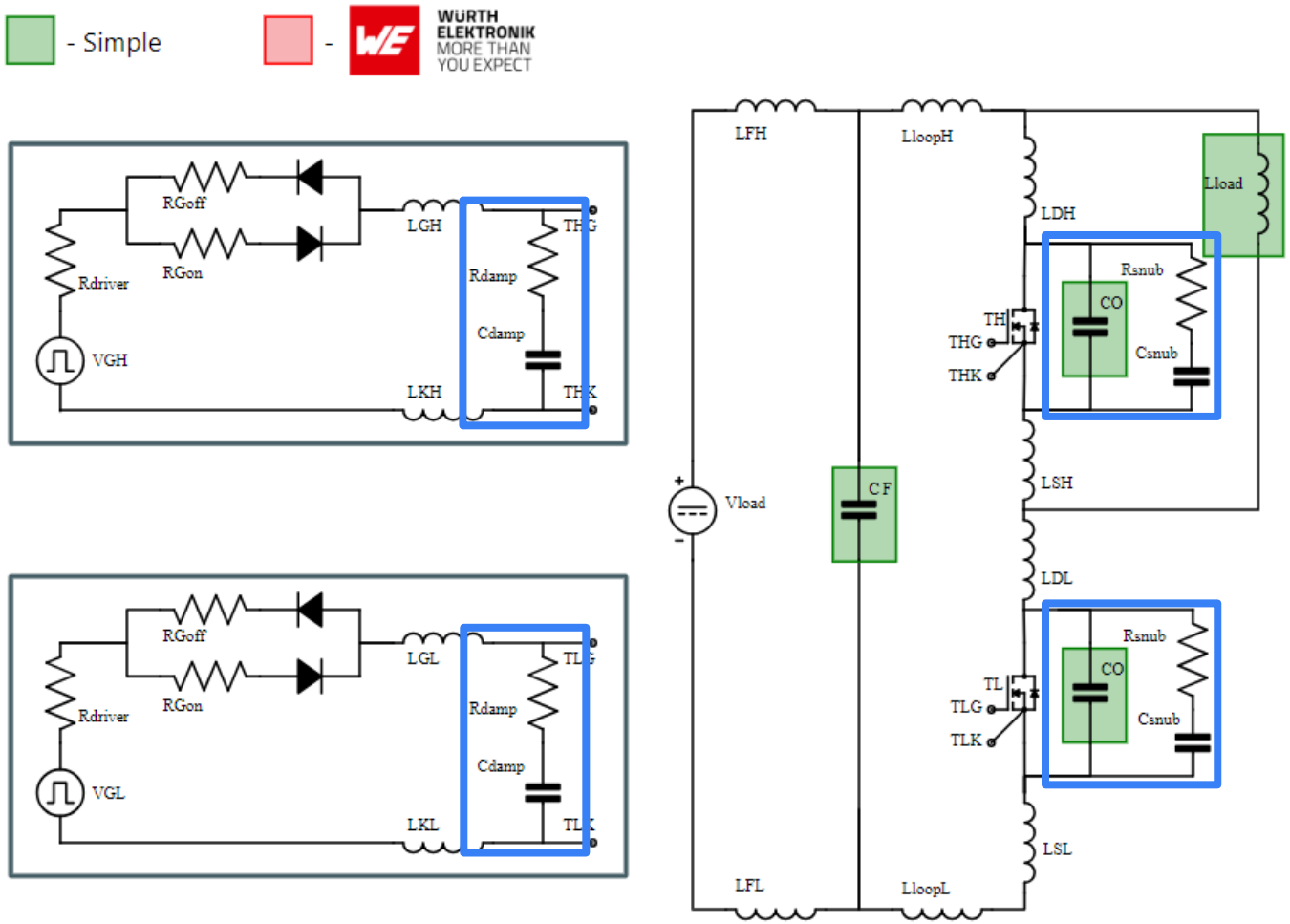


Gate Driver	
Rdriver (Gate driver internal resistance, Ω)	1
TR (Gate drive rise time, s)	50n
TF (Gate drive fall time, s)	50n

The driver is model by a pulse voltage source with Minimum and Maximum (ON and OFF) voltage defined in Step 4.

In Step 5, the user defines the Rise (TR) and Fall (TF) times. The user can also give the driver internal resistance value Rdriver.

Step 5 : EMI Damping parameters



EMI Damping	
Rdamp (Ω)	100
Cdamp (F)	47p
CO (F)	100p
Rsnub (Ω)	1
Csnub (F)	200p

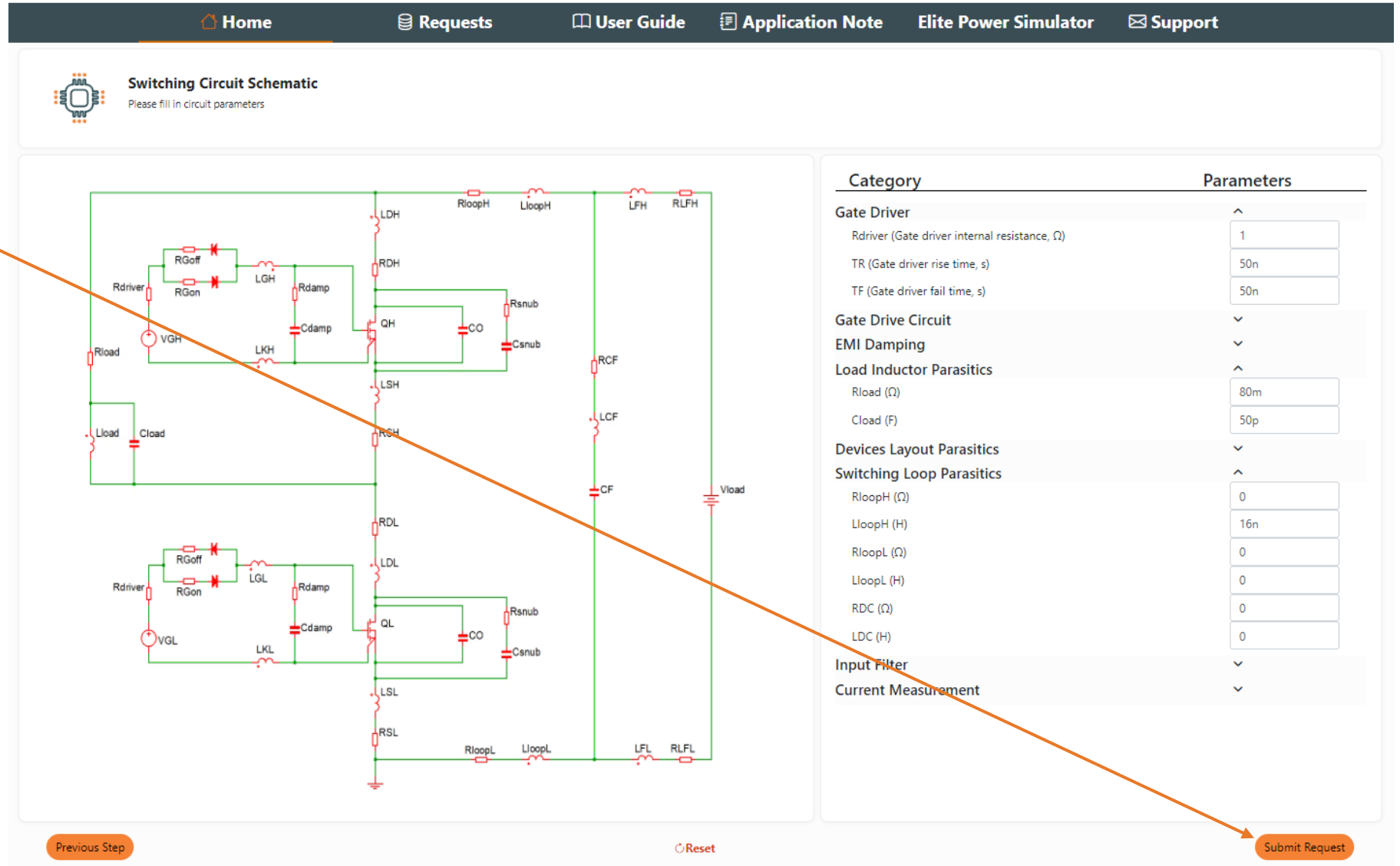
For EMI reduction, two damping circuits can be added.

Between Drain to Source, a parallel capacitor linearizes the switching device output capacitor. A snubber circuit can also be added.

Between Gate and (Kelvin) Source, an R-C series damping network will damp the Miller effect ringing.

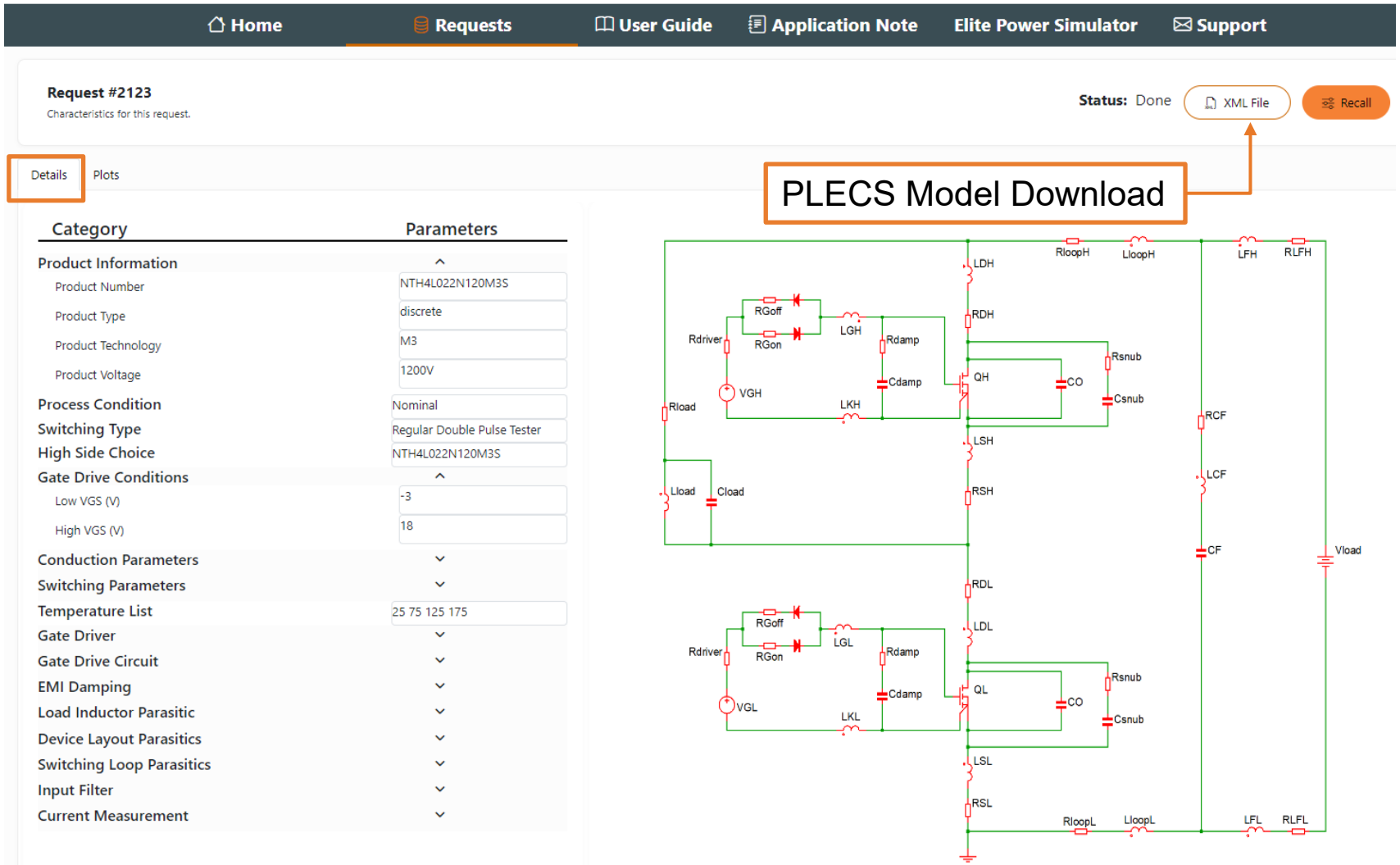
Step 6: Submit Request

- From the Circuit Schematic Tab, once the circuit parameters are entered, **Submit Request** button becomes active.
- User clicks on **Submit Request** and is brought to the Request Details page
- Requests take several minutes to complete depending on the density of the input characteristics.
- Modules take longer due to higher complexity compared to discretes.



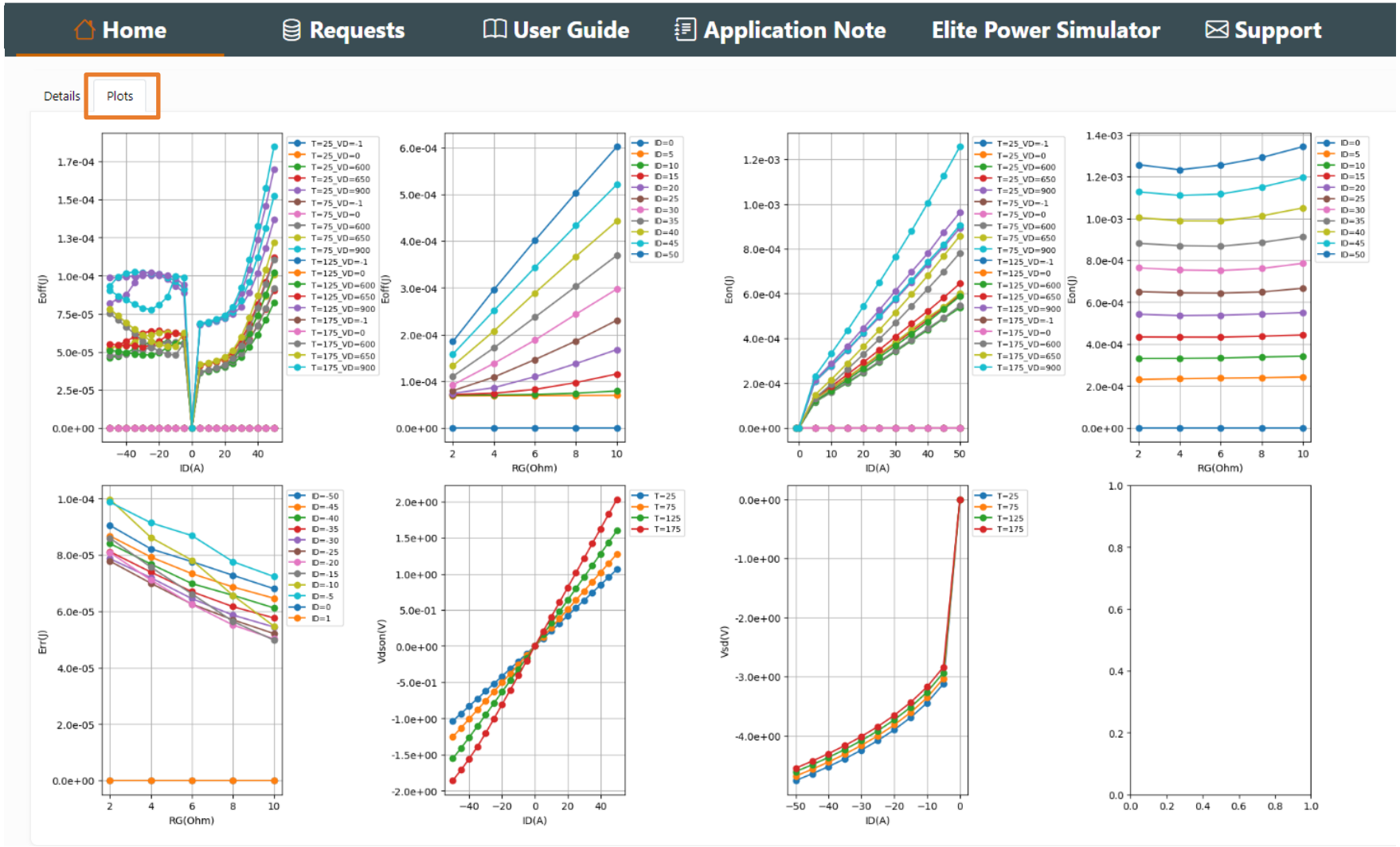
Step 7: Review Request Details Page

- The Request Details page provides user with
  - Details of the input parameters
  - Plots of the simulation results
  - Status field:
    - Pending – simulation in queue
    - Running – simulation running
    - Done – simulation completed
  - PLECS Model (XML File) download
  - Recall button: Enable users to recall the current request into a new request where changes can be made before submitting the new request. The current request is maintained.

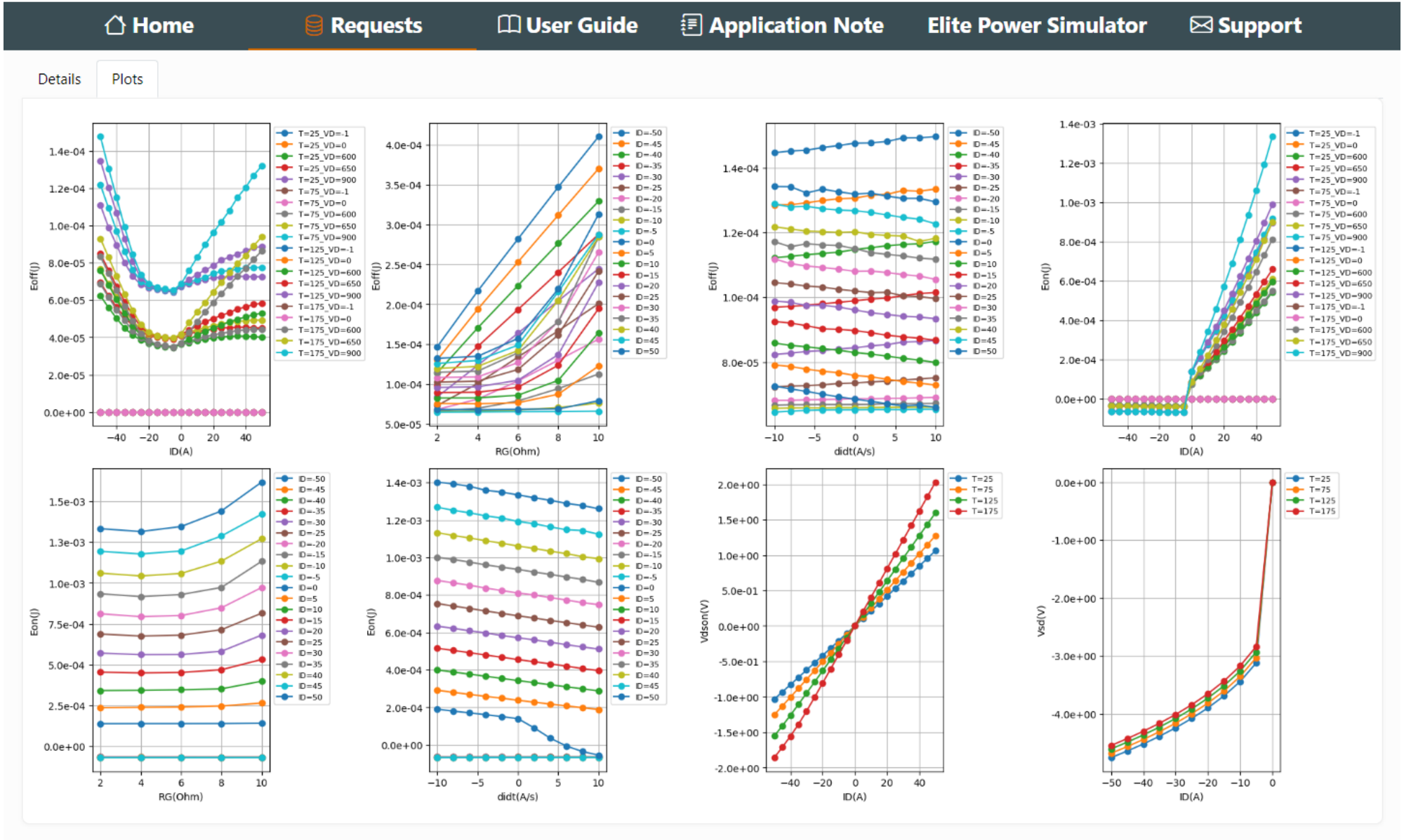


Step 7: Review Request Details Page – Plots Tab

- The Plots tab provides users with multiple plots representing the data in the XML file.
  - Eoff, Eon, Err vs. ID (current) for different temperatures and voltage @default RG
  - Eoff at negative ID is essentially Err.
  - Eoff, Eon, Err vs. RG for different currents @maximum temperature and voltage.
  - Transistor conduction plot VDSon vs. ID for different temperatures.
  - Diode conduction plot Vsd vs. ID for different temperatures.



Example Full Switching Model Results

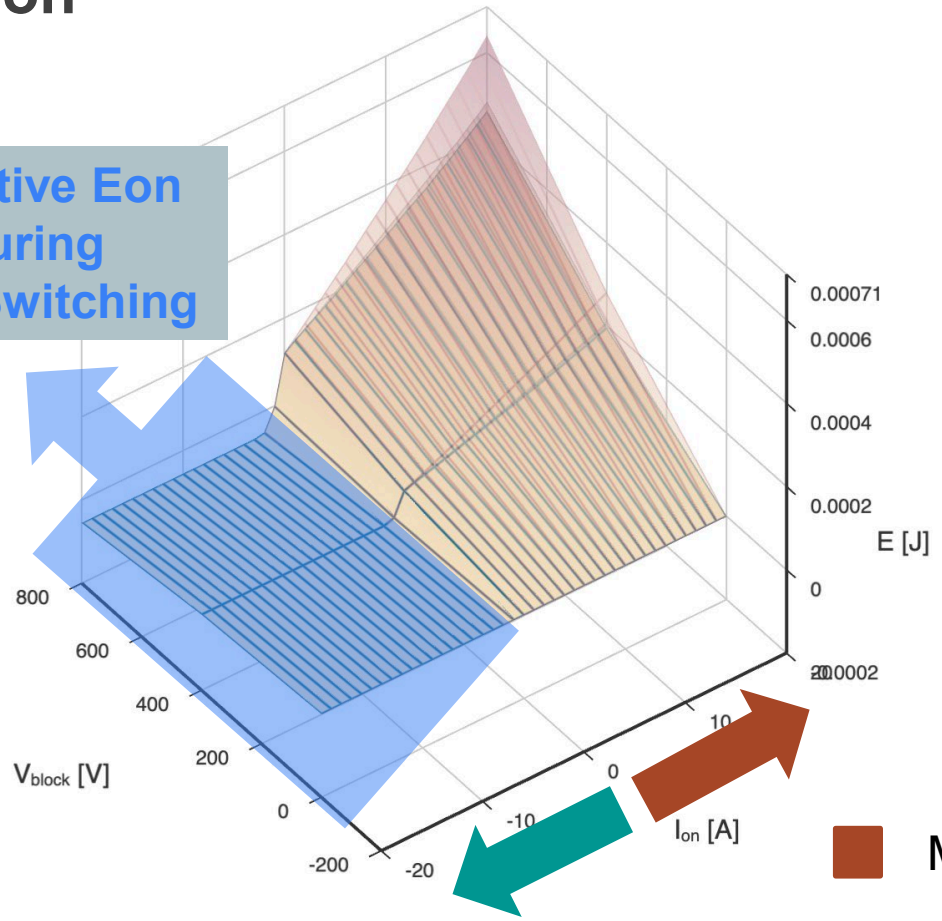


Example Full Switching Model Results

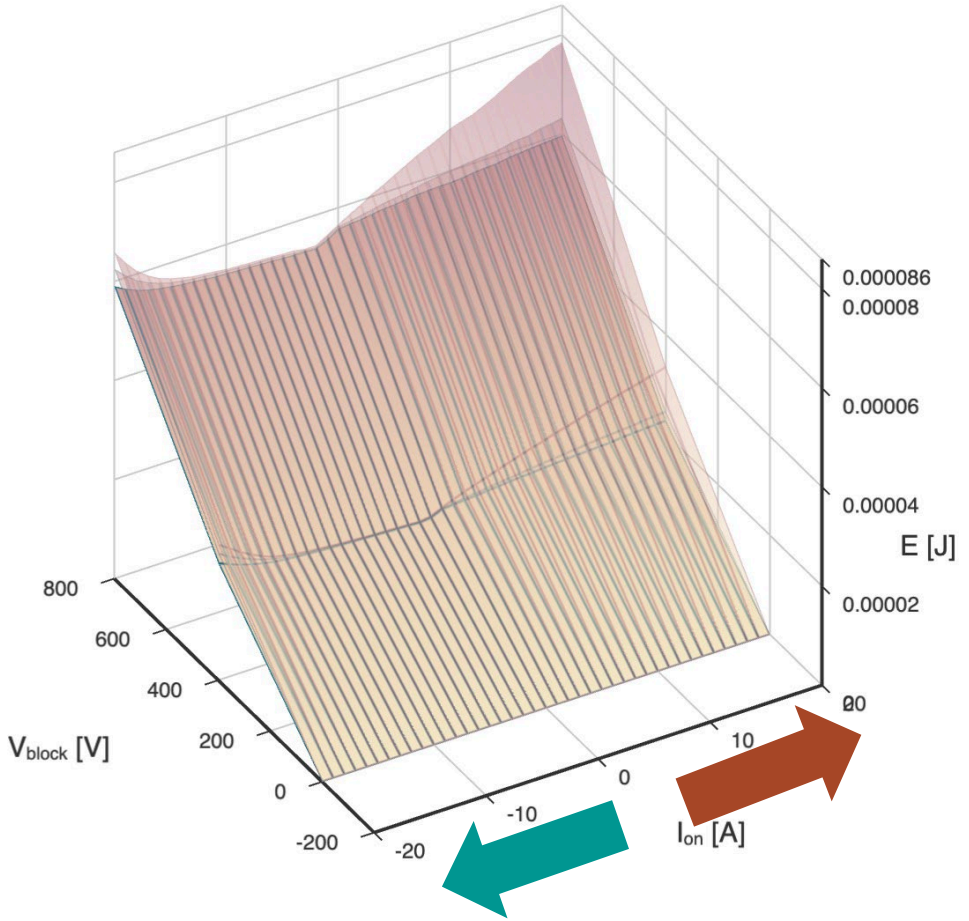
Example Full Switching Model Results: 3D View

- Eon

Negative Eon during Soft-Switching



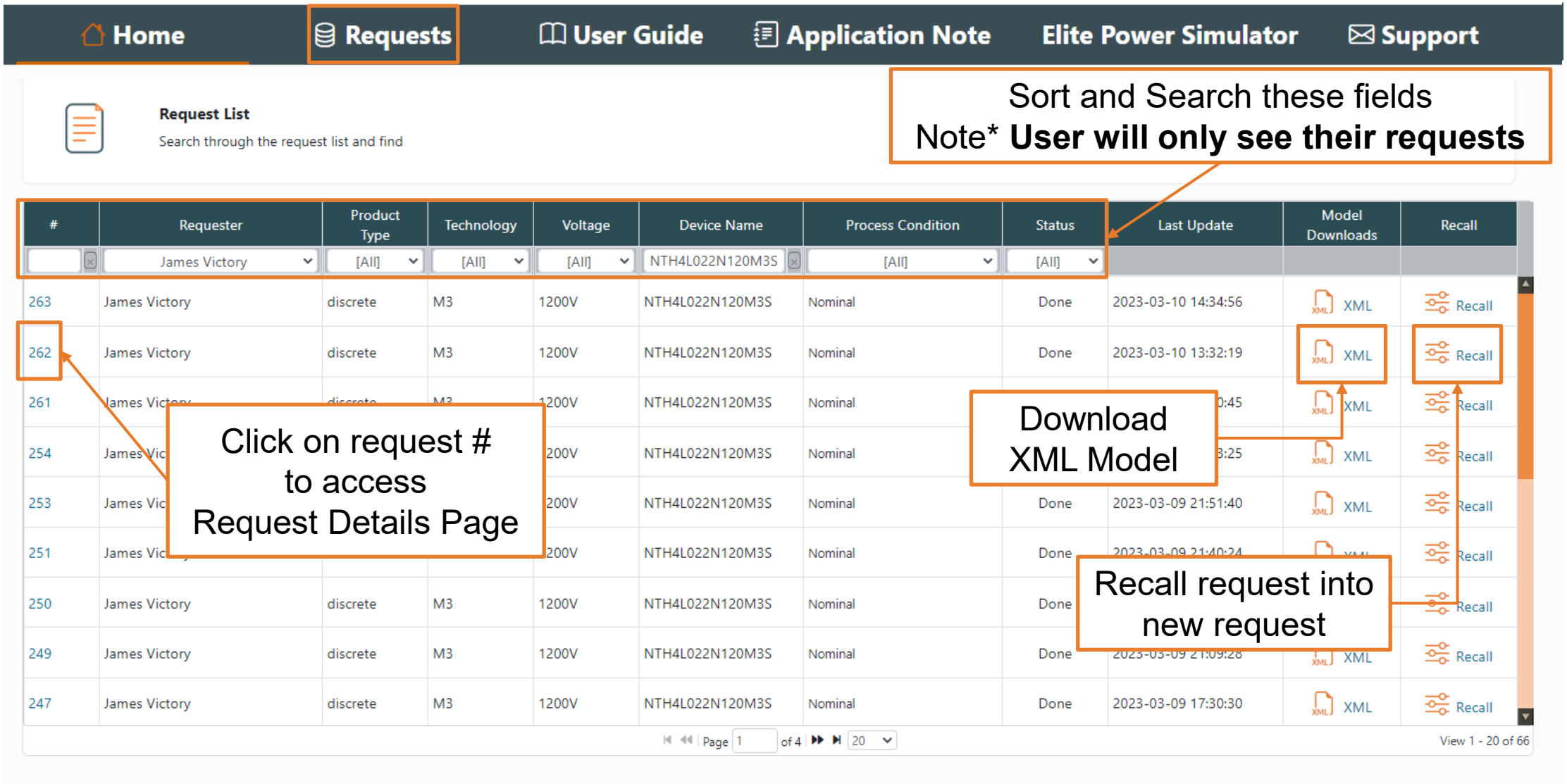
- Eoff



Main Switch

Synchronous Rectifier

Step 8: Review Requests Summary Page



#	Requester	Product Type	Technology	Voltage	Device Name	Process Condition	Status	Last Update	Model Downloads	Recall
	James Victory	[All]	[All]	[All]	NTH4L022N120M3S	[All]	[All]			
263	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-10 14:34:56	XML	Recall
262	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-10 13:32:19	XML	Recall
261	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal		:45	XML	Recall
254	James Vic			200V	NTH4L022N120M3S	Nominal		:25	XML	Recall
253	James Vic			200V	NTH4L022N120M3S	Nominal	Done	2023-03-09 21:51:40	XML	Recall
251	James Vic			200V	NTH4L022N120M3S	Nominal	Done	2023-03-09 21:40:24	XML	Recall
250	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done			Recall
249	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-09 21:09:28	XML	Recall
247	James Victory	discrete	M3	1200V	NTH4L022N120M3S	Nominal	Done	2023-03-09 17:30:30	XML	Recall

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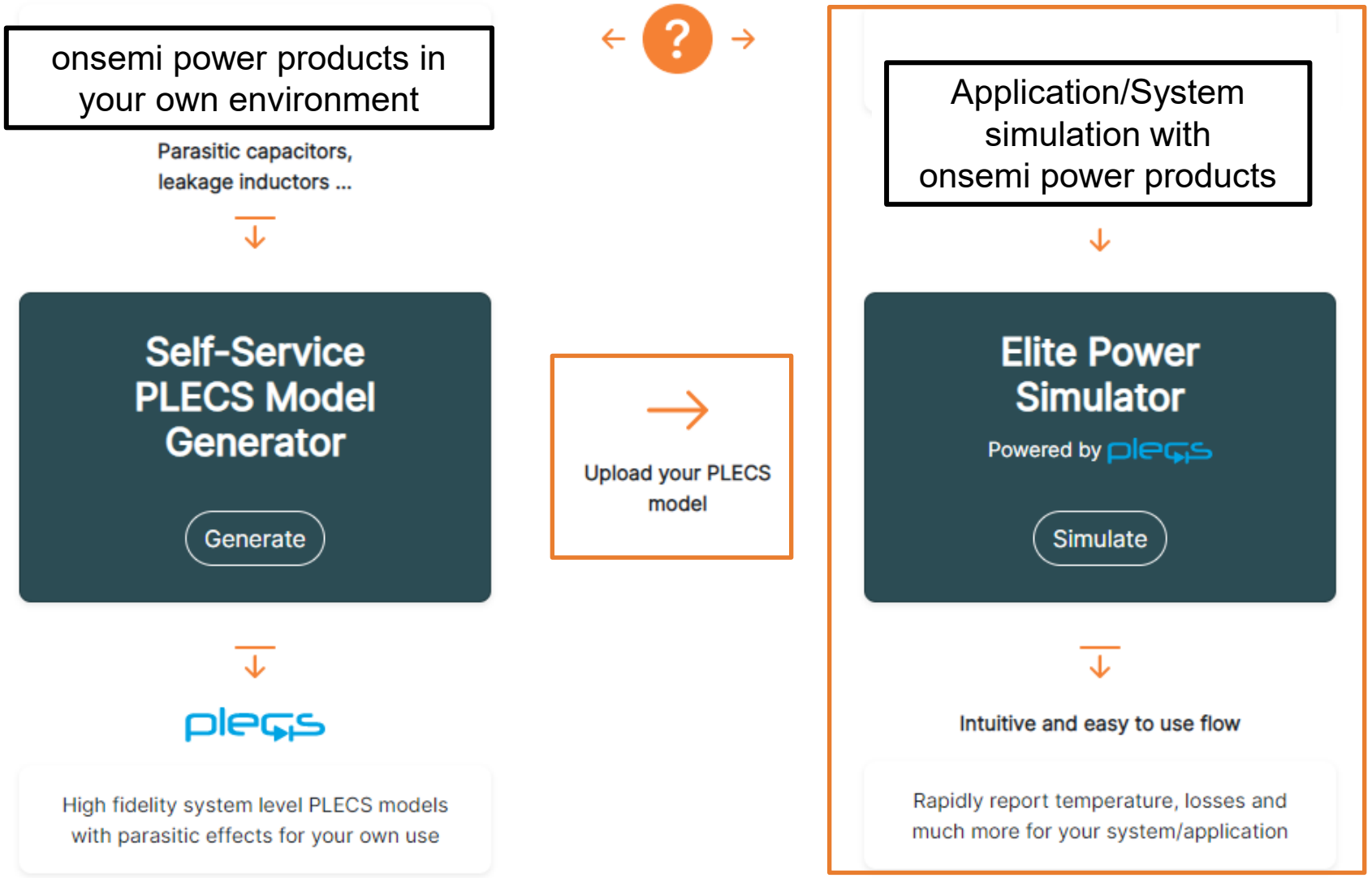
FAQ: Common Causes of SSPMG Failed Runs

- Very small switching current step (<1A) causing very long simulation times while not really improving the accuracy of the table model.
- Switching currents too close to 0 (<1A): In the EOFF extraction, 1% ID point by IEC standard will yield very small currents which can cause extraction errors due to leakage. For example, when ID=0.1A,the 1%ID will be only 1mA,which could be less than the leakage for some high temperature conditions.
- Switching load voltages are too low. Very low Vload can cause errors in the EON extraction, in which we need to measure 3% VDS by IEC standard.
- Switching load voltage too close to the device breakdown voltage BV can cause issues if there is overshoot of VDS in turn off. If the overshoot is higher than BV, the breakdown current will generate strange behaviors.
- For full switching, users may put very small negative current. For these inputs, there would be only 1 or 2 points for negative current yielding poor results. There should be at least 3 points in the negative current range.
  - Iswitch_min=-1 Iswitch_max=50 Iswitch_step=5
  - Iswitch_min=-10 Iswitch_max=50 Iswitch_step=5
- Very large dI/dt could cause convergence issues or very strange behavior.
- In general user should check ranges of parasitics. Unreasonably large inductors, resistors, and capacitors can cause issues. For example, large CLOAD/CO could cause very long turn on/off edge.

Outline of User Guide

1	Introduction to Self-Service PLECS Model Generator: What is it and What are the benefits
2	Step by Step Tool Flow
3	Deploying PLECS Models in Elite Power Simulator and PLECS Stand Alone

Deploying SSPMG PLECS Models in the Elite Power Simulator



Load SSPMG models into Elite Power Simulator

In Device Configuration Tab, user can select to upload SSPMG generated model

Application — Device Selection — 3 Device Configuration — 4 Circuit Parameters

MOSFET configuration

Device name: **NTH4L022N120M3S**

Number of parallel devices

Value *

1

Turn-on gate resistance $R_{g\text{-}on,ext}$

Value *

4.5

Turn-off gate resistance $R_{g\text{-}off,ext}$

Value *

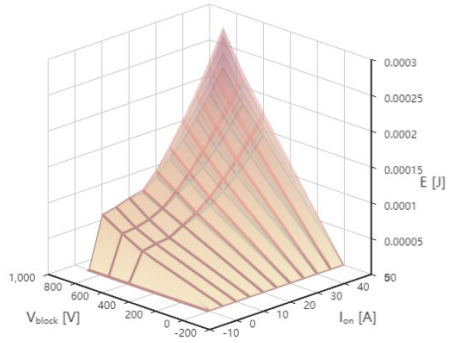
4.5

Loss model type

- ○ Nominal loss data
- ○ Best case conduction loss/worst case switching loss
- ○ Worst case conduction loss/best case switching loss
- ◉ Upload PLECS custom loss model from onsemi's SSPMG tool

Model data file

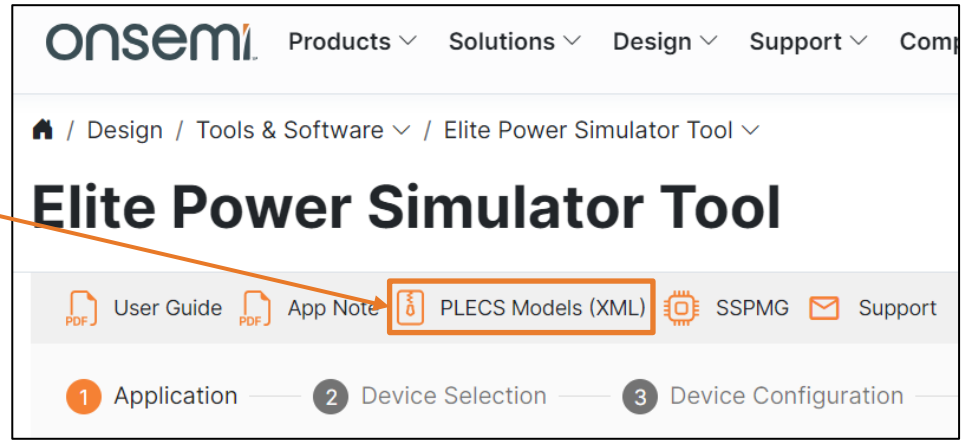
Select model file — Browse for SSPMG XML file

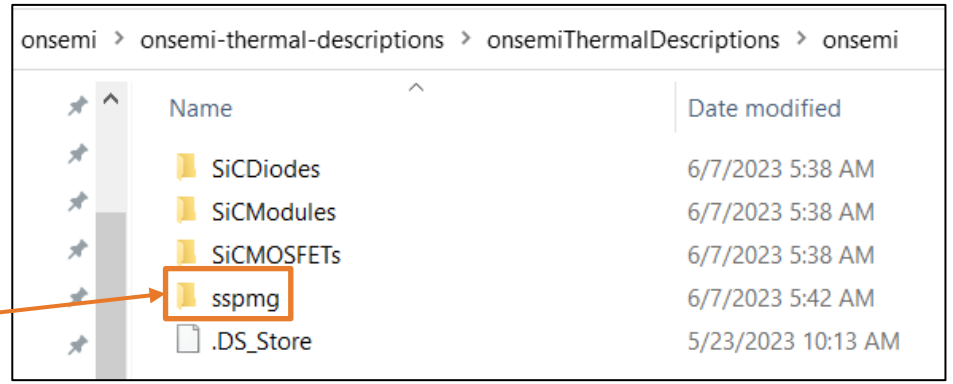


Previous Step

Load SSPMG models into PLECS Stand Alone

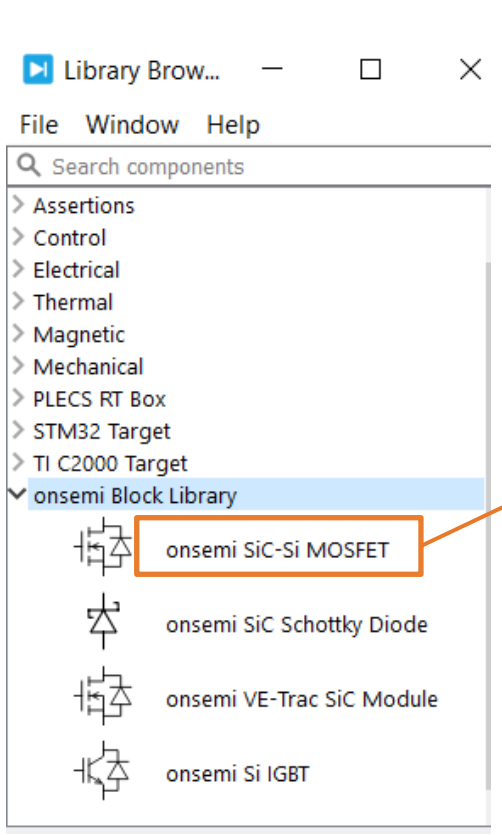
- First download PLECS models from Elite Power Simulator and follow instructions in “Install.txt” file.
  - *To install the onsemi SiC library components and corresponding thermal descriptions (XML files), simply add this directory (containing the "onsemiThermalDescriptions/" folder, "onsemiComponentLibrary_public.plecs" PLECS model, and "info.xml" file) into the list of thermal description search paths in the Thermal tab of the PLECS Preferences window. Click the Refresh button on the left side of the list and click OK to load the onsemi files into PLECS. Then a new entry in the PLECS Library Browser should appear "onsemi Block Library" containing several components that can be dragged into your own circuit models and directly be used with the provided thermal descriptions.*
- Create subfolder sspmg here and place SSPMG XML files in this directory. Note folder can be any name.

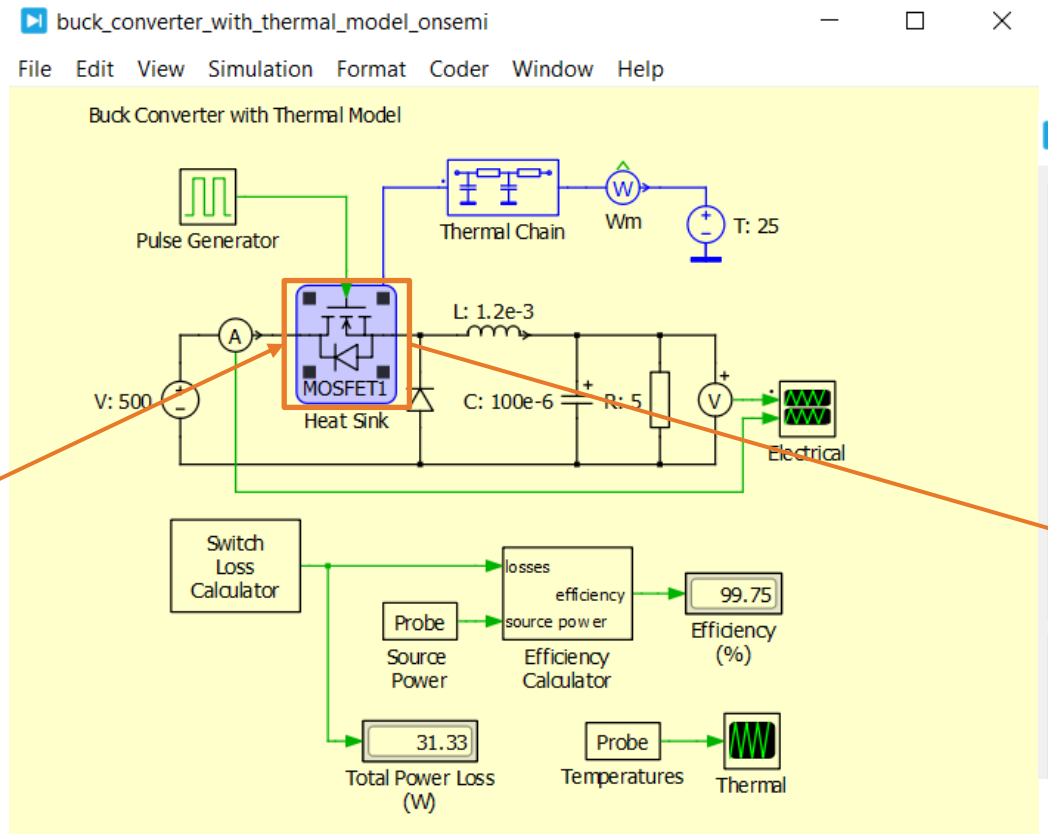


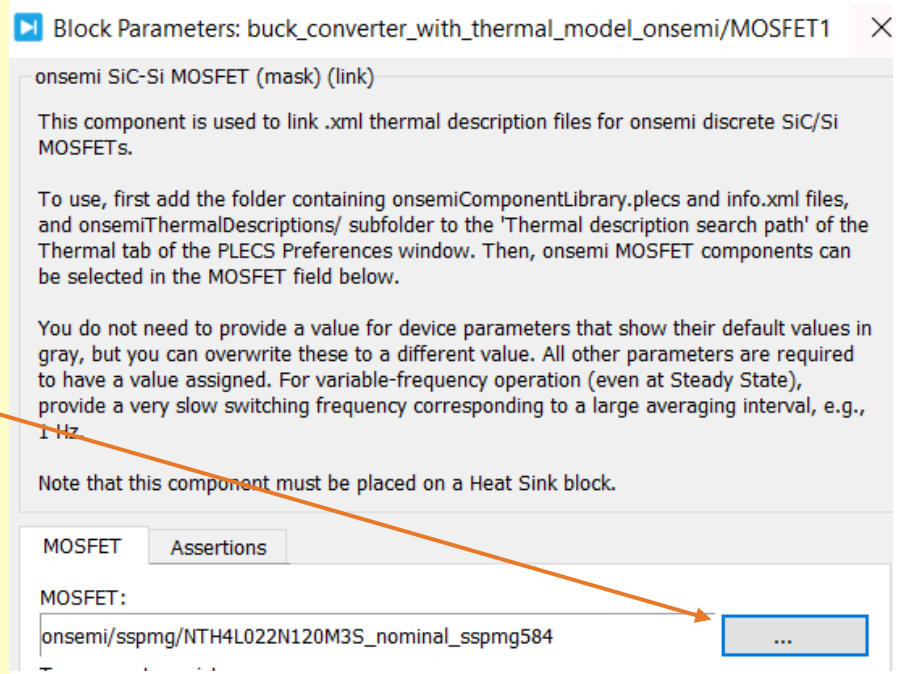


Load SSPMG models into PLECS Stand Alone

- Place an onsemi SiC-Si MOSFET or Si IGBT in PLECS schematic.
- Double click MOSFET/IGBT symbol and browse for SSPMG XML file.

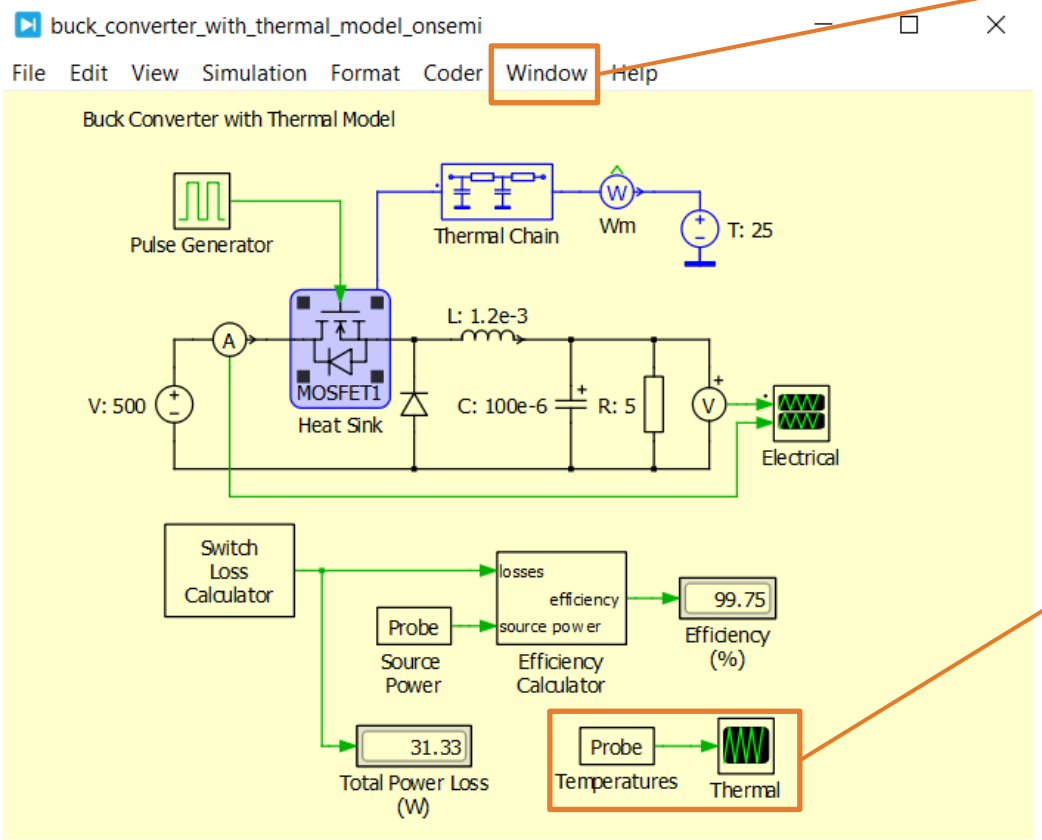


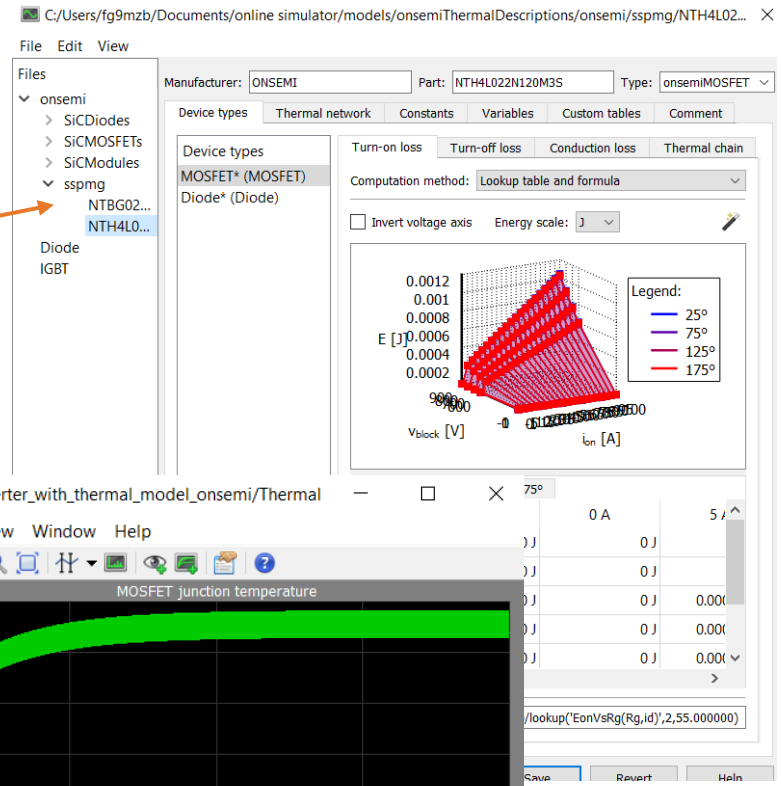


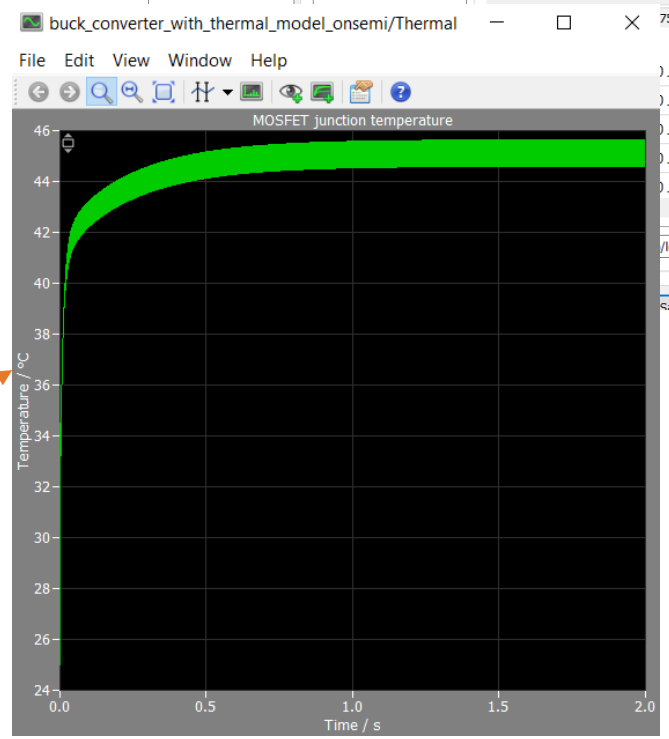


Load SSPMG models into PLECS Stand Alone

- Review XML data under Window →Thermal Library Browser
- Run simulation







Questions?

Have questions, comments, or need support with your Self-Service PLECS Model Generator needs? We're here to help! Write us an email at **sspmg@onsemi.com**.

- Self-Service PLECS Model Generator:

  www.onsemi.com/self-plecs-generator

- Elite Power Simulator:

  www.onsemi.com/elite-power-simulator

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