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Origins of SiC JFETs and Their Evolution Towards the Perfect Switch

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Abstract

Wide band−gap semiconductors as high−frequency switches are enablers for better efficiency in power conversion. One example, the silicon carbide switch can be implemented as a SiC MOSFET or in a cascode configuration as a SiC FET. This white paper traces the origins and evolution of the SiC FET to its latest generation and compares its performance with alternative technologies.

White Paper

The (near) perfect electrical switch has existed for a long time of course, but we are not talking about mechanics here. Modern power conversion depends on semiconductor switches that ideally have no resistance when on, infinite resistance and voltage withstand when off and ability to switch between the two states with a simple drive, arbitrarily fast, and with no momentary power dissipation.

In our energy− and cost−conscious world these features are enablers for high power conversion efficiency in power supplies, inverters, battery chargers, motor drives and more. Consequent benefits are reductions in equipment size, weight and failure rate, along with reduced acquisition and life−time costs. Sometimes a simple efficiency threshold is exceeded which opens up whole application areas. For example, EVs would be hardly viable if the motor drive were excessively lossy and consequently large and heavy, requiring in turn more battery power with yet further weight and range penalty. From the days of Shockley, Bardeen and Brattain nearly 75 years ago, engineers have therefore worked to improve semiconductor switches to get ever−closer to the ideal.

Progress Towards the Ideal Switch

Mechanical switches were indeed used in the first power conversion applications − mechanical ‘vibrators’ were initially the only alternative to motor−generator sets for isolated DC−DC conversion or DC voltage step−up. However, about ten years after the invention of the transistor, the first ‘switched−mode’ power supplies (SMPS) appeared and from that point, designers had to work with the semiconductor technology available. Although the principle of a field effect transistor (FET) had been proposed and patented in 1930 by Julius Edgar Lilienfeld[1], they were not practically manufacturable and it was the bipolar transistor, initially using germanium that dominated early SMPS circuits.

Bipolar transistors at first had limited voltage rating, high off−state leakage, slow and lossy switching and required complex base drive. To this day, power bipolar transistors have low gain and can require amps of base current. Stored charge in the base was a big problem, limiting turn−off times and efficiency, so techniques were used to tailor the base drive exactly and limit charge using techniques such as the ‘Baker clamp’ which traded some conduction loss for lower dynamic loss.

Silicon ‘metal oxide gate FETS’ or ‘MOSFET’s became viable for high power in the ‘70s and ‘80s with a vertical conduction path and planar gate structure, followed by a ‘trench’ arrangement in the ‘90s. Use at higher powers was limited however by the voltage rating and on−resistance achievable. A major development was the insulated gate bipolar transistor (IGBT) in the late ‘70s, which combined a MOSFET−like gate drive with a bipolar−like conduction path giving the benefits of easy drive and a fixed saturation voltage so that power dissipation nominally increased proportionally to current rather than current squared as in MOSFETs. IGBTs were not without their own problems however, with a tendency to latch on, with catastrophic results. ‘Tail current’ on switch−off also made dynamic losses relatively high, limiting operating frequency. The latch−up problem in modern IGBTs is now resolved and tail current minimized, while current and voltage ratings have increased dramatically, making the parts common in very high power conversion. Switching frequencies are still limited to a few tens of kHz maximum though, because of dynamic losses.

High switching frequencies are the key to smaller magnetics and overall smaller and lighter power conversion products with higher performance control loops, so as MOSFET on−resistance and voltage ratings have improved, they have been increasingly utilized, with frequencies pushed up to several hundreds of kHz, ‘super−junction’ types being the state of the art. A limiting factor however is the breakdown voltage of silicon, forcing a minimum thickness of bulk material for a given operating voltage and a consequently high value of on−resistance (R_{DS}). Many cells can be paralleled to reduce this, but then total die area (A) increases. The effect is quantified by the ‘figure of merit’ on−resistance per unit area or R_{DSA} and has prompted the surge in interest in wide band−gap materials silicon carbide (SiC) and gallium nitride (GaN), which have higher intrinsic breakdown voltage and other favorable characteristics such as higher electron mobility and saturation velocity, high temperature capability and for SiC, better thermal conductivity. Figure 1 shows a comparison of the headline characteristics of silicon, SiC and GaN materials.

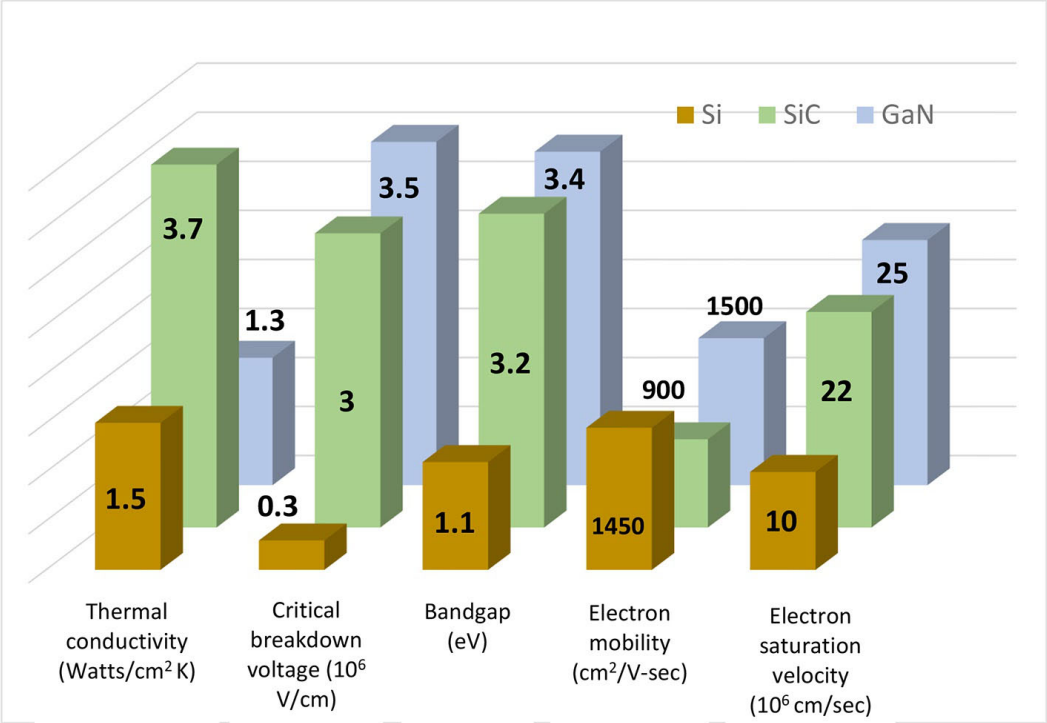

Figure 1. Si, SiC and GaN Material Characteristics

Early SiC Device Developments

Development of SiC devices started a decade before GaN with an expected initial wider applicability to higher voltages and power rating. A natural starting point for a SiC switch was to consider development of enhancement−mode, normally−off MOSFETs, for compatibility with existing Si MOSFET designs and fabrication techniques. As with any new technology, there were teething problems, some that were predicted, but others that were not and which caused delays to the commercialization of the parts.

An inherent characteristic of SiC was, and still is, the greater number of lattice defects compared with silicon and this causes low electron mobility at the gate−oxide interface with the SiC channel, leading to relatively high on−resistance. For cost effectiveness, SiC wafer size has to be maximized and it is difficult to maintain low defect rate and wafer flatness at the six−inch industry standard. SiC MOSFETs also exhibit gate threshold instability with significant hysteresis, making gate drive difficult to design for optimum efficiency and reliability. Although latest SiC MOSFETs are better, and in theory could use a unipolar 0−15 V drive, in practice, a negative gate voltage of −5 V is often used for reliable operation. 15 V also does not give the lowest on−resistance so 18 V is often used for best efficiency but at the cost of reduced short−circuit withstand capability and a decreased margin to the typical absolute maximum of 19 or 20 V. Other issues addressed were degradation of the gate oxide after short circuit and overvoltage events and excessive electric field stress in the gate oxide due to high drain−gate field intensity in the device blocking state.

An unpredicted difficulty with SiC MOSFETs was encountered around 2010 with ‘basal plane dislocations’ – bulk defects in the lattice, which actually grew and migrated during operating stress. With the body diode from source to drain conducting, electron–hole carriers are generated, which, when they recombine, have enough energy to move and enlarge the defects. This is a result of the higher band–gap energy value of SiC and the consequence can be degradation – higher leakage current and on–resistance, in turn leading to higher losses and failure. SiC MOSFETs today have improved considerably with advances in fabrication methods and with defect screening but efforts are ongoing to improve yield and cost effectiveness of the die and performance of the packaging, for low inductance and thermal resistance.

The SiC FET – An Alternative Approach

With the arrival of wide band–gap technology, while many semiconductor manufacturers took the route of development of SiC MOSFETs using existing fabrication lines, others started with a ‘blank sheet’ and considered other options. The simplest switch implemented with SiC is the JFET structure which has no gate oxide and is a unipolar conduction device, so does not show some of the MOSFET limitations. The device has a major drawback though – it is ‘normally on’ with gate drive at zero volts and requires a negative drive to turn off. This is at best inconvenient and at worst risks application failure, especially under transient conditions such as system turn on/off. Originally proposed in the 90s, a device was developed around 2010which solved the problem – the SiC FET – a combination of a SiC JFET and a Silicon MOSFET which is normally off, but which maintains the advantages of a JFET over a MOSFET. Figure 2 shows the SiC FET arrangement (right) compared with a generic SiC MOSFET schematic (left).

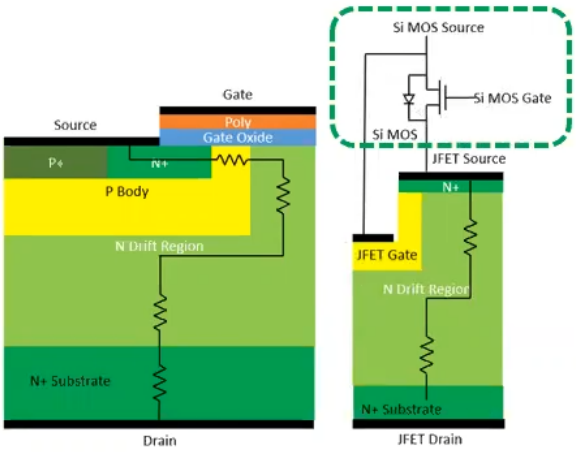

Figure 2. SiC MOSFET (left) and (right) SiC FET Construction

The arrangement of the SiC FET is a cascode, perhaps familiar to more mature engineers who may have even seen it implemented in its original form as a combination of vacuum tubes, intended to reduce noise in audio amplifiers. The cascode or ‘emitter switch’ has appeared in different guises over the years, with combinations of bipolar transistors or a BJT and a MOSFET, with the general attribute that a low voltage switch controls a high voltage one with a good

compromise between high voltage rating and easy drive. Circuits with BJTs were not popular at high power however, due to the significant base drive current necessary and slow switching speed. The SiC cascode or ‘SiC FET’ solves these problems.

Referring to the SiC FET schematic shown in Figure 3**,** when the Si−MOSFET is turned on via its gate, the JFET source and gate are effectively shorted and the JFET conducts. Current can now pass through the JFET and MOSFET drain−source channels with the conduction loss fixed by the JFET, because the low−voltage Si−MOSFET on−resistance can be extremely low compared with that of the high−voltage SiC JFET. When the Si−MOSFET is off, the JFET source voltage rises to the point where its gate−source threshold of a few volts negative is exceeded and the JFET turns off. Because of the ratio of device capacitances, dynamically, the voltage across the Si−MOSFET remains low.

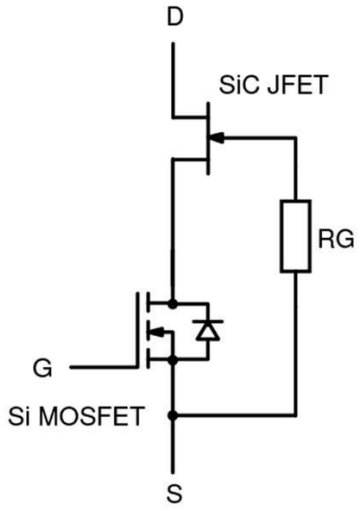

Figure 3. The SiC FET Schematic

There are many advantages to the SiC FET over a SiC MOSFET, both in electrical performance and in practical use. As a switch, on−resistance is a major factor and the SiC JFET inherently has much better electron mobility in the channel than a SiC MOSFET. The channel density is also higher and the combination means that for a given die area, SiC FET on−resistance is 2−4x less or conversely, up to four times the number of die can be obtained per wafer than with a SiC MOSFET for the same on−resistance. Compared with a silicon superjunction MOSFET, the increased die count can be up to 13x. This increase in dross die per wafer is critical to the success of the SiC FET technology given that silicon carbide as a material is likely always to be more expensive than silicon. As discussed, a measure of the viability of a die is the figure of merit R_{DSA}.

Another figure of merit given in Table 1 is $R_{DS}*E_{OSS}$ or the trade−off between on−resistance and device output switching energy, derived from output capacitance. This is a useful measure as it is possible to reduce on−resistance and conduction losses by simply paralleling more cells in the die, but as well as increasing area, this also directly increases capacitance and

consequently E_{OSS}, which results in increased frequency−dependent switching losses. A low value for R_{DS}*E_{OSS} is therefore advantageous.

The gate of the SiC FET is simply that of the cascoded Si MOSFET. It has a stable, essentially hysteresis−free threshold of around 5 V and is therefore easy to drive with 12 V or 15 V for full enhancement and low R_{DSON}, with a large margin to the absolute maximum of typically 25 V. The easy SiC FET gate drive is nominally compatible with silicon MOSFET and even IGBT levels, giving potential backwards−compatibility for existing product design upgrades. SiC MOSFETs and certainly GaN HEMT cells in practice require custom drive arrangements for optimum efficiency and sufficient protection against overvoltage on the gates.

SiC FETs exhibit virtually no gate−drain or 'Miller' capacitance C_{rss}, due to the small device dimensions and isolating effect of the Si MOSFET in the cascode arrangement, enabling ultra−fast switching. Output capacitance, $C_{OSS,}$ along with associated switching energy E_{OSS} is low, as noted in Table 1, also leading to fast switching with minimal loss. Edge rates are so fast that in practical circuits, the SiC FET has to be slowed down to limit voltage overshoots and EMI. This can be done with added gate resistors but can lead to unacceptable control delays at high switching frequency, so simple RC snubbers are often a better solution. With the capacitor typically set at around 3 x C_{OSS}, dissipation in the series resistor is minimal. Figure 4 shows typical SiC FET device capacitances and their variation with drain voltage in the blocking state. C_{iss} = C_{GS} + C_{GD}, (C_{DS} shorted), C_{rss} = C_{GD}, Coss = C_{DS} + C_{GD}.

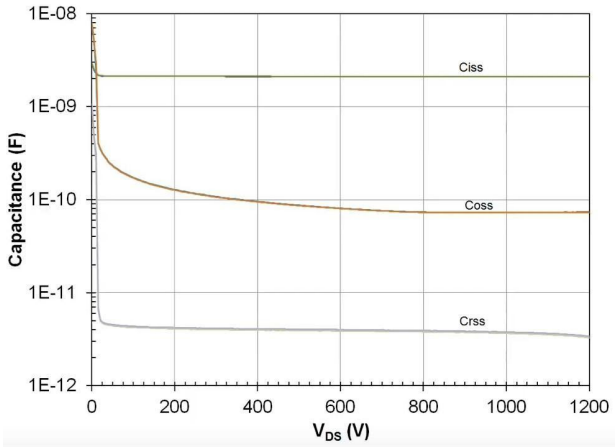

Figure 4. SiC FET Device Capacitances

The SiC FET 'Body Diode'

In power converters, the perfect switch should conduct in both directions with low losses. This is actually required in circuits such as AC motor drives and converters with inductive loads, so−called 'third quadrant' operation. IGBTs cannot do this and require a parallel diode, but MOSFETs and JFETs in silicon and SiC can conduct in either direction through their channel under the control of the gate. MOSFETs also have an inherent body diode which is absent in JFETs and this body diode conducts automatically by 'commutation' in hard switched converters

with inductive loads in the ‘dead time’ before the device channel is switched on through the gate, to allow reverse current flow. This conduction stores charge Q_{rr}, which is recovered when the body diode is subsequently reverse biased and this action dissipates significant peak power which averages to a higher and higher value as frequency increases, reducing efficiency. With Silicon MOSFETs, the effect can be so severe that practically they cannot be used in some circuits such as the popular totem−pole PFC stage, operating in continuous conduction mode (CCM). SiC MOSFETs have a Q_{rr} value which is perhaps 10x better than Si but the SiC FET is better still, due to the lower output capacitance of the device and minimal stored charge in the low voltage MOSFET. Comparisons do depend on the voltage class of device but Figure 5 shows typical reverse recovery plots of a SiC FET and an otherwise similar silicon superjunction MOSFET.

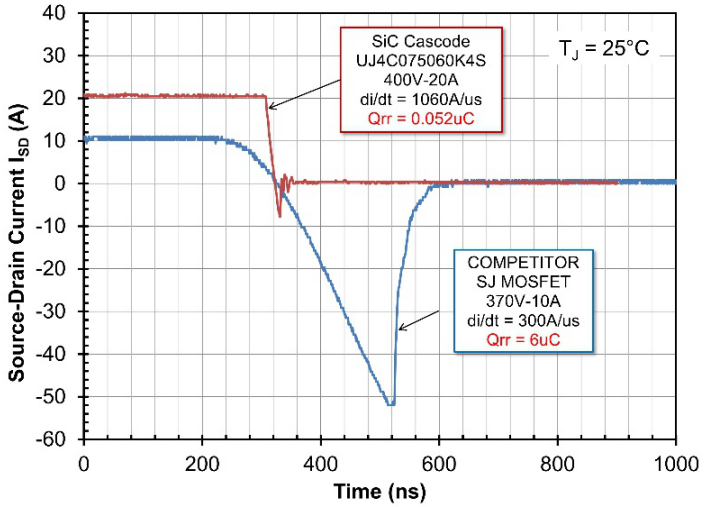

Figure 5. SiC FET Cascodes have around 100x Smaller Reverse Recovery Charge than Silicon SJ MOSFETs

While SiC MOSFETs and GaN devices may have adequately low or no reverse recovery losses, the voltage drop with reverse conduction is a different story. This can produce significant loss during dead time in power converters. Si superjunction MOSFETs exhibit a diode drop which is typically around 1 V and SiC MOSFETs are much worse with a body diode than can easily drop 4 V. GaN HEMT cells in third quadrant operation drop a voltage V_{sd} which is the sum of the I*R channel voltage and gate threshold voltage less gate source voltage, or:

$V_{sd} = (V_{th}−V_{gs})+(I_{sd}*R_{on})$

The gate threshold for GaN is typically 1.5 V so at high currents, the total drop can be high. If the gate is driven negative to turn off, which is common, this voltage V_{gs} adds to the source−drain drop, resulting in a V_{sd} of several volts, which can be significantly worse than other technologies. The SiC FET, when conducting source to drain, has an I*R drop from the channel resistance similar to the GaN device but this is only increased by the voltage across the body diode of the low voltage cascoded Si MOSFET, which is relatively low. The resulting forward voltage drop is typically around 1.5V, better than the SiC MOSFET or GaN performance.

Proving the Reliability of the SiC FET

Wide band−gap switches are robust, not least because of their inherent high temperature and high breakdown voltage capability and a particular advantage of the SiC FET is the absence of a SiC gate oxide as is present in SiC MOSFETs, with their problems of degradation from high E−fields. The Si−MOSFET in the cascode is a robust low voltage type with a high threshold voltage and thick gate oxide layer, additionally protected by built−in zener clamps. In practice, SiC FETs have shown themselves to be extremely reliable, with parts now routinely achieving automotive AEC−Q ratings. An important consideration is also reliability during unintended stress events such as over−voltage and short circuit. SiC FETs have a robust avalanche capability which is activated by the JFET drain−gate breaking over. The resulting current through Rg in Figure 3 drops voltage, turning the JFET on and clamping the over−voltage. The Si MOSFET does now avalanche but in a highly controlled way, as avalanche protection diodes are included in the fabrication of each cell and little power is dissipated. SiC MOSFETs also have an avalanche rating but GaN HEMT cells do not, forcing manufacturers to rate the parts at lower voltages to achieve adequate margin between operating and destructive breakdown voltage.

The SiC FET also has a benign short circuit current characteristic; at high currents, the voltage drop gradient across the channel causes a natural ‘pinch−off’ effect to limit current. Short circuit current is independent of gate voltage, unlike with MOSFETs and IGBTs and the on−resistance positive temperature coefficient of the SiC FET channel also helps to reduce the limiting current and spread the stress across the individual cells in the die. The effect is so consistent that SiC FETs can be used as accurate current limit devices in linear circuits. A typical test in automotive applications is for the device to withstand a short circuit for at least 5 μs and Figure 6 shows a 750 V SiC FET withstanding the stress for 8 μs with no degradation. Figure 7 shows the effect of on−resistance increasing with temperature, reducing short circuit current to an end−value largely independent of initial junction temperature with a 1200 V rated SiC FET.

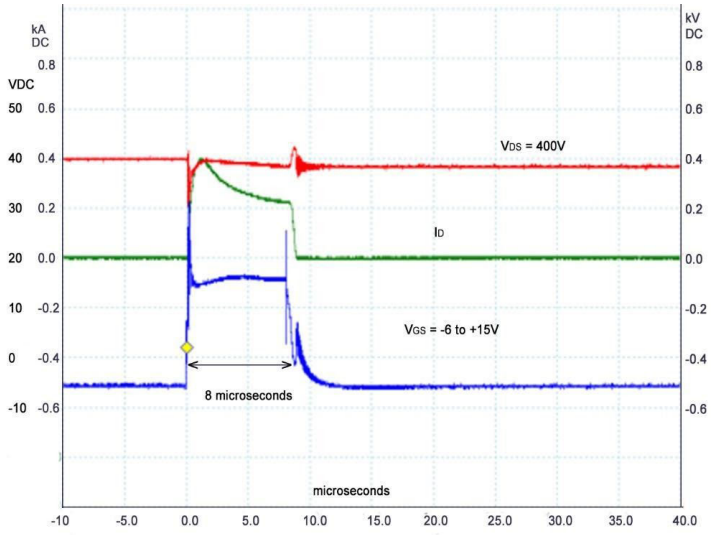

Figure 6. SiC FETs withstand an 8 μs Short Circuit Stress from a 400 Vbus

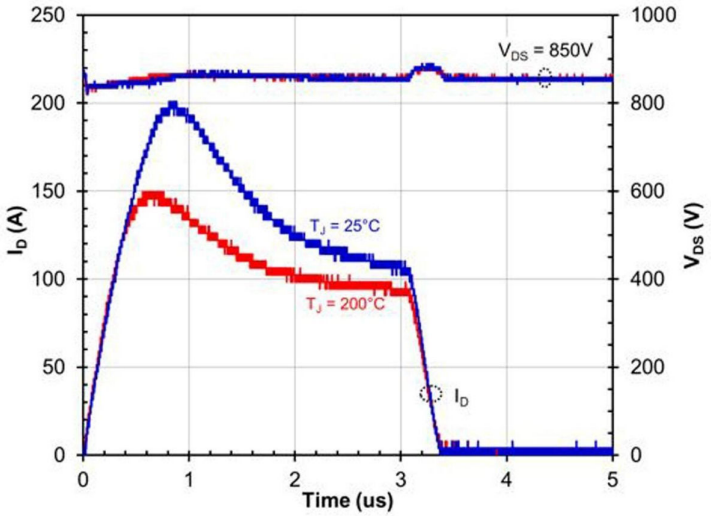

Figure 7. SiC FET Short Circuit Current is Independent of Initial Junction Temperature

To maintain reliability, temperature rise and gradients in a packaged SiC FET should be minimized and the thermal conductivity of SiC at more than 3x better than silicon or GaN is an advantage here. Latest devices also use silver sintering rather than soldering for the die attach, which yields a 6x improvement in thermal conductivity of the interface, keeping junction temperature rise low and reliability high.

Other SiC FET Applications

SiC FETs are finding a natural home in high efficiency power converters and are available up to 1700 V rating for typical industrial three−phase applications. The cascode principle can be easily expanded however by ‘stacking’ SiC JFETs on a controlling Si MOSFET (Figure 8). Modules demonstrating the principle have been developed with 40 kV rating[3].

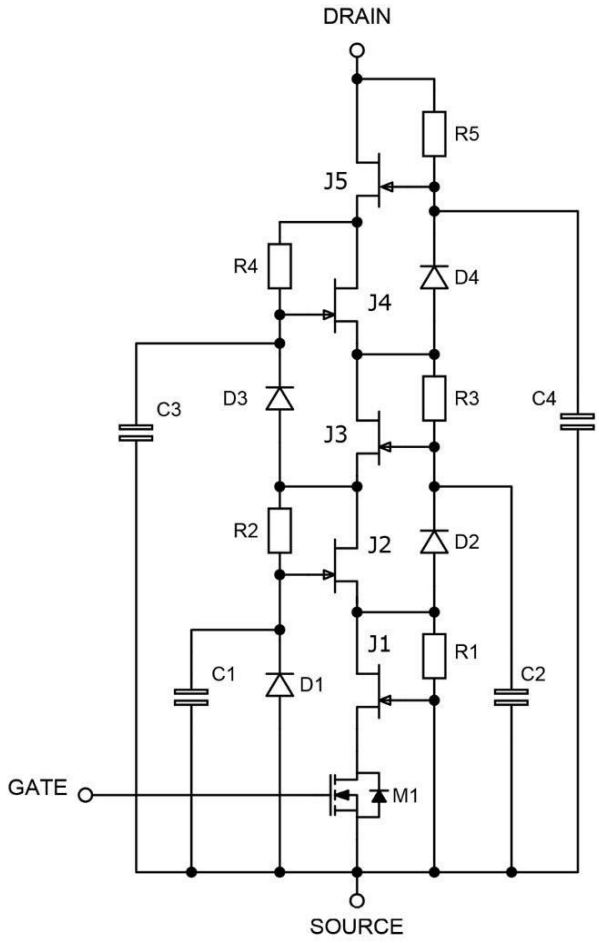

Figure 8. Stacked Cascodes Principle can be used at High Voltage to tens of kV Rating

As mentioned, SiC JFETs have a near−constant saturation current characteristic with gate−source and drain voltage and this can be used to advantage in circuit protection applications such as current limiters or breakers. Figure 9 shows a self−biasing circuit breaker concept using SiC FET cascodes that is truly ‘two−terminal’ with no external auxiliary power rails or internal DC−DC converters.

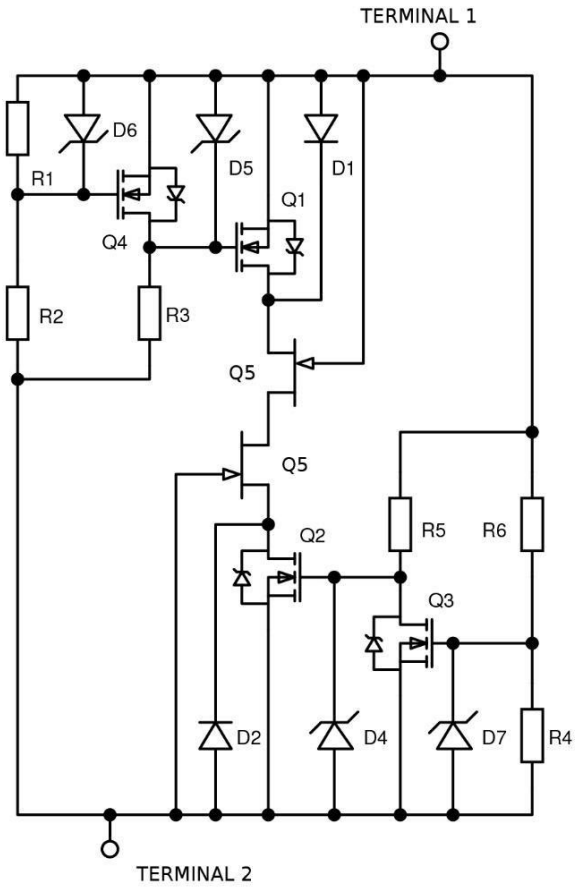

Figure 9. Two−terminal Self−biasing Circuit Breaker Concept

Progress Towards Enhanced Performance and Value

SiC FETs have progressed through technology generations, ‘GEN4’ being the latest with a slew of improvements including voltage range available, cell density for better on−resistance, and sintered die attach for improved thermal performance. ‘Substrate thinning’ techniques are now used, as the channel resistance is so low that conduction loss through the substrate itself becomes a limiting factor. Dynamically, parts have also improved, particularly with a reduction in output capacitance C_{OSS}. This decreases losses in hard−switched topologies such as the totem−pole PFC in continuous conduction mode and enables higher frequency operation in soft−switched resonant circuits such as the LLC or PSFB. Switching edge rates are now so fast that devices are offered with ‘ultra−fast’ and deliberately slowed, merely ‘fast’ ratings, to suit applications where edge rates are not critical to performance and could cause EMI and breakdown problems such as in motor drives.

Packaging has also advanced from first SiC FETs, formed by a side−by−side arrangement of the Si MOSFET and SiC FET die with interconnecting wire bonds. This enables flexibility in the TO−247 package for example, but for lower cost and better performance, ‘stacked’ die arrangements are now common for high current with larger die, especially when paralleling parts in a compact module. Solder die attach has given way to silver sintering for better thermal

performance and a DFN8x8 package enables low inductance high−frequency layout for MHz switching. TO−220, TO−247 and D2PAK packages are still popular as they can allow retrofitting of SiC FETs into older designs, even those using IGBTs. Four−lead versions of these packages with a ‘Kelvin’ source connection alleviate problems caused by source lead inductance interfering with the gate drive loop.

Alongside all this, the increasing value of using SiC FETs from their electrical performance is complemented by a cost reduction program from ongoing improvements to production yield and progress towards 8−inch wafers.

SiC FETs are a Compelling Solution

The ideal switch is now a little closer with the latest generation of SiC FETs. Conduction and dynamic losses are the lowest ever, enabling high−frequency power conversion stages with 99%+ efficiency with the corresponding energy, size and weight savings that follow on. Designers have a wider definition of ‘ideal’ − they also want the part to be easy to drive in a convenient package, with stable characteristics, over a wide range of operating and fault conditions. At the same time, equipment end−users want reliable end products with a total lifetime−cost that is a step improvement from older technology implementations. SiC FETs from United Silicon Carbide enable this with a range of parts with voltage ratings from 650 V to 1700 V and with on−resistances down to 7 milliohms. As a design aid, the UnitedSiC ‘FET JET’ calculator[4] allows rapid selection and performance prediction of any of their devices in a selection of power conversion topologies including PFC stages and isolated/non−isolated DC−DC converters.

References

[1] https://en.wikipedia.org/wiki/Julius_Edgar_Lilienfeld

[2] 'Trends in SiC MOSFET Threshold Voltage and ON−Resistance Measurements from Thermal Cycling and Electrical Switching Stresses' Josef P Kozak et. al. https://www.nrel.gov/docs/fy18osti/70550.pdf

[3] 'A brief history of supercascodes' https://unitedsic.com/a−brief−history−of−supercascodes/

[4] https://info.unitedsic.com/fet−jet

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