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|--------------------------------|---|
| Title of Change: | AR0144AT Datasheet Update |
| Effective date: | 03 Feb 2021 |
| Contact information: | Contact your local ON Semiconductor Sales Office or Andrew.Ko@onsemi.com |
| Type of notification: | This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin. |
| Change Category: | Documentation Change |
| Change Sub-Category(s): | Datasheet/Product Doc change |

Sites Affected:

| ON Semiconductor Sites | External Foundry/Subcon Sites |
|------------------------|-------------------------------|
| None | None |

Description and Purpose:

Updated AR0144AT datasheet to correct errors. There is no product or design change.

- Updated Table 2, "Available Part Numbers" with new OPNS

Old Table 2**ORDERING INFORMATION****Table 2. AVAILABLE PART NUMBERS**

| Part Number | Product Description | Orderable Product Attribute Description |
|-------------------------|---------------------|--|
| AR0144ATSM20XUEA0-DPBR | Mono, iBGA | Mono, iBGA, CRA = 20°, Dry pack with PF, Double Sided BBAR Glass |
| AR0144ATSM20XUEA0-DRBR | Mono, iBGA | Mono, iBGA, CRA = 20°, Dry pack without PF, Double Sided BBAR Glass |
| AR0144ATSM20XUEA0-TPBR | Mono, iBGA | Mono, iBGA, CRA = 20°, Tape & Reel with PF, Double Sided BBAR Glass |
| AR0144ATSM20XUEA0-TRBR | Mono, iBGA | Mono, iBGA, CRA = 20°, Tape & Reel without PF, Double Sided BBAR Glass |
| AR0144ATSM20XUEAD3-GEVK | Mono, iBGA | Mono, Demo kit |
| MARS1-AR0144ATSM-GEVB | Mono, iBGA | MARS Parallel board |
| MARS1-AR0144ATSMS-GEVB | Mono, iBGA | MARS MIPI board |
| GAZET1-AR0144ATSM-GEVK | Mono, iBGA | GazeT Driver Monitoring System kit |

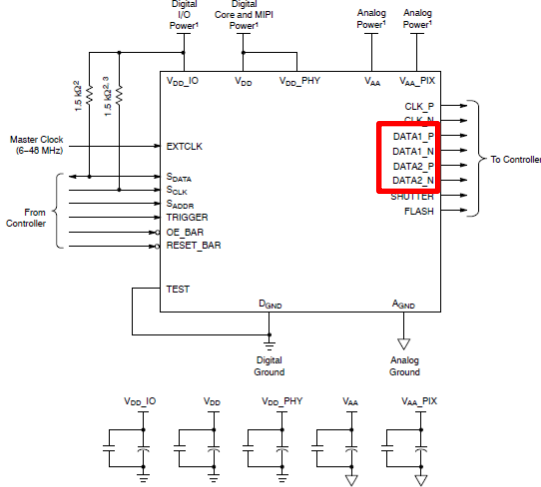
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| AR0144ATSM20XUEA0-TPBR | Mono, iBGA | Mono, iBGA, CRA = 20°, Tape & Reel with PF, Double Sided BBAR Glass |
| AR0144ATSM20XUEA0-TRBR | Mono, iBGA | Mono, iBGA, CRA = 20°, Tape & Reel without PF, Double Sided BBAR Glass |
| AR0144ATSM20XUD20 | Mono, Bare Die | Mono, CRA = 20 deg |
| AR0144ATSM20XUEAD3-GEVK | Mono, iBGA | Mono, Demo kit |
| AR0144ATSM20XUEAH3-GEVB | Mono, iBGA | Mono, Headboard |
| MARS1-AR0144ATSM-GEVB | Mono, iBGA | MARS Parallel board |
| MARS1-AR0144ATSMS-GEVB | Mono, iBGA | MARS MIPI board |
| GAZET1-AR0144ATSM-GEVK | Mono, iBGA | GazeT Driver Monitoring System kit |



2. Updated Figure 4, "Serial 2-Lane MIPI Interface"

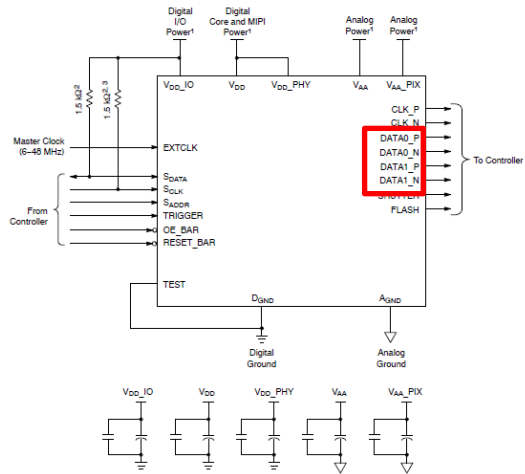
Old Figure 4



- Notes:
1. All power supplies must be adequately decoupled.
 2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
 3. This pull-up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
 4. The parallel interface output pads can be left unconnected if the serial output interface is used.
 5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0144AT demo headboard schematics for circuit recommendations.
 6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

Figure 4. Serial 2-lane MIPI Interface

New Figure 4

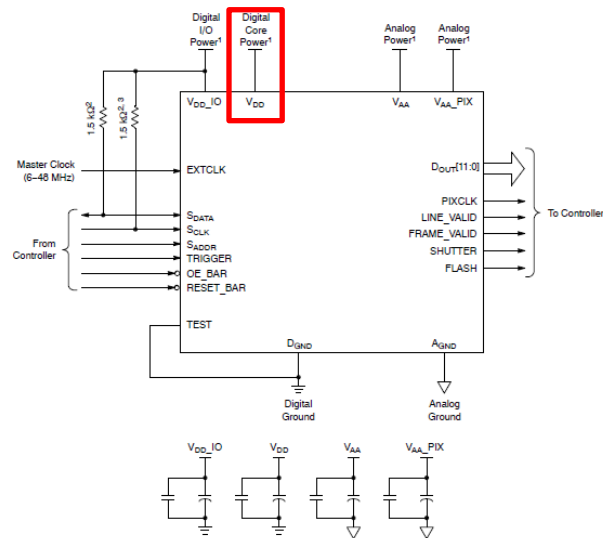


- Notes:
1. All power supplies must be adequately decoupled.
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 6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

Figure 4. Serial 2-lane MIPI Interface

3. Updated Figure 5, "Parallel Pixel Data Interface"

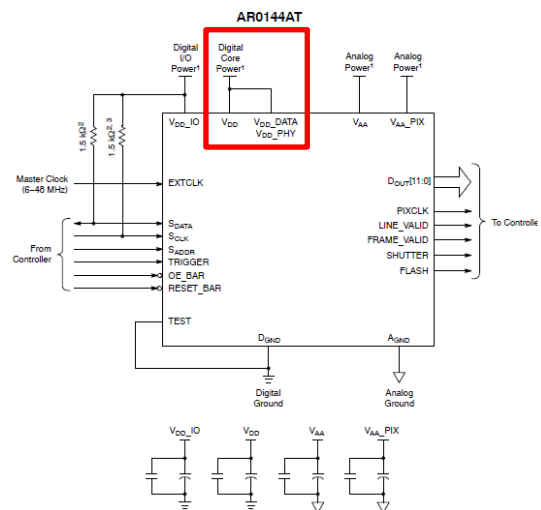
Old Figure 5



- Notes:
1. All power supplies must be adequately decoupled.
 2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
 3. This pull-up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
 4. The serial interface output pads can be left unconnected if the parallel output interface is used.
 5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0144AT demo headboard schematics for circuit recommendations.
 6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

Figure 5. Parallel Pixel Data Interface

New Figure 5



- Notes:
1. All power supplies must be adequately decoupled.
 2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
 3. This pull-up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
 4. The serial interface output pads can be left unconnected if the parallel output interface is used.
 5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0144AT demo headboard schematics for circuit recommendations.
 6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

Figure 5. Parallel Pixel Data Interface



4. Updated Table 3, "Pin Descriptions, 63 Ball iBGA Package"

Old Table 3

Table 3. PIN DESCRIPTIONS – 63-BALL iBGA PACKAGE (continued)

| Name | CSP Ball | Type | Description |
|---------------------|----------|-------|--|
| EXTCLK | B3 | Input | External input clock |
| V _{DD_PHY} | C5 | Power | MIPI power (may leave unconnected if parallel interface is used) |

New Table 3

Table 3. PIN DESCRIPTIONS – 63-BALL iBGA PACKAGE (continued)

| Name | iBGA Ball | Type | Description |
|---------------------|-----------|-------|----------------------|
| EXTCLK | B3 | Input | External input clock |
| V _{DD_PHY} | C5 | Power | MIPI power |

5. Removed reference to slave mode in "Features" and "Features Overview" section.

6. Updated Table 12, "DC Electrical Characteristics"

Old Table 12

Table 12. DC ELECTRICAL CHARACTERISTICS

| Symbol | Definition | Condition | Min | Typ | Max | Unit |
|---------------------|-----------------------|---|--------------------------|---------|--------------------------|------|
| V _{DD} | Core Digital Voltage | | 1.14 | 1.2 | 1.26 | V |
| V _{DD_IO} | I/O Digital Voltage | | 1.7/2.5 | 1.8/2.8 | 1.9/3.1 | V |
| V _{AA} | Analog Voltage | | 2.5 | 2.8 | 3.1 | V |
| V _{AA_PIX} | Pixel Supply Voltage | | 2.5 | 2.8 | 3.1 | V |
| V _{DD_PHY} | MIPI Supply Voltage | | 1.14 | 1.2 | 1.26 | V |
| V _{IH} | Input HIGH Voltage | | V _{DD_IO} * 0.7 | – | – | V |
| V _{IL} | Input LOW Voltage | | – | – | V _{DD_IO} * 0.3 | V |
| I _{IN} | Input Leakage Current | No Pull-up Resistor; V _{IN} = V _{DD_IO} or D _{IGND} | 20 | – | – | μA |
| V _{OH} | Output HIGH Voltage | | V _{DD_IO} * 0.7 | – | – | V |
| V _{OL} | Output LOW Voltage | V _{DD_IO} = 2.8 V | – | – | V _{DD_IO} * 0.3 | V |
| I _{OH} | Output HIGH Current | At Specified V _{OH} | –12 | – | – | mA |
| I _{OL} | Output LOW Current | At Specified V _{OL} | – | – | 12 | mA |

CAUTION: Stresses greater than those listed in Table 13 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.



New Table 12

Table 12. DC ELECTRICAL CHARACTERISTICS

| Symbol | Definition | Condition | Min | Typ | Max | Unit |
|---------------------|-----------------------|--|--------------------------|---------|--------------------------|------|
| V _{DD} | Core Digital Voltage | | 1.14 | 1.2 | 1.26 | V |
| V _{DD_IO} | I/O Digital Voltage | | 1.7/2.5 | 1.8/2.6 | 1.9/3.1 | V |
| V _{AA} | Analog Voltage | | 2.5 | 2.6 | 3.1 | V |
| V _{AA_PIX} | Pixel Supply Voltage | | 2.5 | 2.6 | 3.1 | V |
| V _{DD_PHY} | MIPI Supply Voltage | | 1.14 | 1.2 | 1.26 | V |
| V _{IH} | Input HIGH Voltage | | V _{DD_IO} + 0.7 | - | - | V |
| V _{IL} | Input LOW Voltage | | - | - | V _{DD_IO} + 0.3 | V |
| I _{IN} | Input Leakage Current | No Pull-up Resistor; V _{IN} = V _{DD_IO} or D _{GNP} | - | - | 20 | μA |
| V _{OH} | Output HIGH Voltage | | V _{DD_IO} - 0.3 | - | - | V |
| V _{OL} | Output LOW Voltage | V _{DD_IO} = 2.6 V | - | - | 0.4 | V |
| I _{OH} | Output HIGH Current | At Specified V _{OH} | -12 (Note 16) | - | - | mA |
| I _{OL} | Output LOW Current | At Specified V _{OL} | - | - | 12 (Note 16) | mA |

16. A slow rate setting of 7 is needed to achieve IOH and IOL minimum and maximum specifications

CAUTION: Stresses greater than those listed in Table 13 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied

List of Affected Standard Parts:

Note: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the [PCN Customized Portal](#).

| | | |
|------------------------|------------------------|------------------------|
| AR0144ATSM20XUEA0-DPBR | AR0144ATSM20XUEA0-DRBR | AR0144ATSM20XUEA0-TPBR |
| AR0144ATSM20XUEA0-TRBR | AR0144ATSM20XUD20 | |