MMDF2C03HD

Power MOSFET
2 Amps, 30 Volts
Complementary SO−8, Dual

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain-to-source diode has a very low reverse recovery time. These devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc-dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

Features

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive − Can Be Driven by Logic ICs
- Miniature SO-8 Surface Mount Package − Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO-8 Package Provided
- This is a Pb−Free Device

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) (Note 1)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	30	Vdc
Gate−to−Source Voltage	V_{GS}	± 20	Vdc
Drain Current − Continuous N−Channel P−Channel − Pulsed N−Channel P−Channel	I_D I_{DM}	4.1 3.0 21 15	A
Operating and Storage Temperature Range	T_J, T_{stg}	− 55 to 150	°C
Total Power Dissipation @ T_A= 25°C (Note 2)	P_D	2.0	W
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	62.5	°C/W
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 30 V, V_{GS} = 5.0 V, Peak I_L = 9.0 Apk, L = 8.0 mH, R_G = 25 Ω) N−Channel (V_{DD} = 30 V, V_{GS} = 5.0 V, Peak I_L = 6.0 Apk, L = 18 mH, R_G = 25 Ω) P−Channel	E_{AS}	 324 324	mJ
Max Lead Temperature for Soldering, 0.0625″ from case. Time in Solder Bath is 10 seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

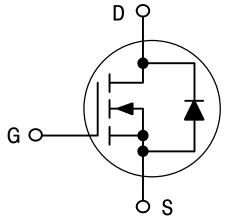
1. Negative signs for P−Channel device omitted for clarity.
2. Mounted on 2” square FR4 board (1” sq. 2 oz. Cu 0.06” thick single sided) with one die operating, 10 sec. max.

ON Semiconductor®

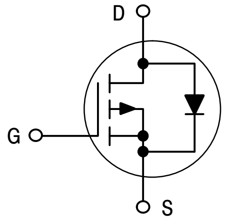
http://onsemi.com

2 AMPERES, 30 VOLTS
$R_{DS(on)}$ = 70 mΩ (N-Channel)
$R_{DS(on)}$ = 200 mΩ (P-Channel)

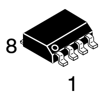
N−Channel



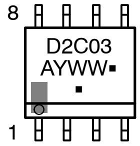
P−Channel



MARKING DIAGRAM



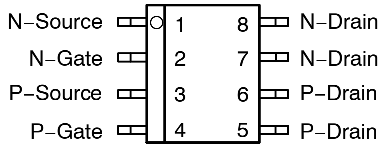
SO−8
CASE 751
STYLE 14



D2C03	= Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
MMDF2C03HDR2G	SO−8 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Note 3)

Characteristic		Symbol	Polarity	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	–	30	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	(N) (P)	– –	– –	1.0 1.0	μAdc
Gate−Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	–	–	–	100	nAdc
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	(N) (P)	1.0 1.0	1.7 1.5	3.0 2.0	Vdc
Drain−to−Source On−Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc) (V_{GS} = 10 Vdc, I_D = 2.0 Adc)		$R_{DS(on)}$	(N) (P)	– –	0.06 0.17	0.070 0.200	Ω
Drain−to−Source On−Resistance (V_{GS} = 4.5 Vdc, I_D = 1.5 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	(N) (P)	– –	0.065 0.225	0.075 0.300	Ω
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.5 Adc) (V_{DS} = 3.0 Vdc, I_D = 1.0 Adc)		g_{FS}	(N) (P)	2.0 2.0	3.6 3.4	– –	mhos
DYNAMIC CHARACTERISTICS							
Input Capacitance	(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	(N) (P)	– –	450 397	630 550	pF
Output Capacitance		C_{oss}	(N) (P)	– –	160 189	225 250	
Transfer Capacitance		C_{rss}	(N) (P)	– –	35 64	70 126	
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	(V_{DD} = 15 Vdc, I_D = 3.0 Adc, V_{GS} = 4.5 Vdc, R_G = 9.1 Ω) (V_{DD} = 15 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	(N) (P)	– –	12 16	24 32	ns
Rise Time		t_r	(N) (P)	– –	65 18	130 36	
Turn−Off Delay Time		$t_{d(off)}$	(N) (P)	– –	16 63	32 126	
Fall Time		t_f	(N) (P)	– –	19 194	38 390	
Turn−On Delay Time	(V_{DD} = 15 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω) (V_{DD} = 15 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	(N) (P)	– –	8.0 9.0	16 18	
Rise Time		t_r	(N) (P)	– –	15 10	30 20	
Turn−Off Delay Time		$t_{d(off)}$	(N) (P)	– –	30 81	60 162	
Fall Time		t_f	(N) (P)	– –	23 192	46 384	
Total Gate Charge	(V_{DS} = 10 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc) (V_{DS} = 24 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	(N) (P)	– –	11.5 14.2	16 19	nC
Gate−Source Charge		Q_1	(N) (P)	– –	1.5 1.1	– –	
Gate−Drain Charge		Q_2	(N) (P)	– –	3.5 4.5	– –	
		Q_3	(N) (P)	– –	2.8 3.5	– –	

3. Negative signs for P−Channel device omitted for clarity.
4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

ELECTRICAL CHARACTERISTICS – continued (T_A = 25°C unless otherwise noted) (Note 6)

Characteristic		Symbol	Polarity	Min	Typ	Max	Unit
SOURCE–DRAIN DIODE CHARACTERISTICS (T_C = 25°C)							
Forward Voltage (Note 7)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	(N) (P)	– –	0.82 1.82	1.2 2.0	Vdc
Reverse Recovery Time	(I_F = I_S, dI_S/dt = 100 A/μs)	t_{rr}	(N) (P)	– –	24 42	– –	ns
		t_a	(N) (P)	– –	17 16	– –	
		t_b	(N) (P)	– –	7.0 26	– –	
Reverse Recovery Storage Charge		Q_{RR}	(N) (P)	– –	0.025 0.043	– –	μC

6. Negative signs for P–Channel device omitted for clarity.
7. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

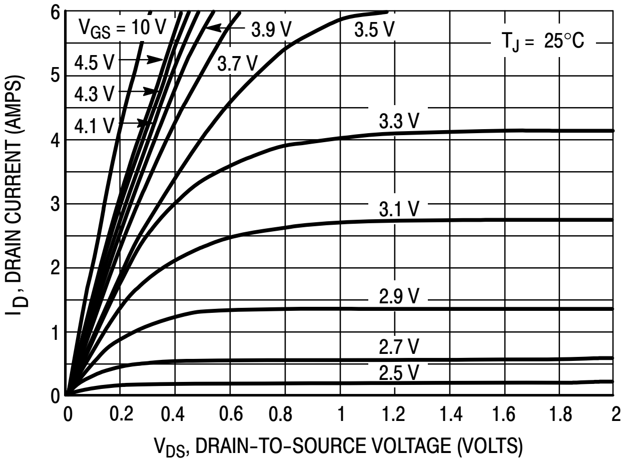


Figure 1. On–Region Characteristics

P–Channel

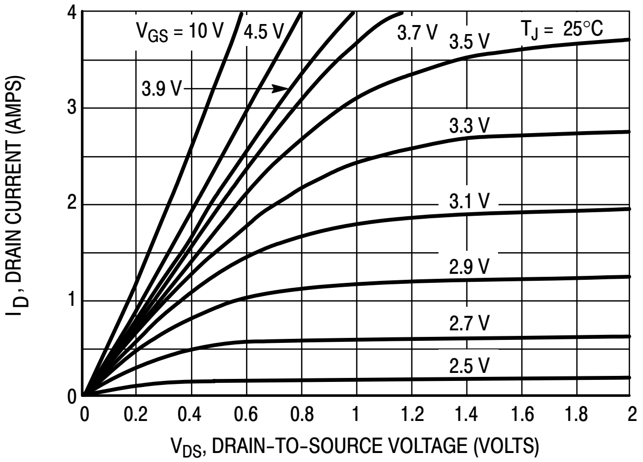


Figure 1. On–Region Characteristics

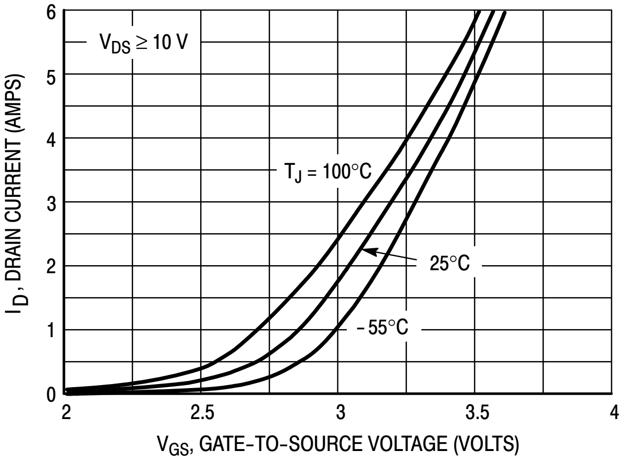


Figure 2. Transfer Characteristics

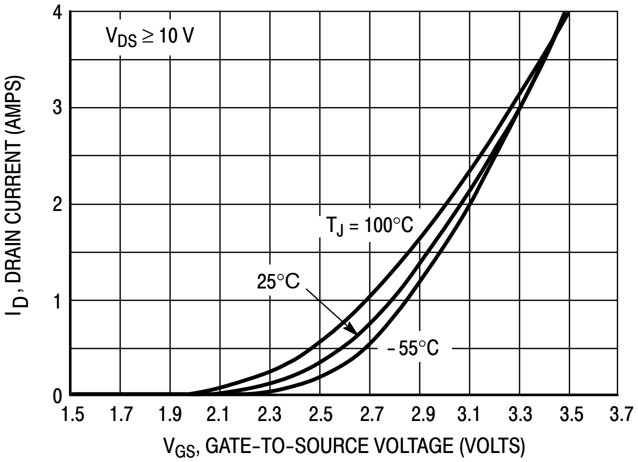


Figure 2. Transfer Characteristics

TYPICAL ELECTRICAL CHARACTERISTICS

N−Channel

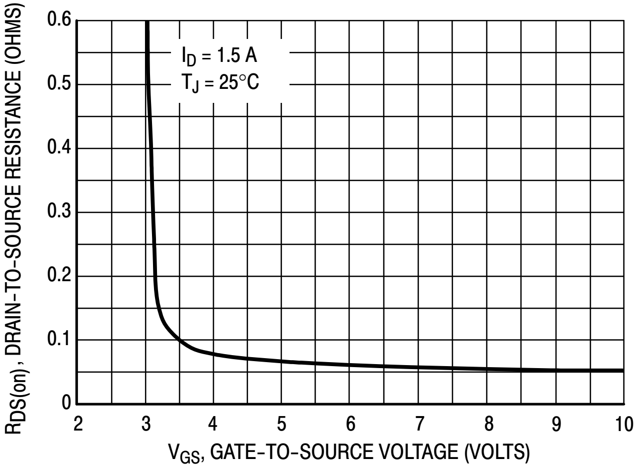


Figure 3. On−Resistance versus Gate−To−Source Voltage

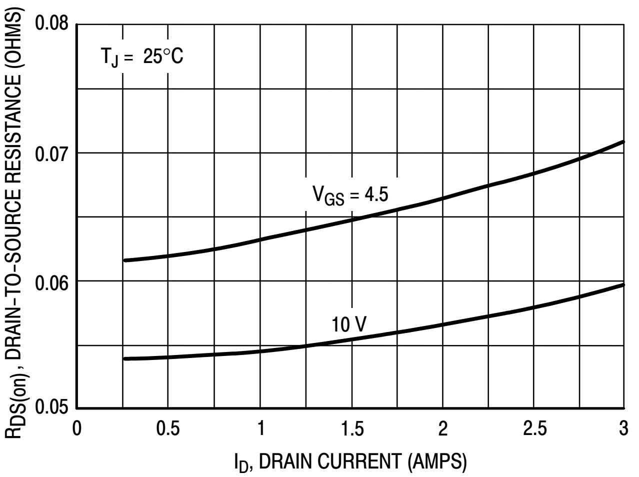


Figure 4. On−Resistance versus Drain Current and Gate Voltage

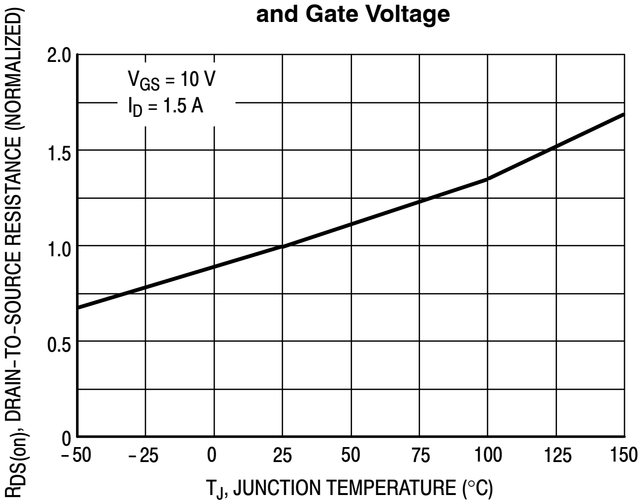


Figure 5. On−Resistance Variation with Temperature

P−Channel

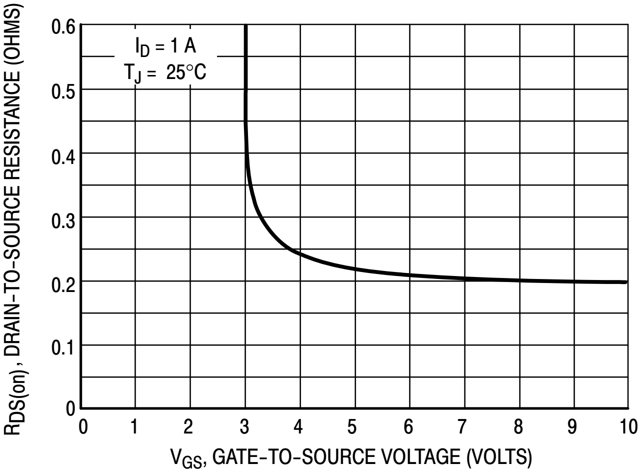


Figure 3. On−Resistance versus Gate−To−Source Voltage

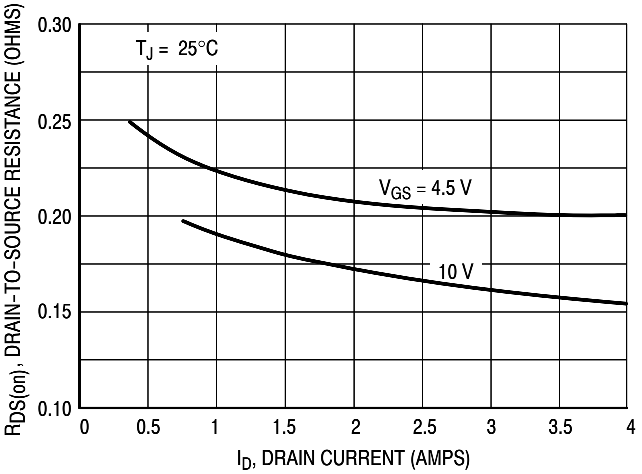


Figure 4. On−Resistance versus Drain Current and Gate Voltage

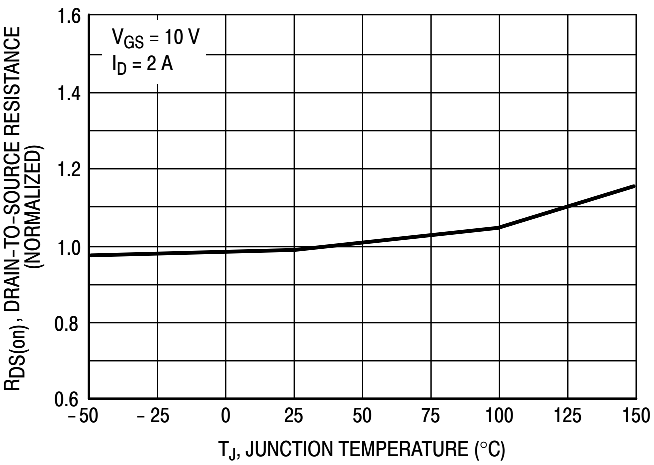


Figure 5. On−Resistance Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

N−Channel

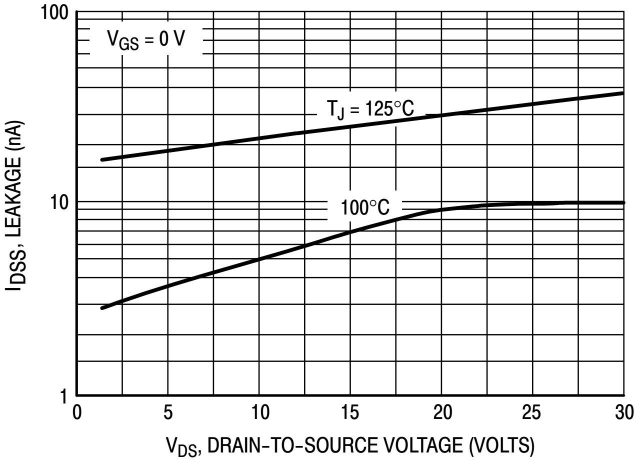


Figure 6. Drain−To−Source Leakage Current versus Voltage

P−Channel

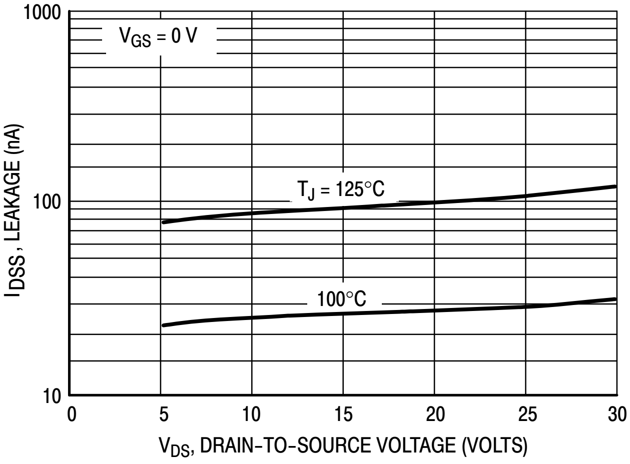


Figure 6. Drain−To−Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

N−Channel

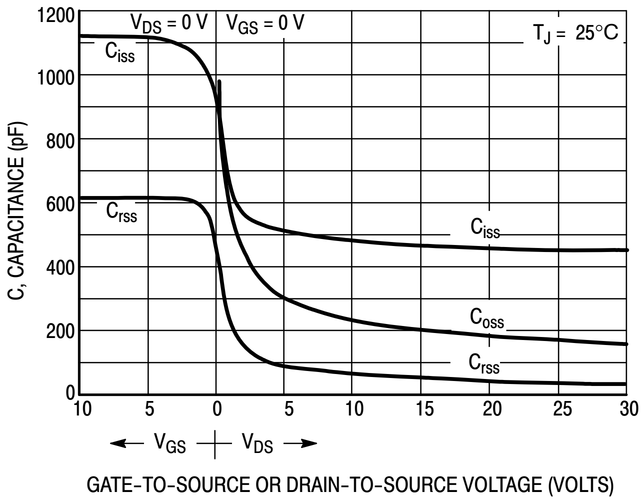


Figure 7. Capacitance Variation

P−Channel

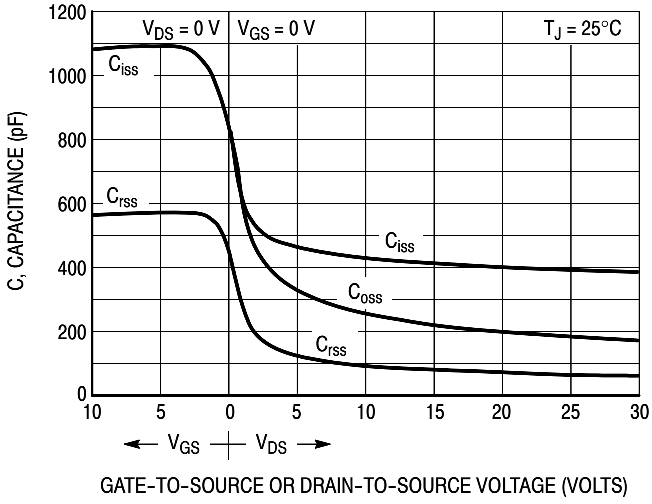


Figure 7. Capacitance Variation

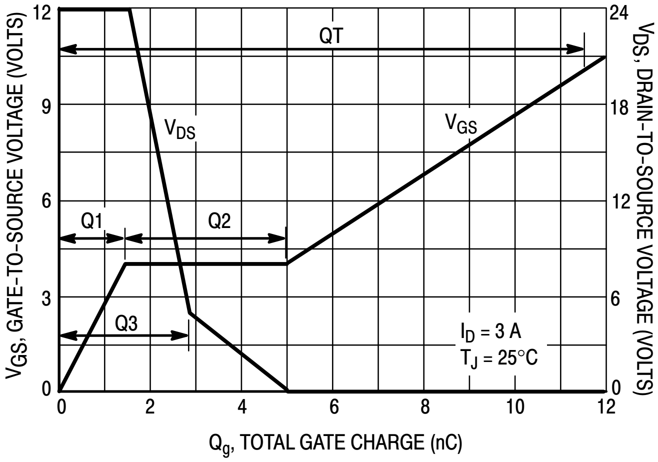


Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

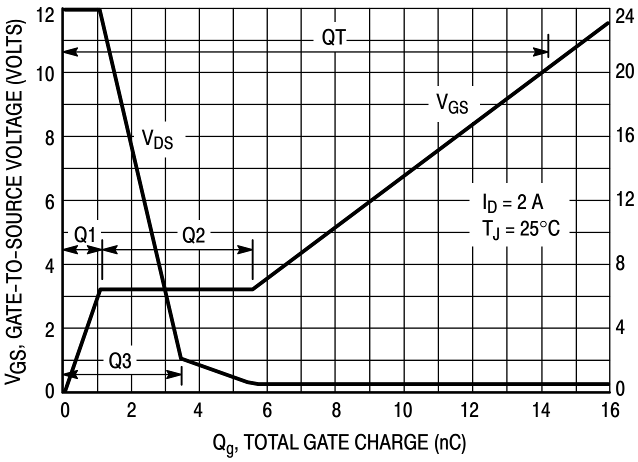


Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

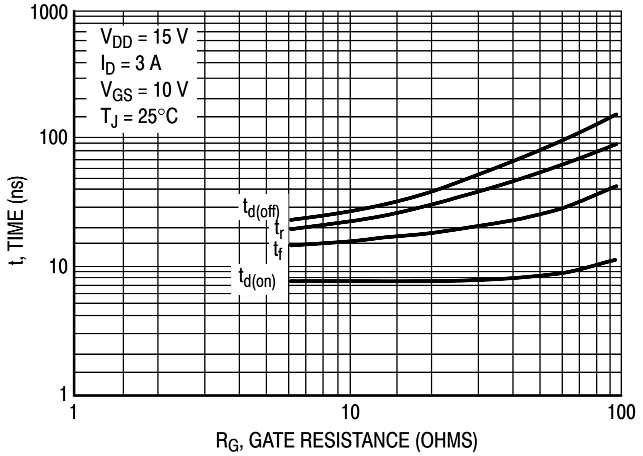


Figure 9. Resistive Switching Time Variation versus Gate Resistance

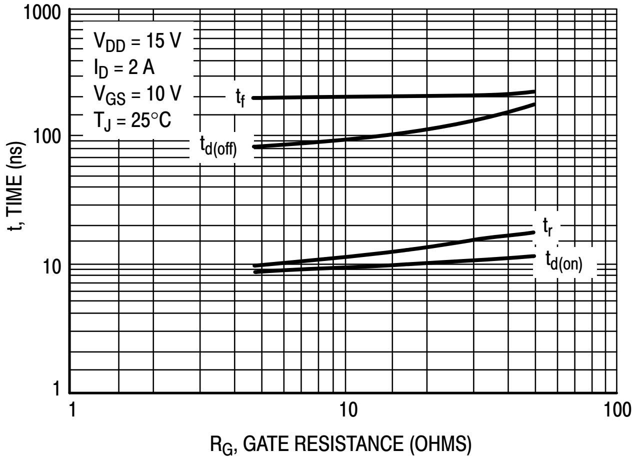


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN−TO−SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

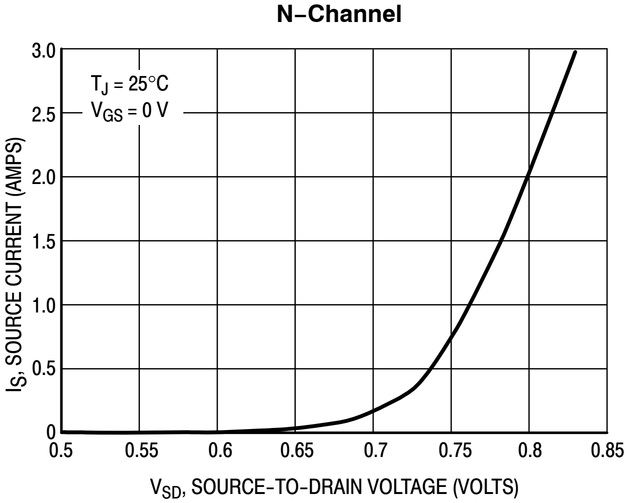

N−Channel

Figure 10. Diode Forward Voltage versus Current

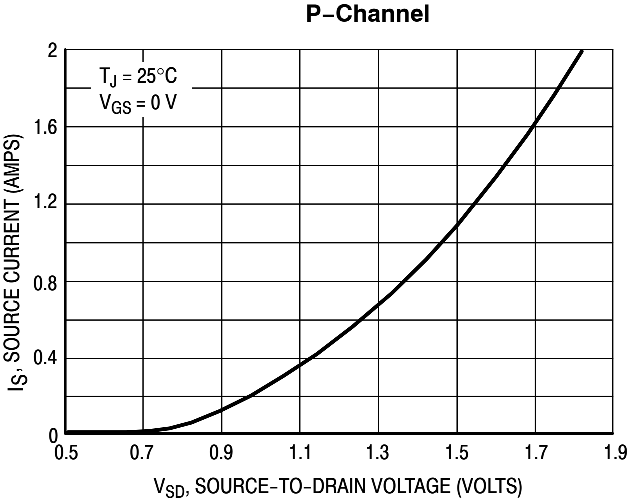

P−Channel

Figure 10. Diode Forward Voltage versus Current

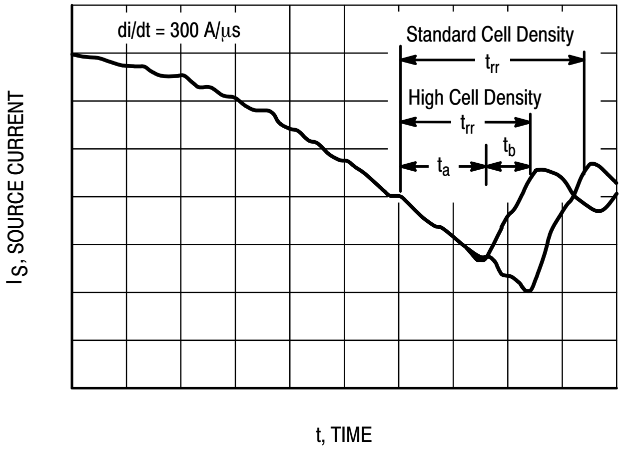


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance − General Data and Its Use.”

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E−FETs can withstand the stress of drain−to−source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

N−Channel

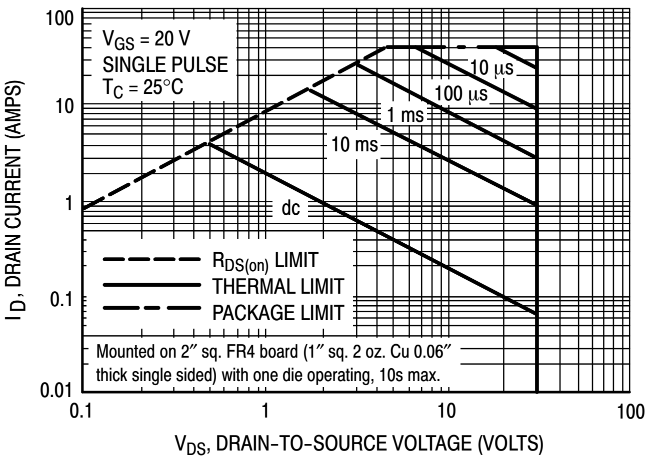


Figure 12. Maximum Rated Forward Biased Safe Operating Area

P−Channel

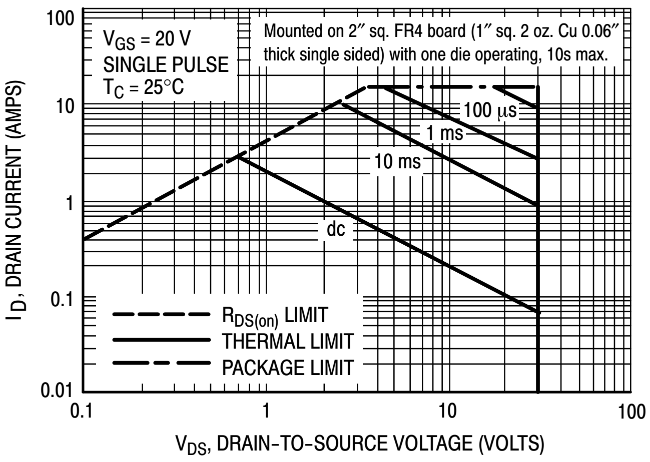


Figure 12. Maximum Rated Forward Biased Safe Operating Area

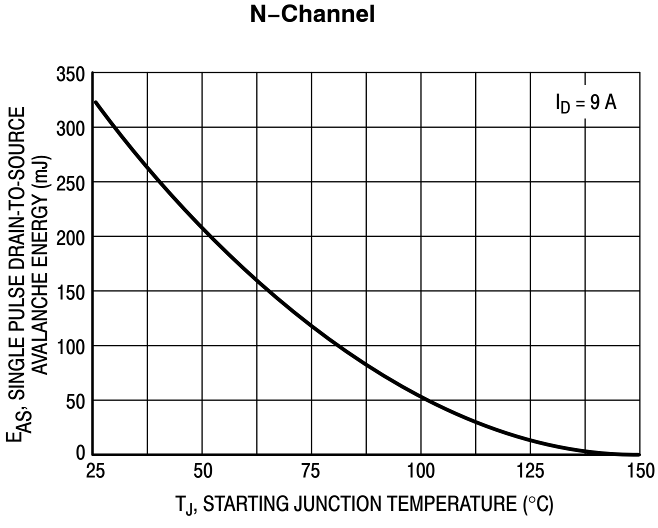

N−Channel

Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

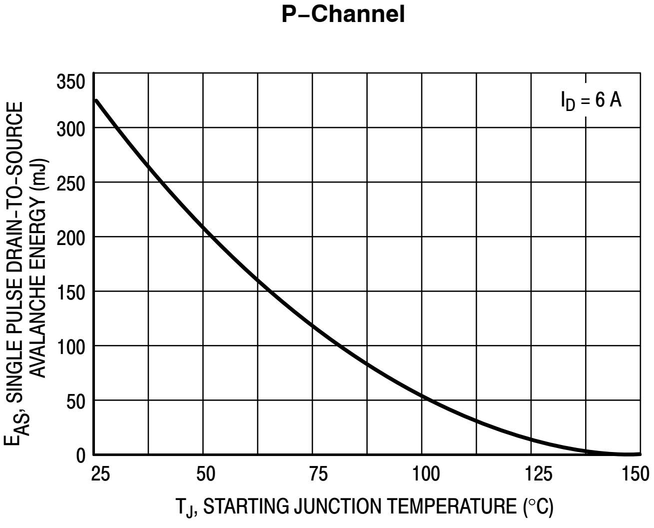

P−Channel

Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

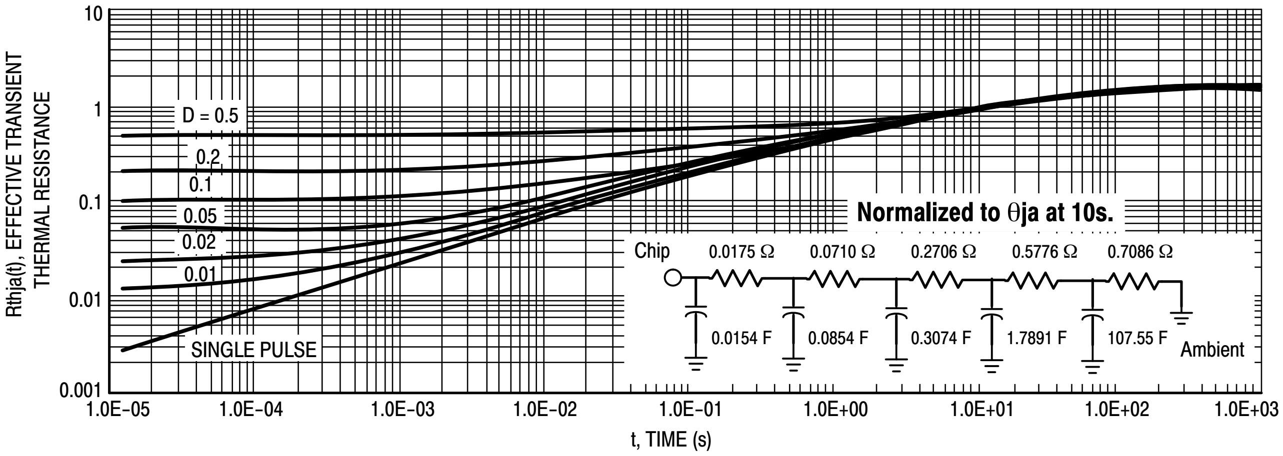


Figure 14. Thermal Response

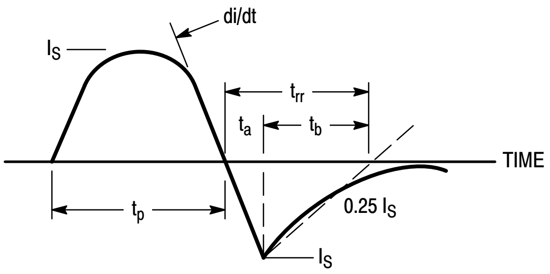
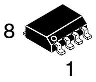


Figure 15. Diode Reverse Recovery Waveform

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

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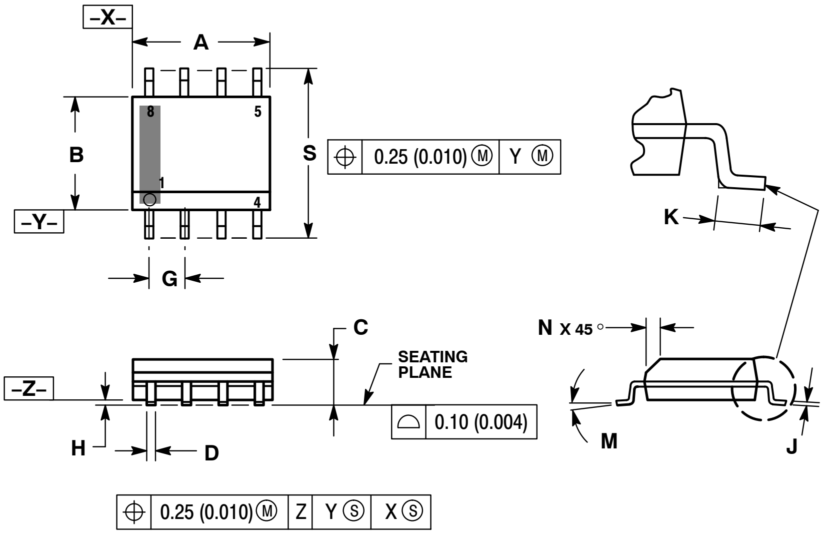
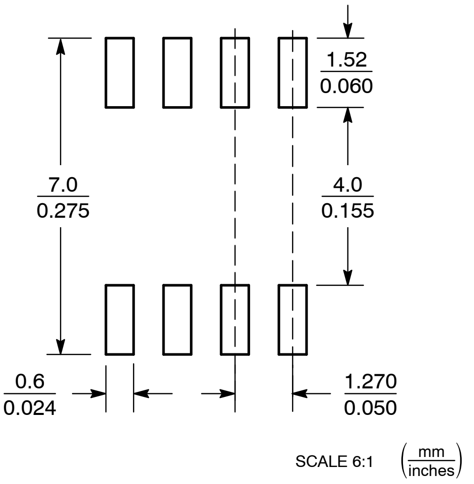


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

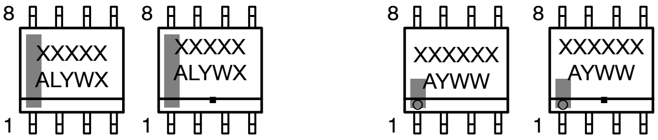
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC **IC (Pb−Free)** **Discrete** **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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