产品概览

MC100LVEL14: 3.3 V ECL 1:5 Clock Distribution Chip

欲看完整文档，请参阅数据表。

The MC100LVEL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The LVEL14 is functionally and pin compatible with the EL14 but is designed to operate in ECL or PECL mode for a voltage supply range of -3.0 V to -3.8 V (or 3.0 V to 3.8 V). The LVEL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input. The common enable (EN) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input. The VBB pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to VBB as a switching reference voltage. VBB may also rebias AC coupled inputs. When used, decouple VBB and VCC via a 0.01 5F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, VBB should be left open.

特性

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: VCC = 3.0 V to 3.8 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = -3.0 V to -3.8 V
- Internal Input Pulldown Resistors on CLK
- Q Output will Default LOW with Inputs Open or at VEE
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

For more features, see the data sheet

器件电气规格

产品	Compliance	Status	Type	Channels	Input / Output Ratio	Input Level	Output Level	V_{CC} Typ (V)	t_{jitter} RMS Typ (ps)	$t_{skew(o-o)}$ Max (ps)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	f_{max} Clock Typ (MHz)	f_{max} Data Typ (Mbps)	Package Type
MC100LVEL14DWG	Pb-free Halide free	Active	Buffer	1	2:1:5	ECL LVDS	ECL	3.3	0.2	50	0.68	500	1000		SOIC-20W
MC100LVEL14DWR2G	Pb-free Halide free	Active	Buffer	1	2:1:5	LVDS ECL	ECL	3.3	0.2	50	0.68	500	1000		SOIC-20W

欲了解更多信息，请联系您当地的销售支援 www.onsemi.cn 。

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