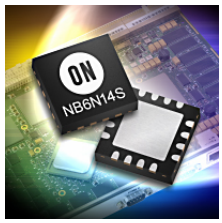
产品概览



NB6N14S: Clock / Data Fanout Buffer, 1:4 AnyLevel™ Input, LVDS, 3.3 V

欲看完整文档，请参阅数据表。

The NB6N14S is a differential 1:4 Clock or Data Receiver and will accept AnyLevel input signals: LVPECL, CML, HCSL, LVCMOS, LVTTL, or LVDS. These signals will be translated to LVDS and four identical copies of Clock or Data will be distributed, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB6N14S is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications. The NB6N14S has a wide input common mode range from GND + 50mV to VCC - 50mV. Combined with the 50-ohm internal termination resistors at the inputs, the NB6N14S is ideal for translating a variety of differential or single-ended Clock or Data signals to 350mV typical LVDS output levels. The NB6N14S is offered in a small 3mm X 3mm 16-QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

特性

- Maximum Input Clock Frequency > 2.0 GHz
- Maximum Input Data Rate > 2.5 Gb/s
- 1 ps Maximum RMS Clock Jitter
- Typically 10 ps of Data Dependent Jitter
- 380 ps Typical Propagation Delay
- 120 ps Typical Rise and Fall Times
- Pb-Free

应用

- Base Stations, Networking, Communications, Computing and ATE

器件电气规格

产品	Pricing ($/Unit)	Compliance	Status	Type	Channels	Input / Output Ratio	Input Level	Output Level	V_{CC} Typ (V)	t_{jitter} RMS Typ (ps)	$t_{skew(o-o)}$ Max (ps)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	f_{max} Clock Typ (MHz)	f_{max} Data Typ (Mbps)	Package Type
NB6N14SMNG		Pb-free Halide free non AEC-Q and PPAP	Active	Buffer	1	1:4	CML CMOS ECL LVDS TTL	LVDS	3.3	0.5	20	0.45	190	2000	2500	QFN-16
NB6N14SMNR2G		Pb-free Halide free non AEC-Q and PPAP	Active	Buffer	1	1:4	CML CMOS ECL LVDS TTL	LVDS	3.3	0.5	20	0.45	190	2000	2500	QFN-16

欲了解更多信息，请联系您当地的销售支援 www.onsemi.cn 。

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