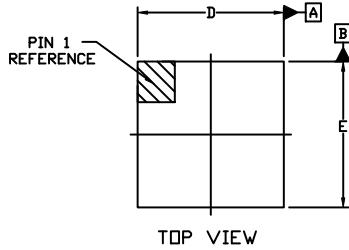
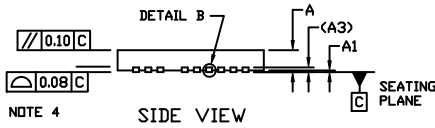


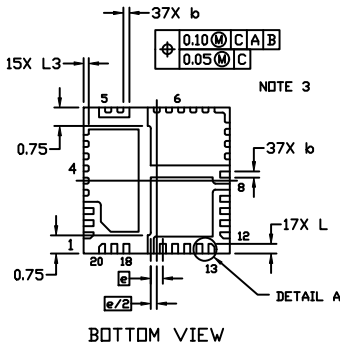
SCALE 2:1



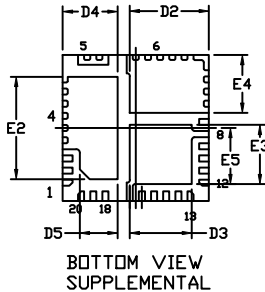
TOP VIEW



SIDE VIEW



BOTTOM VIEW



BOTTOM VIEW SUPPLEMENTAL

GENERIC MARKING DIAGRAM*



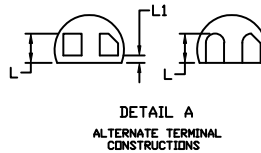
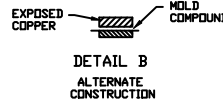
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

QFN20 6x6, 0.5P
CASE 485FC
ISSUE C

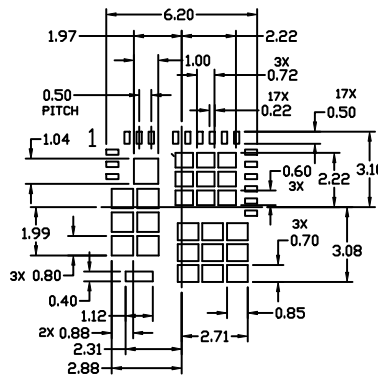
DATE 12 FEB 2019

NOTES:

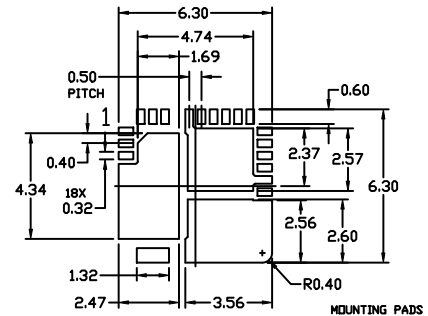
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	5.85	6.00	6.15
D2	3.15	3.25	3.35
D3	2.50	---	2.60
D4	2.15	2.25	2.35
D5	1.50	---	1.60
e	0.50 BSC		
E	5.85	6.00	6.15
E2	4.15	---	4.25
E3	2.38	---	2.48
E4	2.28	2.38	2.48
E5	2.20	2.30	2.40
L	0.30	0.40	0.50
L1	---	---	0.15
L3	0.10	0.20	0.30



RECOMMENDED STENCIL PATTERN



RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the IN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	QFN20 6x6, 0.5P	PAGE 1 OF 1

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