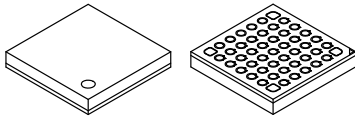


MECHANICAL CASE OUTLINE

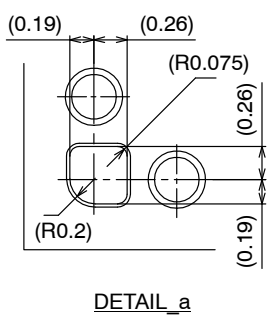
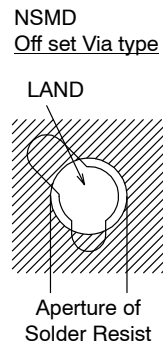
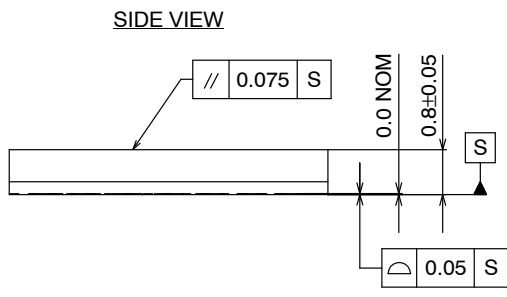
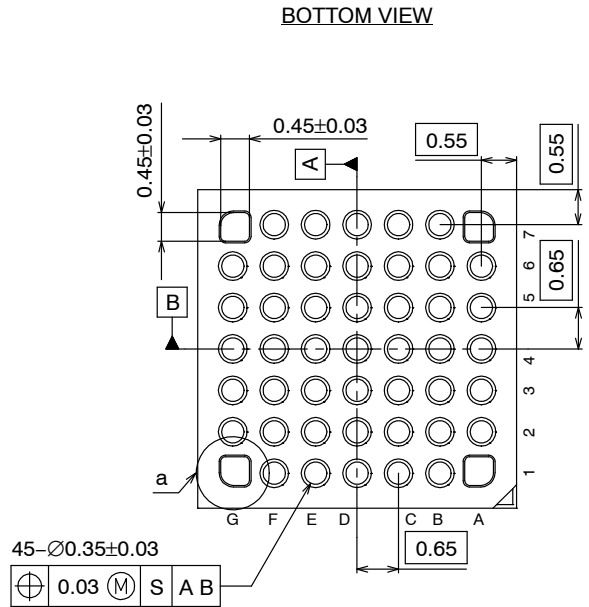
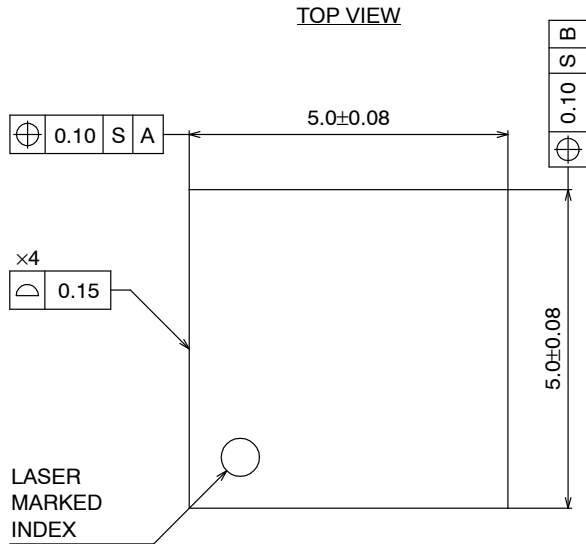
PACKAGE DIMENSIONS

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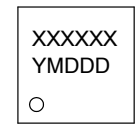


LFLGA49 5x5 / FLGA49J
CASE 569AC
ISSUE A

DATE 17 JAN 2014



GENERIC MARKING DIAGRAM*



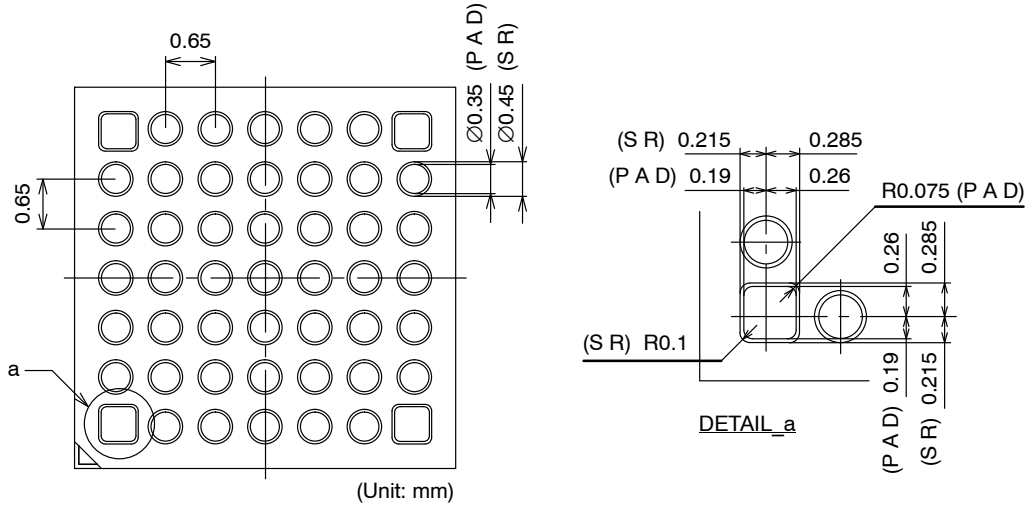
XXXXXX = Specific Device Code
 Y = Year
 M = Month
 DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

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SOLDERING FOOTPRINT*



NOTES:

1. The measurements are not to guarantee but for reference only.
2. Module level verification after set designing must be implemented. Validating solderability and Reliability verification for joint areas such as Exposed Die-pad and must be carried out. Drawing above is a design applicable for NSMD pad specification. For SMD pad specification, layout of SR opening size specified as PKG terminal size = Pad size is to be complied.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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