MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®
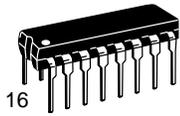
PDIP–16
CASE 648–08
ISSUE V

DATE 22 APR 2015

SCALE 1:1

TOP VIEW

END VIEW
WITH LEADS CONSTRAINED
NOTE 5

SIDE VIEW

$\boxed{\oplus}$ 0.010 Ⓜ C A Ⓜ B Ⓜ

END VIEW
NOTE 6
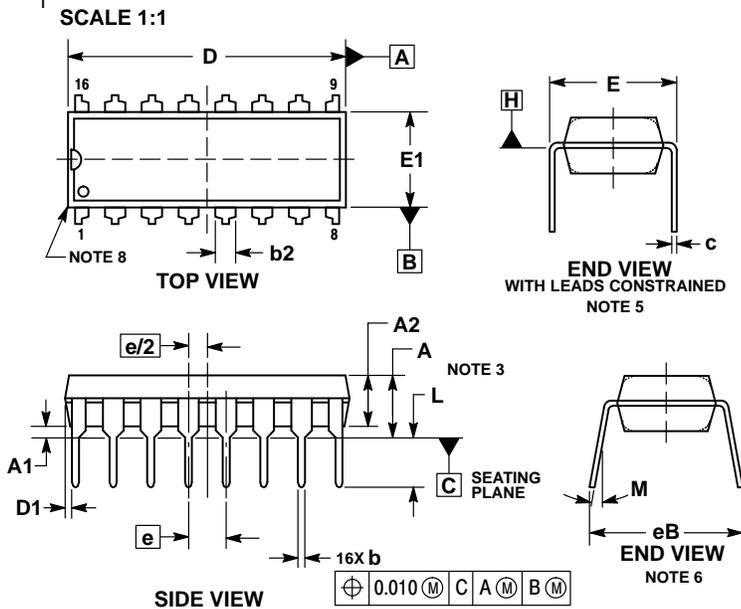
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–––––	0.210	–––	5.33
A1	0.015	–––––	0.38	–––
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	–––––	0.13	–––
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	–––––	0.430	–––	10.92
L	0.115	0.150	2.92	3.81
M	–––––	10°	–––	10°

GENERIC
MARKING DIAGRAM*

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XXXXXXXXXXX
XXXXXXXXXXX
AWLYYWWG
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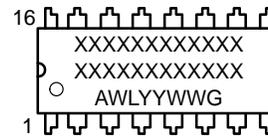
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present.

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

DOCUMENT NUMBER:	98ASB42431B	
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	PDIP–16	PAGE 1 OF 2

ISSUE	REVISION	DATE
T	ADDED MARKING DIAGRAM. REQ. BY S. FARRETTA	04 MAY 2004
U	REDRAWN TO UNIFORM FABRICATION SITE SPECIFICATIONS. REQ. BY J. LETTERMAN.	05 JUN 2013
V	CORRECTED DIMENSION REFERENCE IN NOTE 6 FROM E3 TO eB. REQ. BY JJ. YEOH.	22 APR 2015