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AN-9095

Smart Power Module 1200V Motion SPM3® Series Application Note

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APPLICATION NOTE

1 Introduction

This application note supports the 1200 V rated Motion SPM® 3 module. It should be used in conjunction with 1200 V Motion SPM 3 datasheet and application notes *AN-9086 - SPM 3 Package Mounting Guidance*.

1.1 Design Concept

Provides a minimized package and low power consumption module with improved reliability. This is achieved by applying a new 1200 V gate-driving high-voltage integrated circuit (HVIC), a new insulated-gate bipolar transistor (IGBT) of advanced silicon technology, and improved direct bonded copper (DBC) substrate base transfer mold package.

1200 V Motion SPM 3 module achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverterized motor drives for industrial use, such as fan motor for air conditioners, small power general-purpose inverters, and serve motors.

The temperature-sensing function of Motion SPM 3 product is implemented in the LVIC to enhance system reliability. An analog voltage proportional to the temperature of the LVIC is provided for monitoring the module temperature and necessary protections against over-temperature situations.

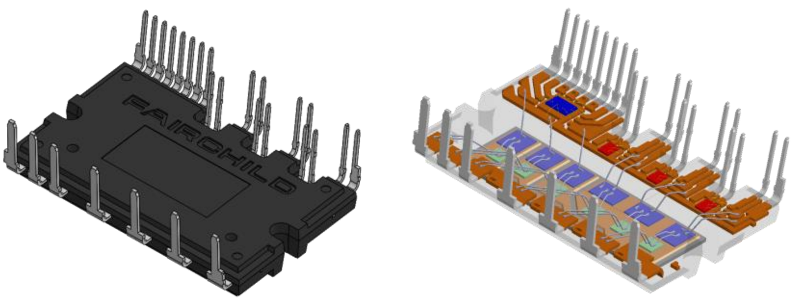

Figure 1. External View and Internal Structure of Motion SPM 3 Series

Table 1. Product Line-up and Target Application

Target Application	Fairchild Device	IGBT Rating	Motor Rating[2]	Isolation Voltage
Motor drives for industrial use, System air conditioners, General-purpose inverters, Servo driver	FSBB10CH120D(F)[1]	10 A / 1200 V	1.5 kW / 440 V_{AC}	V_{ISO} = 2500 V_{RMS} (Sine 60 Hz, 1 min All Shorted Pins Heat Sink)
	FSBB15CH120D(F)	15 A / 1200 V	2.2 kW / 440 V_{AC}	
	FSBB20CH120D(F)	20 A / 1200 V	3.0 kW / 440 V_{AC}	

Notes:

1. Difference between FSBB10CH120D and FSBB10CH120DF is temperature sensing range. Temperature range of FSBB10CH120D is 0 ~ 150ºC, FSBB10CH120DF is -25 ~ 125°C.
2. These motor ratings are simulation results under following conditions: V_{AC} = 440 V, V_{DD} = 15 V, T_C = 100°C, T_J = 150°C, f_{PWM} = 5 kHz, PF=0.8, MI=0.9, Motor efficiency=0.75, overload 150% for 1min. ***These motor ratings are general rating, so may be changed by conditions.***

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1.2 Ordering Information

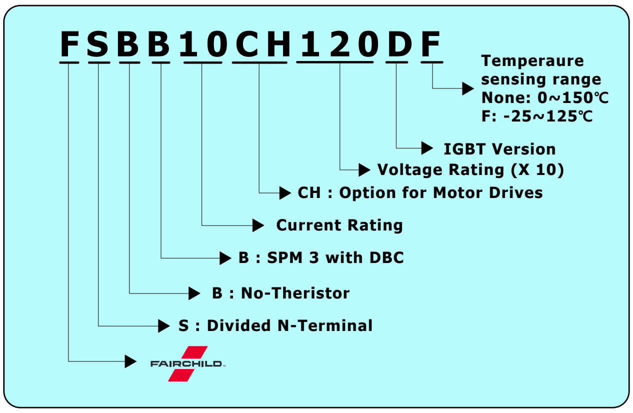


Figure 2. Ordering Information

1.3 Features and Integrated Functions

- DBC Substrate
  - Excellent Thermal Conductivity, Keeping 2500 V_{rms} Isolation Voltage from Pin to Heat Sink
- Integrated Components:
  - One-Channel HVIC (three HVIC) for High-Side IGBTs Control
  - Three-Channel LVIC (one LVIC) for Low-Side IGBTs Control
  - Six IGBTs / Diodes
  - Temperature Sensing of LVIC(Optional)
- Control Drive Supply:
- Single DC Supply Compatible Using Integrated Bootstrap Diode
- High-Side Gate Driver (One-Channel)
  - High-Voltage Level-Shift Circuit
  - Input interface: Active HIGH
  - Compatible for 3.3 V Controller Outputs
  - Under-Voltage Lockout without Fault Signal
- Low-Side Gate Driver (Three-Channel)
  - Input Interface: Active HIGH
  - Compatible for 3.3 V Controller Outputs
  - Under-Voltage Lockout with Fault Signal
  - Short-Circuit, Over-Current Protection
- Soft Turn-off Prevents Excessive Surge Voltage
- Temperature Sensing of LVIC (2 kind option)

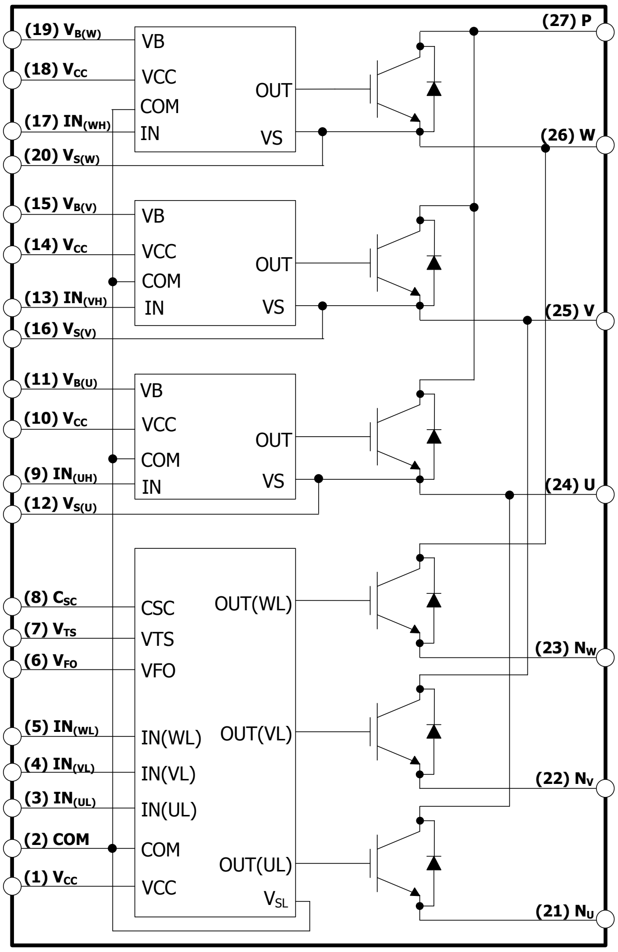


Figure 3. Internal Equivalent Circuit, Input / Output Pins

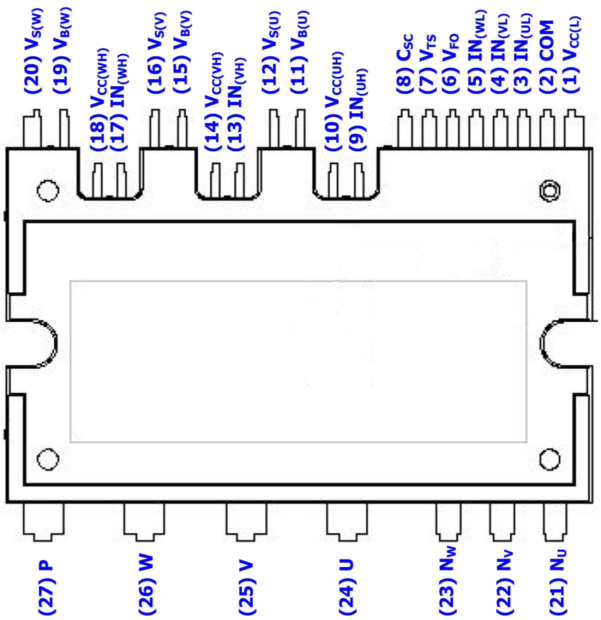


Figure 4. Package Top-View and Pin Assignment

2 Product Synopsis

This section discusses pin descriptions, electrical specifications, characteristics, and packaging.

Table 2. Pin Description

Pin Number	Name	Description
1	VCC(L)	Low-Side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	IN(UL)	Signal Input for Low-Side U Phase
4	IN(VL)	Signal Input for Low-Side V Phase
5	IN(WL)	Signal Input for Low-Side W Phase
6	VFO	Fault Output
7	VTS	Thermal Sensing Voltage in LVIC
8	CSC	Voltage Input for SC detection
9	IN(UH)	Signal Input for High-Side U Phase
10	VCC(UH)	High-Side Bias Voltage for U Phase IC
11	VB(U)	High-Side Bias Voltage for U Phase IGBT Driving
12	VS(U)	High-Side Bias Voltage Ground for U Phase IGBT Driving
13	IN(VH)	Signal Input for High-Side V Phase
14	VCC(VH)	High-Side Bias Voltage for V Phase IC
15	VB(V)	High-Side Bias Voltage for V Phase IGBT Driving
16	VS(V)	High-Side Bias Voltage Ground for V Phase IGBT Driving
17	IN(WH)	Signal Input for High-Side W Phase
18	VCC(WH)	High-Side Bias Voltage for W Phase IC
19	VB(W)	High-Side Bias Voltage for W Phase IGBT Driving
20	VS(W)	High-Side Bias Voltage Ground for W Phase IGBT Driving
21	NU	Negative DC-Link Input for U Phase
22	NV	Negative DC-Link Input for V Phase
23	NW	Negative DC-Link Input for W Phase
24	U	Output for U Phase
25	V	Output for V Phase
26	W	Output for W Phase
27	P	Positive DC-Link Input

2.1 Detailed Pin Definition & Notification

- High-Side Bias Voltage Pins for Driving the IGBTs / High-Side Bias Voltage Ground Pins for Driving the IGBTs:
  - ► Pins: VB(U)-VS(U), VB(V)-VS(V), VB(W)-VS(W)
  - These are drive power supply pins for providing gate drive power to the high-side IGBTs.
  - The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs.
  - Each bootstrap capacitor is charged from the V_{CC} supply during ON state of the corresponding low-side IGBT.
  - To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to these pins.
- Low-Side Bias Voltage Pin / High-Side Bias Voltage Pins:
  - ► Pins: VCC(L), VCC(WH), VCC(VH), VCC(UH)
  - These are control supply pins for the built-in ICs.
  - These four pins should be connected externally.
  - To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to these pins.
- Common Supply Ground Pins
  - ► Pins: COM
  - These are supply ground pins for the built-in ICs.
  - Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.
- High-Side Bias Voltage Pins for Driving the IGBTs / High-Side Bias Voltage Ground Pins for Driving the IGBTs
  - ► Pins: VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)
  - These are drive power supply pins fro providing gate drive power to the high-side IGBTs.
  - The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs.
  - Each bootstrap capacitor is charged from the VCC supply during the ON-state of the corresponding low-side IGBTs.

    In order to prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mount very close to these pins.
- Signal Input Pins
  - ► Pins: IN(UL), IN(VL), IN(WL), IN(UH), IN(VH), IN(WH)
  - These pins control the operation of the built-in IGBTs.
  - They are activated by voltage input signals. The terminals are internally connected to a Schmitt-trigger circuit composed of 5 V-class CMOS.
  - The signal logic of these pins is active HIGH. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
  - The wiring of each input should be as short as possible to protect the Motion SPM® 3 module against noise influences.
  - To prevent signal oscillations, an RC coupling as illustrated in *Figure 29* is recommended.
- Fault Out Duration Selection Pin / Analog Temperature Sensing Output Pin
  - ► Pin: VTS
  - This indicates the temperature of the V-phase LVIC with analog voltage. LVIC itself creates some power loss, but mainly heat generated from the IGBTs increase the temperature of the LVIC.
  - V_{TS} versus temperature characteristics are illustrated in *Figure 38*
- Short-Circuit and Over-Current Detection Input Pin
  - ► Pin: CSC
  - The current detecting resistor (shunt resistor) should be connected between low pass filter before the pin CSC and the low-side ground (COM) to detect over-current or short-circuit current.
    (Figure 21)
  - The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to the CSC pin to eliminate noise.

    The connection length between the shunt resistor and CSC pin should be minimized.

- Fault Output Pin
  - ▶ Pin: VFO
  - This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the SPM® module.
  - The alarm conditions are: Short-Circuit Protection (SCP), and low-side bias Under-Voltage Lockout (UVLO).
  - The VFO output is open drain configured. The VFO signal line should be pulled to the 5 V logic power supply with approximately 4.7 kΩ resistance.
- Positive DC-Link Pin
  - ▶ Pin: P
  - This is the DC-link positive power supply pin of the inverter.
  - It is internally connected to the collectors of the high-side IGBTs.
  - To suppress surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: metal film capacitor is typically used).
- Negative DC-Link Pins
  - ▶ Pins: NU, NV, NW
  - These are the DC-link negative power supply pins (power ground) of the inverter.
  - These pins are connected to the low-side IGBT emitters of the each phase.
- Inverter Power Output Pins
  - ▶ Pins: U, V, W
  - Inverter output pins for connecting to the inverter load (e.g. motor).

2.2 Absolute Maximum Ratings (TJ=25°C, unless otherwise specified)

Table 3. Inverter (Based on FSBB10CH120D)

Symbol	Parameter	Conditions	Rating	Unit
V_{PN}	Supply Voltage	Applied between P – NU, NV, NW	900	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P – NU, NV, NW	1000	V
V_{CES}	Collector – Emitter Voltage		1200	V
$\pm I_C$	Each IGBT Collector Current	T_C=25°C, $T_J \leq$150°C	10	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C=25°C, $T_J \leq$150°C, Under 1 ms Pulse Width	20	A
P_C	Collector Dissipation	T_C=25°C per Chip	69	W
T_J	Operating Junction Temperature(3)		-40~150	°C

Note:
3. The maximum junction temperature rating of the power chips integrated within the Motion SPM 3 product is 150°C.

Table 4. Control Part

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Control Supply Voltage	Applied between VCC(H), VCC(H) - COM	20	V
V_{BS}	High-Side Control Bias Voltage	Applied between VB(x), VS(x)	20	V
V_{IN}	Input Signal Voltage	Applied between IN(xH), IN(xL) - COM	-0.3~V_{CC}+0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between VFO - COM	-0.3~V_{CC}+0.3	V
I_{FO}	Fault Output Current	Sink Current at VFO Pin	2	mA
V_{SC}	Current Sensing Input Voltage	Applied between CSC - COM	-0.3~V_{CC}+0.3	V

Table 5. Total System

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short-Circuit Protection Capability)	V_{CC}, V_{BS}=13.5~16.5 V, T_J=150℃, Non-Repetitive, < 2 μs	800	V
T_C	Module Case Operation Temperature	*See Figure 5*	-40~125	°C
T_{STG}	Storage Temperature		-40~125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1-Minute, Connect Pins to Heat Sink	2500	V_{rms}

Table 6. Thermal Resistance

Symbol	Parameter	Conditions		Rating	Unit
$R_{th(j-c)Q}$	Junction-to-Case Thermal Resistance	Inverter IGBT Part (per 1/6 Module)	FSBB10CH120D(F)	1.80	°C/W
			FSBB15CH120D(F)	1.50	
			FSBB20CH120D(F)	0.60	
$R_{th(j-c)F}$		Inverter FWD Part (per 1/6 Module)	FSBB10CH120D(F)	2.75	
			FSBB15CH120D(F)	1.75	
			FSBB20CH120D(F)	0.90	

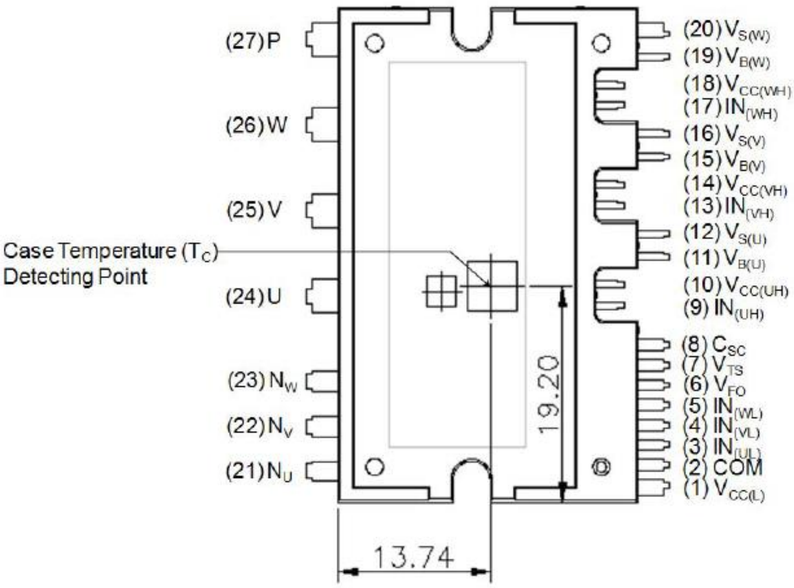


Figure 5. Case Temperature (T_C) Detecting Point

Table 7. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P - NU, NV, NW	400	600	800	V
V_{CC}	Control Supply Voltage	Applied between VCC(xH) - COM(H), VCC(L) - COM(L)	13.5	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between VB(x) - VS(x)	13.0	15.0	18.5	V
dV_{CC}/dt, dV_{BS}/dt	Control Supply Variation		-1		+1	V/µs
t_{dead}	Blanking Time for Preventing Arm-Short	For Each Input Signal	2.0			µs
f_{PWM}	PWM Input Signal	$-40°C \le T_C \le 125°C$, $-40°C \le T_J \le 150°C$			20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between NU, NV, NW - COM(H, L) (Including Surge Voltage)	-5		5	V
$P_{WIN(ON)}$	Minimum Input Pulse Width(4)	IC ≤ 20 A, Wiring Inductance between NU, NV, NW and DC Link N < 10 nH	1.5			µs
$P_{WIN(OFF)}$			1.5			
T_J	Junction Temperature		-40		150	°C

Note:

4. This product might not make response if the input pulse width is less than the recommended value.

2.3 Electrical Characteristics (TJ=25°C, unless otherwise specified)

Table 8. Inverter Part (Based on FSBB10CH120D)

Symbol		Parameter	Conditions		Min.	Typ.	Max.	Unit
$V_{CE(SAT)}$		Collector – Emitter Saturation Voltage	V_{CC}, V_{BS}=15 V, V_{IN}=5 V	I_C=10 A, T_J=25°C		2.2	2.8	V
V_F		FWDi Forward Voltage	V_{IN}=0 V	I_F=10 A, T_J=25°C		2.2	2.8	V
HS	t_{ON}	Switching Times	V_{PN}=600 V, V_{CC}=15 V, V_{BS}=15 V, I_C=10 A T_J=25, V_{IN}=0 V ↔5 V, Inductive Load(5)		0.45	0.85	1.35	μs
	$t_{C(ON)}$					0.25	0.60	
	t_{OFF}					0.95	1.50	
	$t_{C(OFF)}$					0.10	0.45	
	t_{rr}					0.25		
LS	t_{ON}					0.75	1.25	
	$t_{C(ON)}$					0.20	0.55	
	t_{OFF}					0.95	1.50	
	$t_{C(OFF)}$					0.10	0.45	
	t_{rr}					0.20		
I_{CES}		Collector – Emitter Leakage Current	V_{CE}=V_{CES}				5	mA

Note:

5. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of the IGBT itself under the given gate driving condition internally. *For the detailed information, see Figure 6 and Figure 7*.

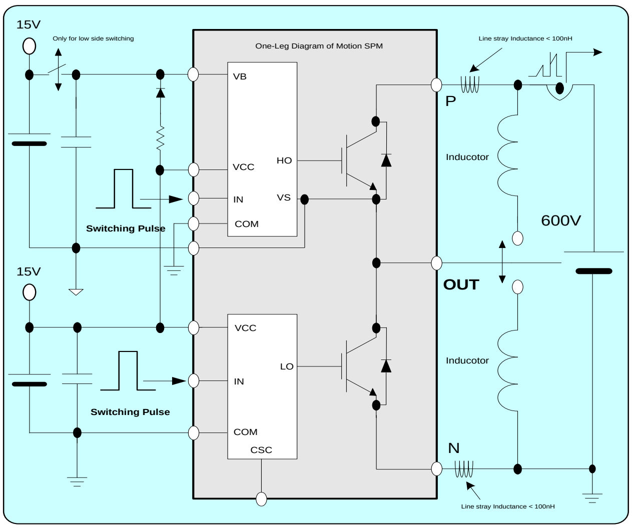


Figure 6. Switching Evaluation Circuit

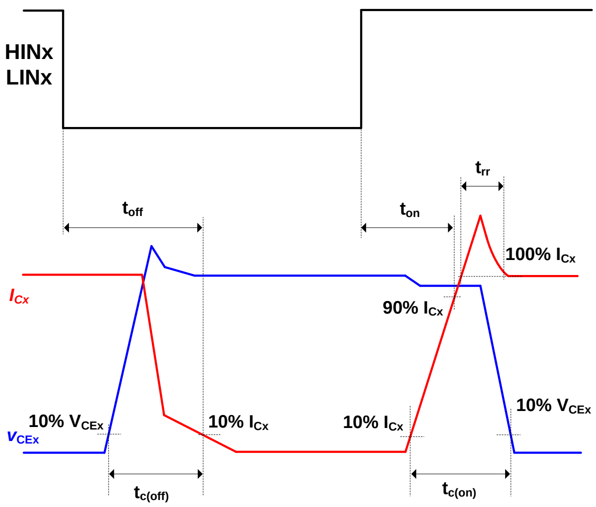


Figure 7. Switching Time Definition

Table 9. Control Part

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{QCCH}	Quiescent V_{CC} Supply Current	VCC(xH)=15 V, IN(xH)=0 V	VCC(xH) - COM(H)			0.15	mA
I_{QCCL}		VCC(L)=15 V, IN(xL)=0 V	VCC(L) - COM(L)			5.00	
I_{PCCH}	Operating High-Side V_{CC} Supply Current	VCC(xH)=15 V, f_{PWM}=20 kHz, Duty=50%, Applied to One PWM Signal Input for High Side				0.30	mA
I_{PCCL}	Operating Low-Side V_{CC} Supply Current	VCC(L)=15 V, f_{PWM}=20 kHz, Duty=50%, Applied to One PWM Signal Input for Low Side				8.5	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS}=15 V, IN(xH)=0 V	VB(x) - VS(x)			0.30	mA
I_{PBS}	Operating V_{BS} Supply Current	V_{CC}=V_{BS}=15 V, f_{PWM}=20 kHz, Duty=50%, Applied to One PWM Signal Input for High Side				4.50	mA
V_{FOH}	Fault Output Voltage	V_{CC}=15 V, V_{SC}=0 V, V_{FO} Circuit: 4.7 kW to 5 V Pull-up		4.5			V
V_{FOL}		V_{CC}=15 V, V_{SC}=1 V, V_{FO} Circuit: 4.7 kW to 5 V Pull-up				0.5	
$V_{SC(ref)}$	Short-Circuit Trip Level	V_{CC}=15 V[(6)]	CSC - COM(L)	0.43	0.50	0.57	V
UV_{CCD}	Supply Circuit, Under-Voltage Protection	Detection Level		10.3		12.8	V
UV_{CCR}		Reset Level		10.8		13.3	
UV_{BSD}		Detection Level		9.5		12.0	
UV_{BSR}		Reset Level		10.0		12.5	
t_{FOD}	Fault-Out Pulse Width			50.0			μs
$V_{IN(ON)}$	ON Threshold Voltage	Applied between IN(xH) - COM(H), IN(xL) - COM(L)				2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8			

Note:

6. Short-circuit current protection is functioning only at the low-sides IGBTs.

3 Package

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade-off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to good package technology lies in the optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

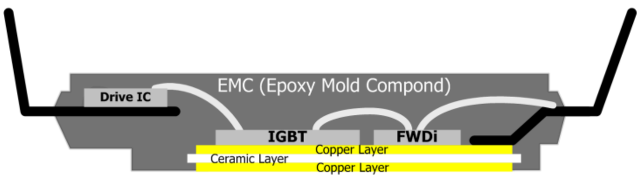


Figure 8. Vertical Structure of SPM 3 Package

In SPM 3 package, technology was developed with DBC substrate that resulted in good heat dissipation characteristics. Power chips are attached directly to the DBC substrate. This technology is applied SPM 3 package, achieving improved reliability and heat dissipation.

Figure 8 show vertical structure of SPM 3 package and *Figure 9 ~ Figure 12* shows the package outline regarding isolation distance.

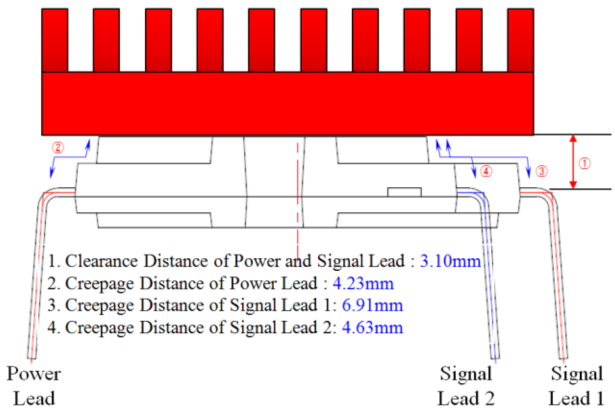


Figure 9. Isolation Distance between Heatsink and Pins

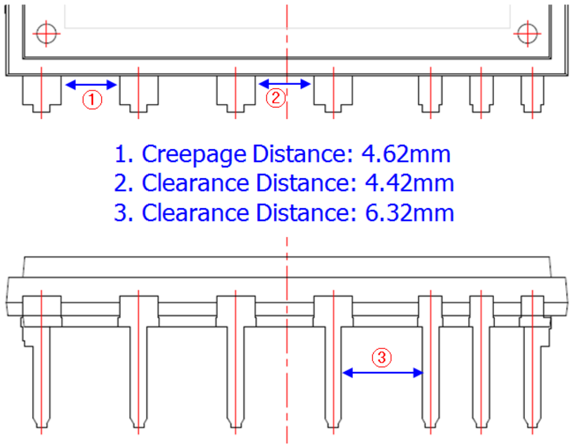


Figure 10. Isolation Distance between Power Pins

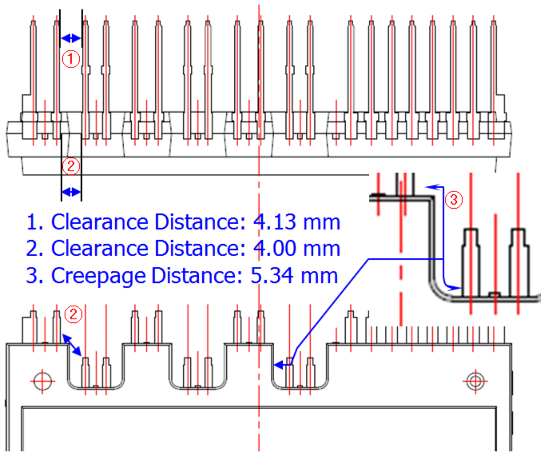


Figure 12. Isolation Distance between Signal Pins and High Potential Pins

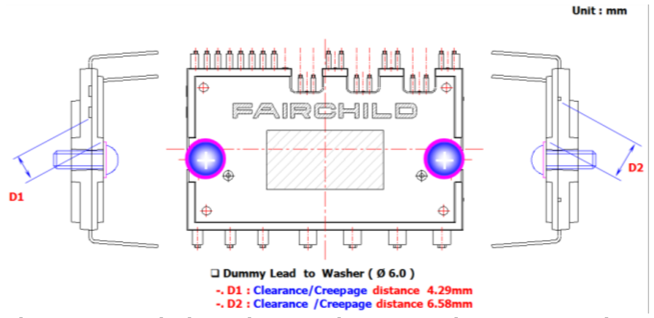


Figure 11. Isolation Distance between Live Dummy Pins and Mounting Screw

Table 10. Mechanical Characteristics and Ratings

Parameter	Conditions		Value			Unit
			Min.	Typ.	Max.	
Device Flatness	*See Figure 13*		0		+150	µm
Mounting Torque	Mounting Screw: M3	Recommended 0.7 N·m	0.6	0.7	0.8	N·m
		Recommended 7.1 kg·cm	6.2	7.1	8.1	kg·cm
Terminal Pulling Strength	Load 19.6 N		10			s
Terminal Bending Strength	Load 9.8 N, 90° Bend		2			Times
Weight				15		g

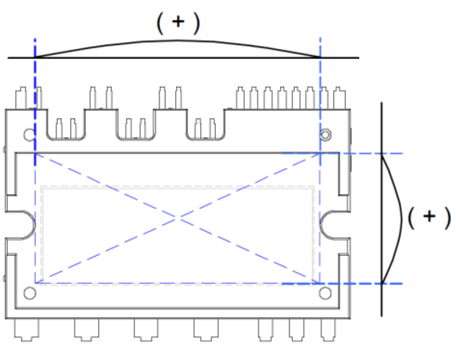


Figure 13. Flatness Measurement Position

3.1 Thermal Impedance

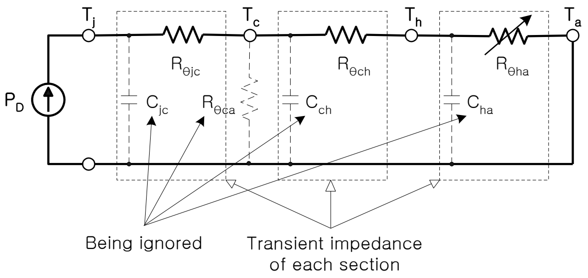


Figure 14. Transient Thermal Equivalent Circuit with a Heatsink

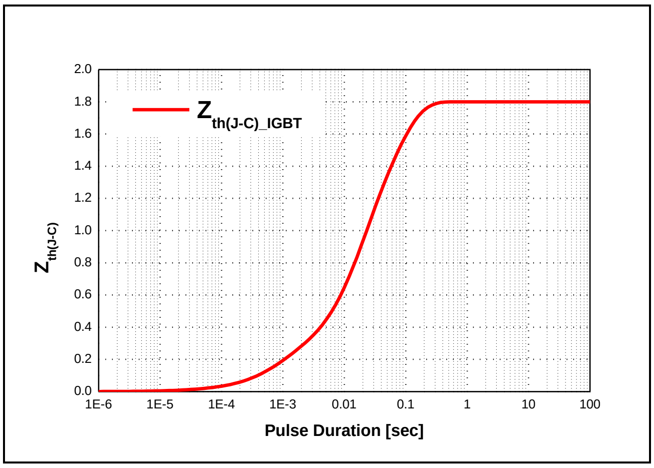
Figure 14 shows the thermal equivalent circuit of a SPM® package mounted on a heatsink. For sustained power dissipation P_D at the junction, the junction temperature T_j can be calculated as;

$$T_j = P_D(R_{\theta jc} + R_{\theta ch} + R_{\theta ha}) + T_a \quad (1)$$

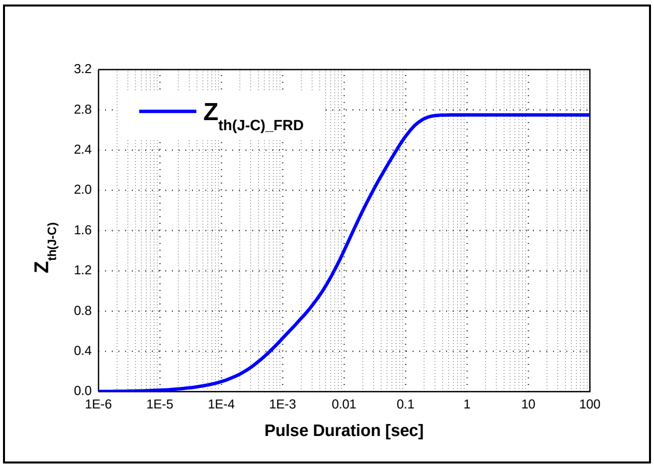
Where T_a is the ambient temperature and $R_{\theta jc}$, $R_{\theta ch}$, and $R_{\theta ha}$ represent the thermal resistance from the junction-to-case, case-to-heat sink, and the heat sink-to-ambient for each IGBT and diode within the SPM packages, respectively. Referencing *Figure 14*, the dotted component of $R_{\theta ca}$ can be ignored due to its large value.

From equation (1), it is evident that for a limited T_{jmax} (150°C). P_D can be increased by reducing $R_{\theta ha}$. This means that a more efficient cooling system will increase the power dissipation capability of SPM packages. An infinite heat sink will result if $R_{\theta ch}$ and $R_{\theta ha}$ are reduced to zero and the case temperature T_c is locked at the fixed ambient temperature T_a.

In practical operation, the power loss P_D is cyclic and therfore the transient RC equivalent circuit shown in *Figure 14* should be considered. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature, and thus permits a heavier loading of the SPM package. *Figure 15* shows thermal impedance curves of FSBB10CH120D. The thermal resistance goes into saturation in about 10 seconds. Other kind of SPM packages also shows similar characteristics.



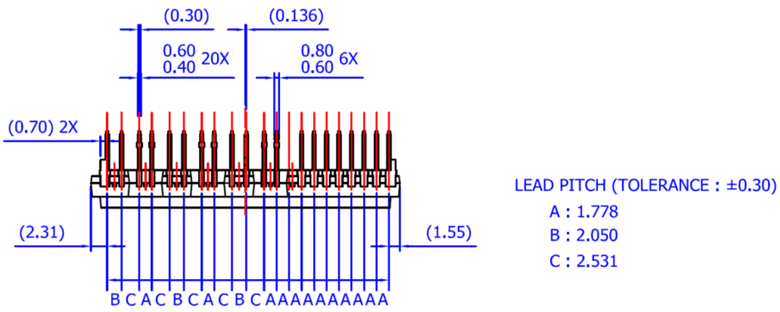
(1) Thermal Impedance Graph of IGBT

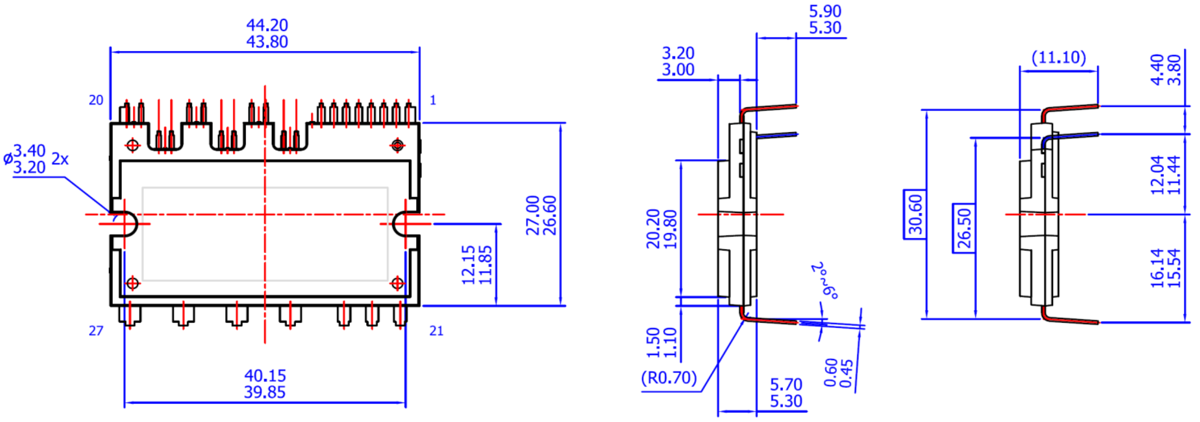


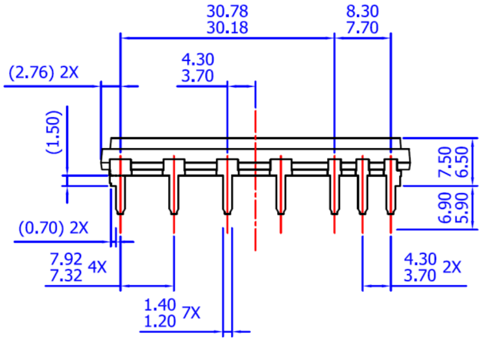
(2) Thermal Impedance Graph of FRD

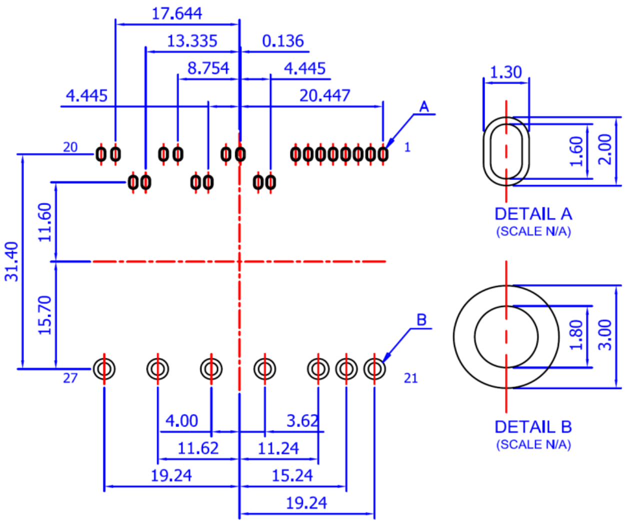
Figure 15. Thermal Impedance Graphs (FSBB10CH120D)

3.2 Detailed Package Outline Drawings





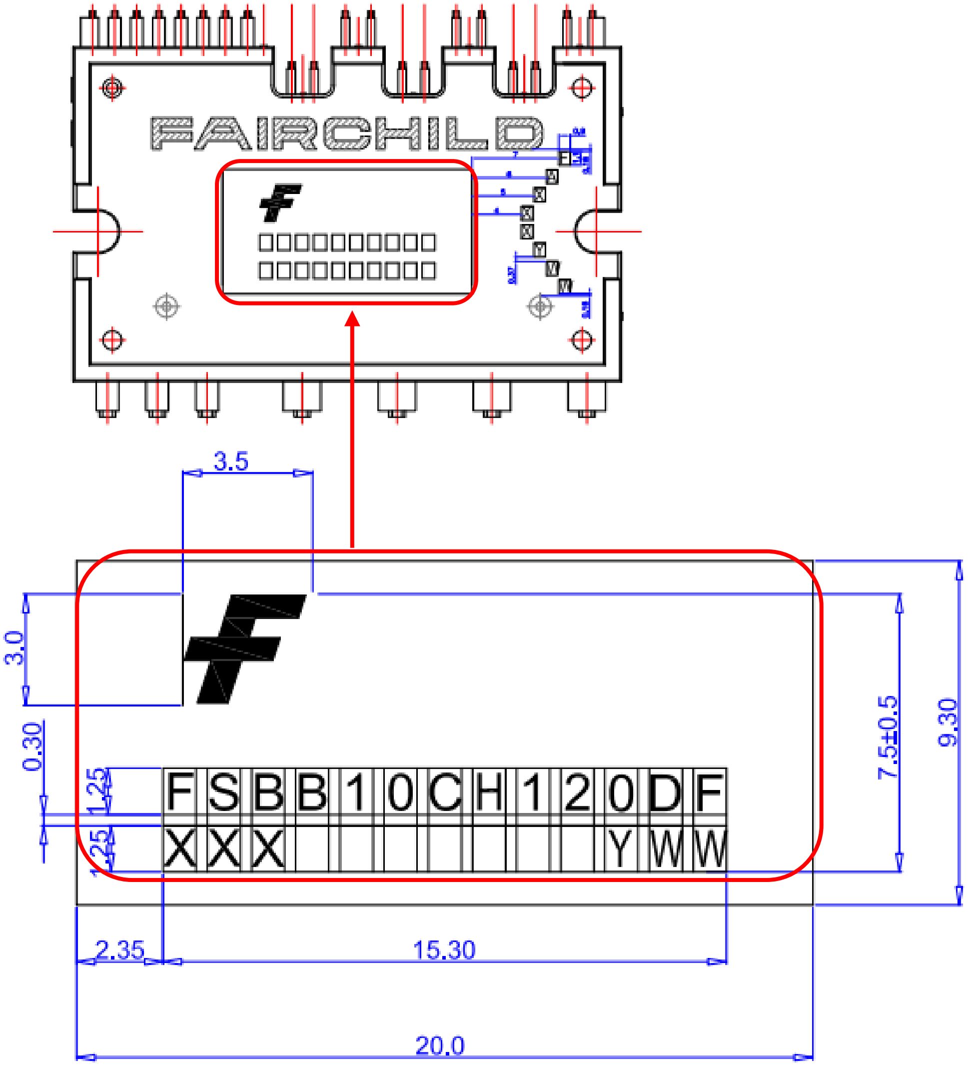




LAND PATTERN RECOMMENDATIONS

NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
- B) ALL DIMENSIONS ARE IN MILLIMETERS
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D) ( ) IS REFERENCE
- E) [ ] IS ASS'Y QUALITY
- F) DRAWING FILENAME: MOD27BCREV2.0
- G) FAIRCHILD SEMICONDUCTOR

3.3 Marking Information



* NOTE

1. F : FAIRCHILD LOGO(STYLE & SIZE : SEE SPEC BD2249)
2. XXX : LAST 3 DIGITS OF LOT NO(OPTION CODE)
3. YWW : WORK WEEK CODE ("Y" REFERS TO THE RIGHT ALPHABET CHARACTER TABLE)
4. Hole Side Marking :
   -.FA :FSBB10CH120DF(Product name)
   -. XXX : Last 3 digits of Lot No.
   -. YWW : Work Week Code("Y" Refers to the right alphabet character table)

X	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

Figure 16. Marking Information

4 Operating Sequence for Protections

4.1 Short-Circuit Current Protection (SCP)

Motion SPM® 3 module uses a shunt resistor for the short circuit current detection, as shown in *Figure 17*. LVIC has a built-in short-circuit current protection function. This protection function senses the voltage to the CSC pin. If this voltage exceeds the $V_{SC(ref)}$ (the threshold voltage trip level of the short-circuit) specified in the device datasheets ($V_{SC(ref)}$, typ. is 0.5 V), a fault signal is asserted and the all low side IGBTs are turned off. Typically, the maximum short-circuit current magnitude is gate-voltage dependent: higher gate voltage (V_{CC} & V_{BS}) results in larger short-circuit current. To avoid potential problems, the maximum short-circuit trip level is set below 1.7 times the nominal rated collector current. The LVIC short-circuit current protection-timing chart is shown in *Figure 18*.

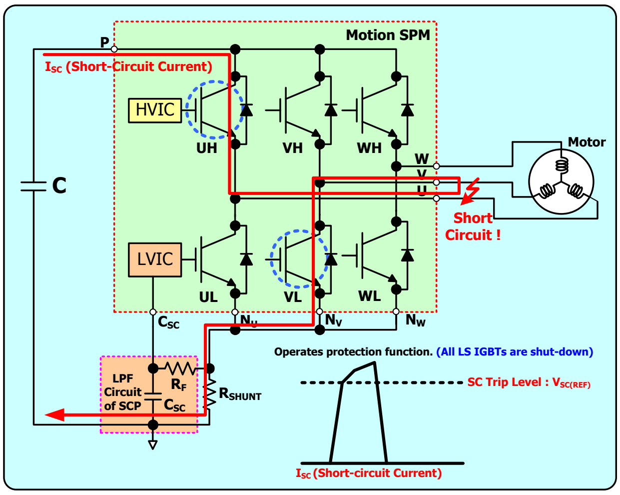


Figure 17. Operation of Short-Circuit Current Protection

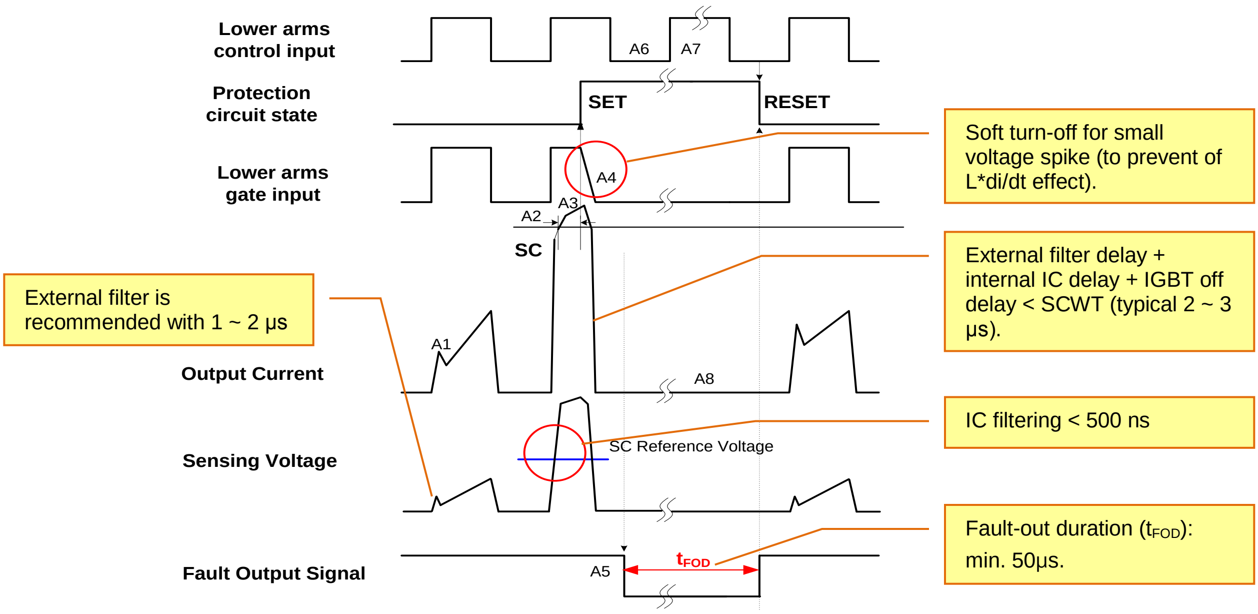


Figure 18. Timing Chart of Short-Circuit Current Protection Function

Notes:

7. A1-normal operation: IGBT on and carrying current.
8. A2-short-circuit current detection (SC trigger).
9. A3-hard IGBT gate interrupt.
10. A4-IGBT turns OFF by soft-off function.
11. A5-fault output timer operation start with internal delay (typ. 3.0 μs), t_{FOD}=min. 50 μs.
12. A6-input “L”: IGBT OFF state.
13. A7-input “H”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON.
14. A8-IGBT keeps OFF state.

4.2 Under-Voltage Lockout Protection

The LVIC has an under-voltage lockout protection (UVLO) function to protect the low-side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in *Figure 19*.

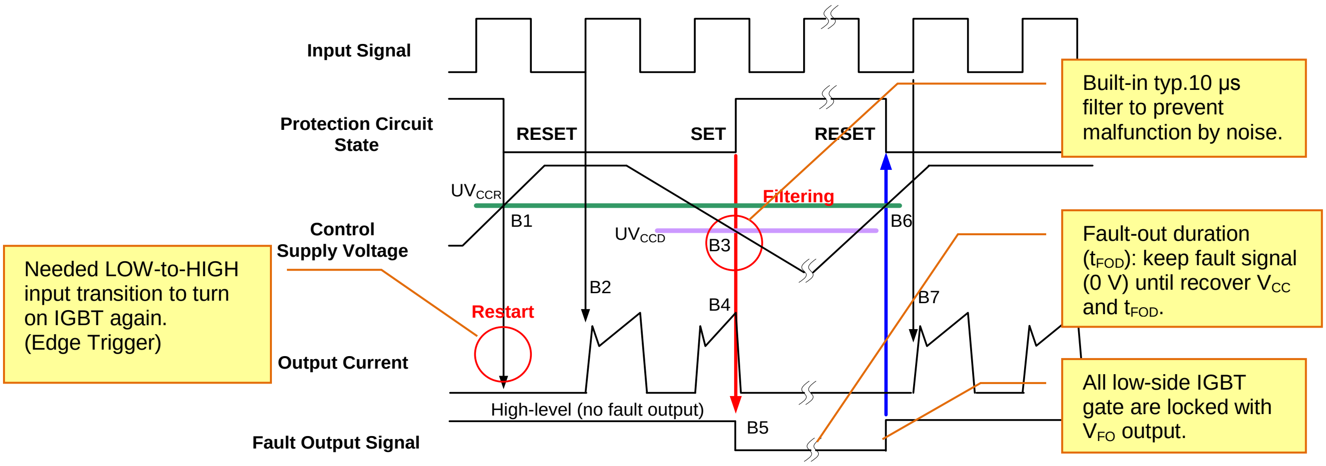


Figure 19. Timing Chart of Low-Side Under-Voltage Protection Function

Notes:

15. B1-control supply voltage rise: after the voltage rises UV_{CCR}, the circuits starts to operate when the next input is applied.
16. B2-normal operation: IGBT ON and carrying current.
17. B3-under-voltage detection (UV_{CCD}).
18. B4-IGBT OFF in spite of control input is alive.
19. B5-fault output signal starts.
20. B6-under-voltage reset (UV_{CCR}).
21. B7-normal operation: IGBT ON and carrying current. If fault-out duration (t_{FOD}=min.50µs) is longer than UV_{CCR} timing, fault output and IGBT state are cleared after t_{FOD}.

The HVIC has an under-voltage lockout function to protect the high-side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in *Figure 20*. A fault-out (FO) alarm is not given for low HVIC bias conditions.

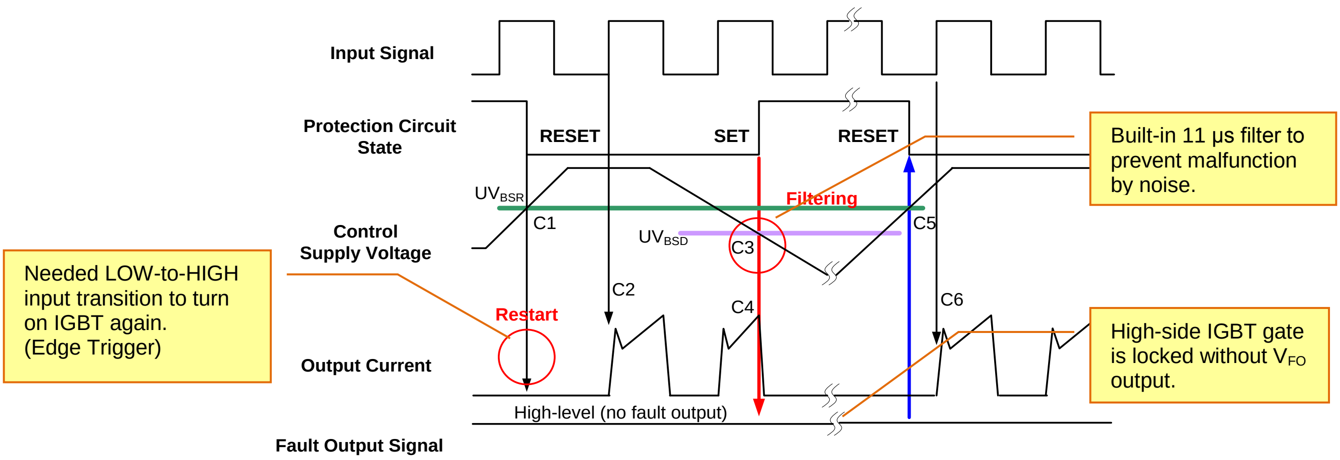


Figure 20. Timing Chart of High-Side Under-Voltage Protection Function

Notes:

22. C1-control supply voltage rises: after the voltage reaches UV_{BSR}, the circuit starts when the next input is applied.
23. C2-normal operation: IGBT ON and carrying current.
24. C3-under-voltage detection (UV_{BSD}).
25. C4-IGBT OFF in spite of control input is alive, but there is no fault output signal.
26. C5-under-voltage reset (UV_{BSR}).
27. C6-normal operation: IGBT ON and carrying current.

5 Key Parameter Design Guidance

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of Motion SPM® 3 module.

5.1 Shunt Resistor Selection at N-Terminal for Current Sensing & Protection

Figure 21 shows a recommended circuitry for over-current & short-circuit protection. The external RC time constant from the N-terminal shunt resistor to CSC must be lower than 2 µs when over load condition is detected for a stable shutdown.

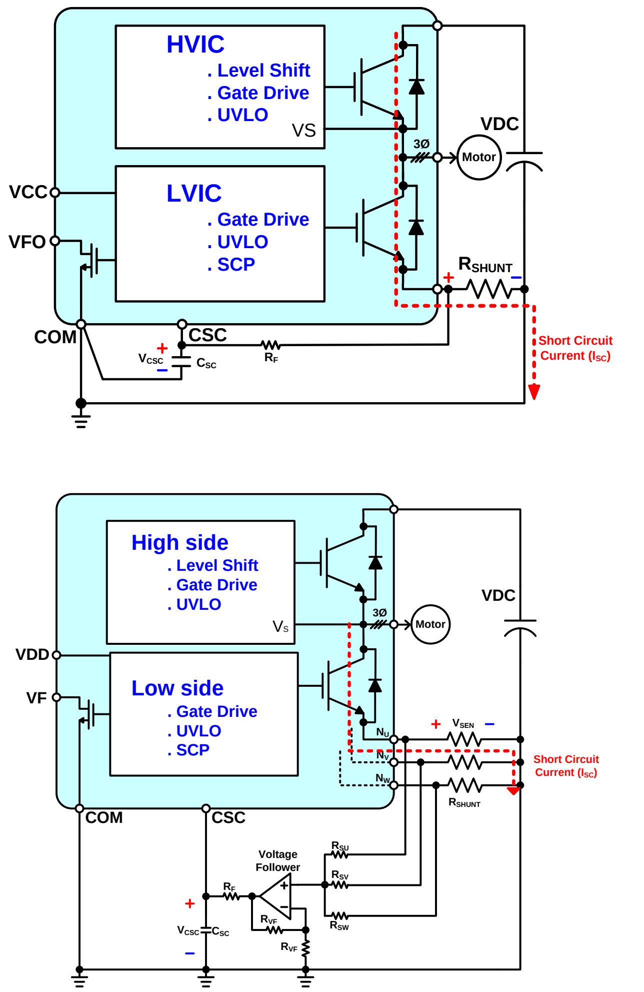


Figure 21. Recommended Circuitry for Over-Current & Short-Circuit Protection

Table 11. OCP & SCP Level ($V_{SC(ref)}$) Specification

Conditions	Min.	Typ.	Max.	Unit
Specification at T_J=25°C, V_{CC}=15 V	0.45	0.50	0.55	V

Table 12. Operating Short-Circuit Current Range (R_{SHUNT}=24.4 mΩ (Min.), 25.7 mΩ (Typ.), 27 mΩ (Max.)) *(see the equations below)*

Conditions	Min.	Typ.	Max.	Unit
Operating SC Level at T_J=25°C	16	19.5	22.5	A

(Table 11 and 12 are based on FSBB15CH120DF)

In case of one shunt, the value of shunt resistor is calculated by the following equations.

Maximum current trip level (depend on user selection):

$$I_{SC(max)} = 1.5 \times I_{C(max)}$$

SC trip reference voltage (depends on datasheet):

$$V_{SC(ref)} = \text{min. } 0.45V, \text{ typ. } 0.5V, \text{ max. } 0.55V$$

Shunt resistance:

$$I_{SC(max)} = V_{SC(max)} / R_{SHUNT(min)} \rightarrow R_{SHUNT(min)} = V_{SC(max)} / I_{SC(max)}$$

If the deviation of the shunt resistor is limited below ± 5%:

$$R_{SHUNT(typ)} = R_{SHUNT(min)} / 0.95,$$

$$R_{SHUNT(max)} = R_{SHUNT(typ)} \times 1.05$$

Actual SC trip current level becomes:

$$I_{SC(typ)} = V_{SC(typ)} / R_{SHUNT(typ)}, \; I_{SC(min)} = V_{SC(min)} / R_{SHUNT(max)}$$

Inverter output power:

$$V_{O,LL} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{V_{DC\_Link}}{2}$$

$$P_{OUT} = \sqrt{3} \times V_{O,LL} \times I_{RMS} \times PF$$

where:

$V_{O,LL}$ = *Inverter Output Voltage between line to line;*

MI = *Modulation Index*

I_{RMS} = *Maximum load current of inverter; and*

PF = *Power Factor*

Average DC current

$$I_{DC\_AVG} = (P_{out} \times Eff) / V_{DC\_Link}$$

where:

Eff = *Inverter efficiency*

The power rating of shunt resistor is calculated by the following equation:

$$P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times Margin) / Derating\ Ratio$$

where:

R_{SHUNT}=Shunt resistor typical value at T_C=25°C

Derating Ratio=Derating ratio of shunt resistor at T_{SHUNT}=100°C

(From datasheet of shunt resistor); and

Margin = Safety margin (determined by user)

✓ Shunt Resistor Calculation Examples

Calculation Conditions:

- DUT: FSBB15CH120DF
- Tolerance of shunt resistor: ±5%
- SC Trip Reference Voltage:

  $V_{SC(min)}$ = 0.45 V, $V_{SC(typ)}$ = 0.50 V, $V_{SC(max)}$ = 0.55 V
- Maximum Load Current of Inverter (I_{RMS}): 7.5 A_{rms}
- Maximum Peak Load Current of Inverter ($I_{C(max)}$): 10 A
- Modulation Index(MI) : 0.9
- DC Link Voltage(V_{DC_Link}): 600 V
- Power Factor(PF): 0.8
- Inverter Efficiency(Eff): 0.95
- Shunt Resistor Value at T_C = 25°C (R_{SHUNT}): 25.7 mΩ
- Derating Ratio of Shunt Resistor at T_{SHUNT}=100°C: 70%
- Safety Margin: 20%

Calculation Results:

- $I_{SC(max)}$: 1.5 × $I_{C(max)}$ = 1.5 x 15 A = 22.5 A
- $R_{SHUNT(min)}$: $V_{SC(max)}$ / $I_{SC(max)}$ = 0.55 V / 22.5 A = 24.4 mΩ
- $R_{SHUNT(typ)}$: $R_{SHUNT(min)}$ / 0.95 = 24.4 mΩ / 0.95 = 25.7 mΩ
- $R_{SHUNT(max)}$: $R_{SHUNT(typ)}$ x 1.05 = 25.7 mΩ x 1.05 = 27 mΩ
- $I_{SC(min)}$: $V_{SC(min)}$ / $R_{SHUNT(max)}$ = 0.45 V / 27 mΩ = 16.6 A
- $I_{SC(typ)}$: $V_{SC(typ)}$ / $R_{SHUNT(typ)}$ = 0.5 V / 25.7 mΩ = 19.5 A
- $V_{O,LL} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{V_{DC\_Link}}{2} = \frac{\sqrt{3}}{\sqrt{2}} \times 0.9 \times 300 = 330.7$ V
- $P_{OUT} = \sqrt{3} \times V_{O,LL} \times I_{RMS} \times PF = 3437$ W
- I_{DC_AVG} = (P_{OUT}/Eff) / V_{DC_Link} = 6.03 A
- P_{SHUNT} = ($I^2_{DC\_AVG}$ × R_{SHUNT} × Margin) / Derating Ratio

  = (6.03^2 × 0.0257 × 1.2) / 0.7 = 1.6 W (Therefore, the proper power rating of shunt resistor is over 2 W)

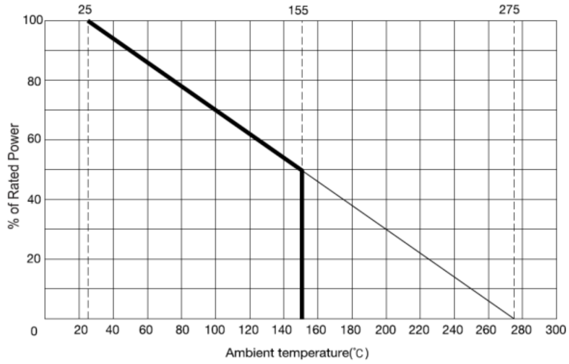


Figure 22. Derating Curve Example of Shunt Resistor (from RARA Elec.)

5.2 Time Constant of Internal Delay

Figure 23 is timing diagram of 1200V Motion SPM 3 module for Short-Circuit Protection (SCP) circuit operation. An RC filter is prevents noise-related SCP circuit malfunction. The RC time constant is determined by the applied noise time and the Short-Circuit Withstanding Time (SCWT) of Motion SPM 3 module. When the V_{CSC} voltage exceeds the SCP level, this is applied to the CSC pin via the RC filter. The RC filter delay (T1) is the time required for the CSC pin voltage to rise to the referenced SCP level. The LVIC has an internal filter time (logic filter time for noise elimination: T2). Consider this filter time when designing the RC filter of V_{CSC}.

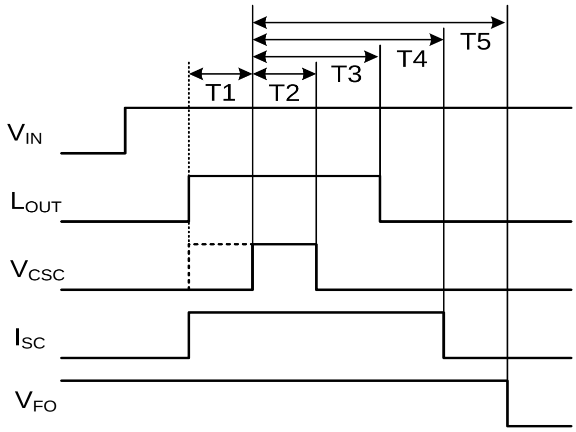


Figure 23. Timing Diagram

Notes:

28. V_{IN}: Voltage of input signal.
29. L_{OUT}: V_{GE} of low-side IGBT.
30. V_{CSC}: Voltage of CSC pin.
31. I_{SC}: Short-circuit current.
32. V_{FO}: Voltage of VFO pin.
33. T1: filtering time of RC filter of V_{CSC}.
34. T2: filtering time of CSC. If V_{CSC} width is less than T2, SCP does not operate.
35. T3: delay from CSC triggering to gate-voltage down.
36. T4: delay from CSC triggering to short-circuit current.
37. T5: delay from CSC triggering to fault-out signal.

Table 13. Time Table on Short-Circuit Conditions: V_{CSC} to L_{OUT}, I_{SC}, V_{FO}

Device Under Test	Typ. at T_J=25°C	Typ. at T_J=150°C	Max. at T_J=25°C
FSBB10CH120D FSBB10CH120DF	T2=0.25 µs	T2=0.09 µs	Considering ±20% Dispersion, T4=3.6 µs
	T3=0.62 µs	T3=0.57 µs	
	T4=3 µs	T4=3.3 µs	
	T5=4.1 µs	T5=4.25 µs	

Note:

38. To guarantee safe short-circuit protection under all operating conditions, C_{SC} should be triggered within 1.0 µs after short-circuit occurs. (Recommendation: SCWT < 5.0 µs, Conditions: V_{DC}=800 V, V_{CC}=16.5 V, T_J=150°C).

It is recommended that delay from short-circuit to CSC triggering should be minimized

5.3 Soft Turn-Off

An LVIC soft turn-off function protects the low side IGBTs from over voltage of V_{PN} (supply voltage) by “short-circuit hard off,” which is when IGBTs are turned off by short input signal before the SCP function under short-circuit condition. In this case, V_{PN} rapidly rises by fast and big di/dt of I_{SC} (short-circuit current). This kind of rapid rise of V_{PN} can cause destruction of IGBT by over-voltage. Therefore, soft-off function prevents IGBT rapid turning off by slow discharging of V_{GE} (gate-to-emitter voltage of IGBT).

An internal block diagram of LVIC and operation sequence of soft turn-off function is shown in *Figure 24* and *Figure 25*. This function operates by two internal protection functions (UVLO and SCP). When the IGBT is turned off in normal conditions, LVIC turns off the IGBT immediately by turn-off gate signal (IN(xL)) via gate driver block. Pre-driver turn-on output buffer of gate driver block, path ①. When the IGBT is turned off by a protection function, the gate driver is disabled by the protection function signal via output of protection circuit (disable output buffer, high-Z) and output of the protection circuit turn-on switch of the soft-off function. V_{GE} (IGBT gate-emitter voltage) is discharged slowly via circuit of soft-off (path ②).

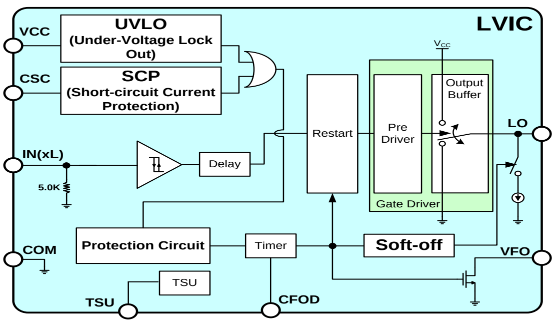


Figure 24. Internal Block Diagram of LVIC

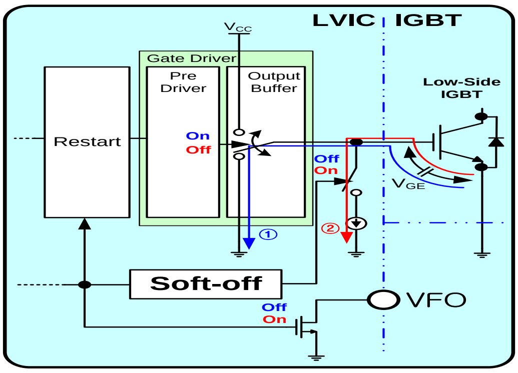


Figure 25. Operating Sequence of Soft Turn-Off

Figure 26 and *Figure 27* show normal turn-off switching operations performed satisfactorily at a V_{DC}=800 V with the surge voltage between the P and N pins ($V_{PN(Surge)}$) limited to under 1000 V. The difference between the hard and soft turn-off switching operation is also shown in *Figure 26* and *Figure 27*. The hard turn-off of the IGBT creates a large overshoot (155 V). The DC-link capacitor supply voltage should be limited to 800 V to safely protect the 1200 V Motion SPM 3. A hard turn-off, with a duration of less than 2 µs, may occur in the case of a short-circuit fault. For a normal short-circuit fault, the protection circuit becomes active and the IGBT is turned off softly to prevent excessive overshoot voltage. An overshoot voltage of <100 V occurs in this condition.

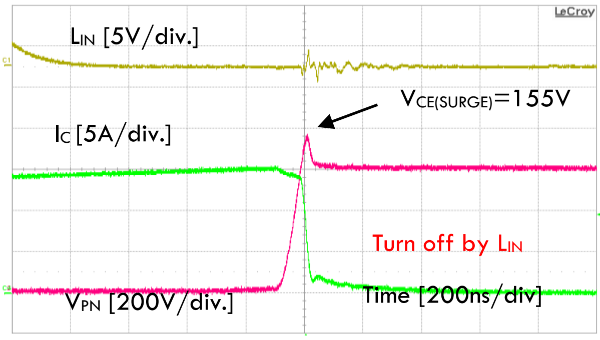


Figure 26. Turn-Off by Input (FSBB10CH120D, Ref. Condition: V_{DC}=600 V, T_J=25°C)

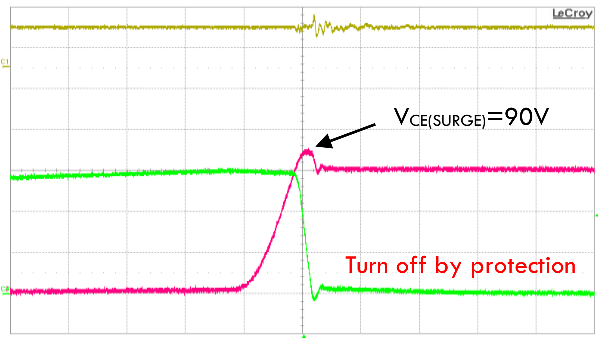


Figure 27. Turn-Off by Soft Off Function (FSBB10CH120D, Ref. Condition: V_{DC}=800 V, T_J=25°C)

5.4 Fault Output Circuit

Table 14. Fault-Output Maximum Ratings

Symbol	Item	Condition	Rating	Unit
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO}-COM	-0.3 ~ V_{CC}+0.3	V
I_{FO}	Fault Output Current	Sink Current at VFO Pin	2	mA

Table 15. Electric Characteristics

Symbol	Item	Conditions	Min.	Max.	Unit
V_{FOH}	Fault Output Supply Voltage	V_{CC}=15 V, V_{SC}=0, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-Up	4.5		V
V_{FOL}		V_{CC}=15 V, V_{SC}=1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-Up		0.5	V

Because V_{FO} terminal is an open-drain type; it should be pulled up via a pull-up resistor. The resistor must satisfy the above specifications.

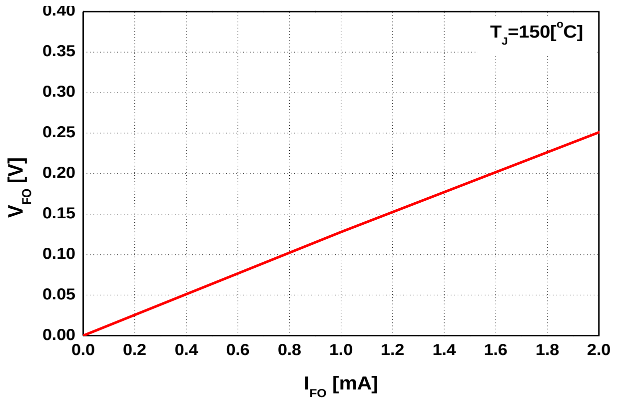


Figure 28. Voltage-Current Characteristics of V_{FO} Terminal

5.5 Circuit of Input Signal (IN(xH), IN(xL))

Figure 29 shows the I/O interface circuit between the MCU and Motion SPM 3 product. Because the Motion SPM 3 product input logic is active HIGH and there are built-in pull-down resistors, external pull-down resistors are not needed.

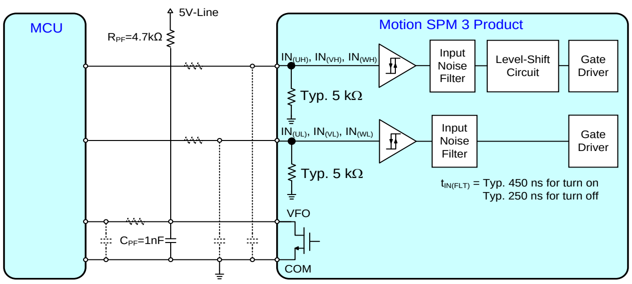


Figure 29. Recommended MCU I/O Interface Circuit

The input and fault output maximum rated voltages are shown in *Table 16*. Since the fault output is open drain, its rating is VCC+0.3 V, 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the de-coupling capacitors be placed at both the MCU and Motion SPM 3 product ends of the V_{FO} signal line, as close as possible to each device. The RC coupling at each input (parts shown dotted in *Figure 29*) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the 1200 V Motion SPM 3 module integrates a 5 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM 3 series input, attention should be given to the signal voltage drop at the SPM 3 module input terminals to satisfy the turn-on threshold voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown dotted in *Figure 29*.

Table 16. Maximum Ratings of Input and VFO Pins

Symbol	Item	Condition	Rating	Unit
V_{IN}	Input Signal Voltage	Applied between $IN_{(xH)}$, $IN_{(xL)}$ - COM(x)	-0.3 ~ V_{CC} +0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO}-COM(L)	-0.3 ~ V_{CC} +0.3	V

Table 17. Input Threshold Voltage Ratings (V_{CC}=15 V, T_J=25°C)

Symbol	Item	Condition	Min.	Max.	Unit
$V_{IN(ON)}$	Turn-On Threshold Voltage	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - COM(H)		2.6	V
$V_{IN(OFF)}$	Turn-Off Threshold Voltage	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM(L)	0.8		V

5.6 Bootstrap Circuit Design

5.6.1 Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between V_B (U, V, W) and V_S (U, V, W), provides the supply to the HVIC within the Motion SPM 3 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high-side IGBT. The under-voltage lockout protection for V_{BS} ensures that the HVIC does not drive the high-side IGBT if the V_{BS} voltage drops below a specific voltage (*refer to the datasheet*). This function prevents the IGBT from operating in a high-dissipation mode.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here (refer to *Figure 30*). This method has the advantage of being simple and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of a bootstrap diode, resistor, and the current flow path of the bootstrap circuit is shown in *Figure 30*. When V_S is pulled down to ground (low-side IGBT turn-on or low-side FRD freewheeling), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply.

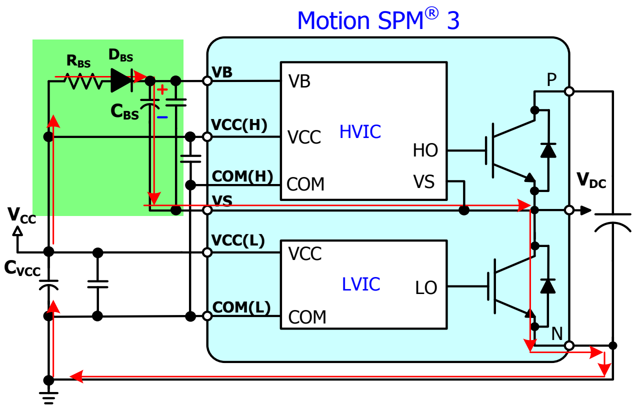


Figure 30. Current Path of Bootstrap Circuit for the Supply Voltage (V_{BS}) of a HVIC when Low-Side IGBT Turns On

5.6.2 Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on-time of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln \frac{V_{CC}}{V_{CC} - V_{BS(min)} - V_F - V_{LS}} \qquad (2)$$

where:

V_F = Forward voltage drop across the bootstrap diode;

$V_{BS(min)}$ = The minimum value of the bootstrap voltage;

C_{BS} = Value of the bootstrap capacitor;

V_{LS} = Voltage drop across the low-side IGBT or load; and

δ = Duty ratio of PWM (0 ~ 1).

When the bootstrap capacitor is charged initially; V_{CC} drop voltage is generated based on initial charging method, V_{CC} line SMPS output current, V_{CC} source capacitance, and bootstrap capacitance. If V_{CC} drop voltage reaches UV_{CCD} level, the low side is shut down and a fault signal is activated. To avoid this malfunction, related parameter and initial charging method should be considered. To reduce V_{CC} voltage drop at initial charging, a large V_{CC} source capacitor and selection of optimized low-side turn-on method are recommended. Adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts.

Figure 31 shows an example of initial bootstrap charging sequence. Once V_{CC} establishes, V_{BS} needs to be charged by turning on the low-side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency. Therefore, it is desired to maintain this structure without creating complementary high-side PWM signals. The capacitance of V_{CC} should be sufficient to supply necessary charge to V_{BS} capacitance in all three phases. If a normal PWM operation starts before V_{BS} reaches V_{UVLO} reset level, the high-side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over-current protection level. Therefore, initial charging time for bootstrap capacitors should be separated, as shown in *Figure 32*. The effect of the bootstrap capacitance factor and charging method (low-side IGBT driving method) is shown in *Figure 33*.

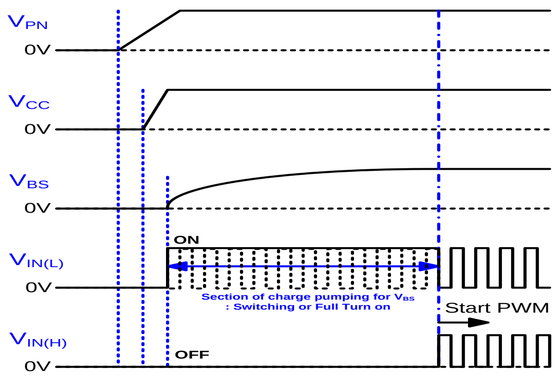


Figure 31. Timing Chart of Initial Bootstrap Charging

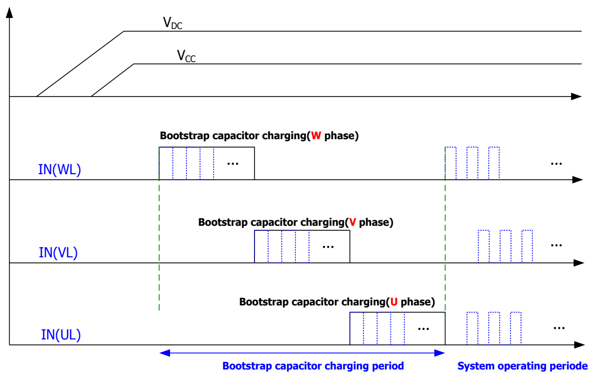


Figure 32. Recommended Initial Bootstrap Capacitors Charging Sequence

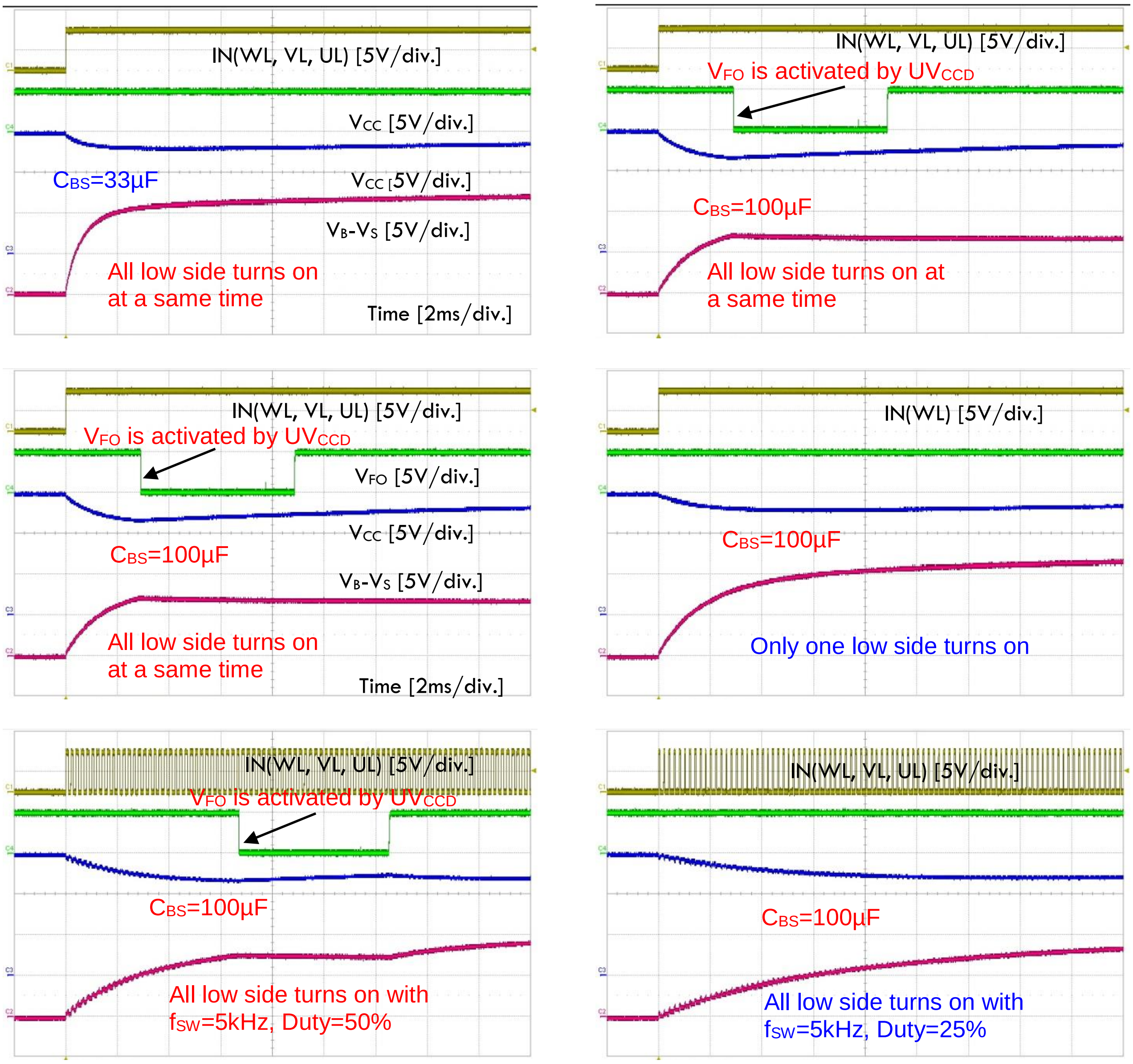


Figure 33.Initial Charging According to Bootstrap Capacitance and Charging Method
(Ref. Condition: V_{CC}=15 V/300 mA, V_{CC} Capacitor=220 µF, Bootstrap Capacitor=100 µF, R_{BS}=20 Ω)

5.6.3 Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} \quad (3)$$

where:
Δt: maximum on pulse width of high-side IGBT;
ΔV_{BS}: the allowable discharge voltage of the C_{BS} (voltage ripple); and
I_{Leak}: maximum discharge current of the C_{BS}.

Mainly via the following mechanisms:

- Gate charge for turning the high-side IGBT on
- Quiescent current to the high-side circuit in HVIC
- Level-shift charge required by level-shifters in HVIC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
- Bootstrap diode reverse recovery charge

Practically, 4.5 mA of I_{Leak} is recommended for the Motion SPM 3 products.(Refer to I_{PBS} value in datasheet) By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the $V_{S(x)}$ voltage is pulled down to ground.

The on-time of the low-side IGBT must be sufficient to for the charge drawn from the C_{BS} capacitor to be fully replenished. This creates an inherent minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).

Calculation Examples of Bootstrap Capacitance A

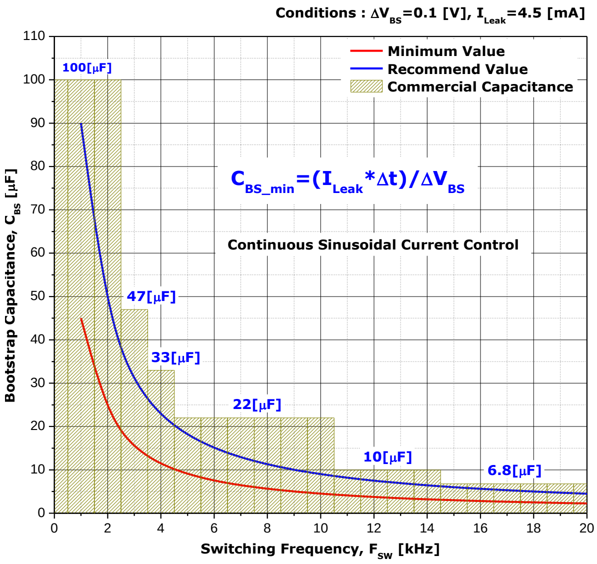


Figure 34. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔV_{BS}

- I_{Leak}: circuit current = 4.5 mA (recommended value)
- ΔV_{BS}: discharged voltage = 0.1 V (recommended value)
- Δt: maximum on pulse width of high-side IGBT = 0.2 ms (depends on application)

$$C_{BS\_min} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} = \frac{4.5\text{mA} \times 0.2\text{ms}}{0.1\text{V}} = 9.0 \times 10^{-6} \quad (4)$$

→ More than 2 times
→ 18 μF (22 μF STD value)

Note:
39. The capacitance value can be changed according to the switching frequency, the capacitor selected, and the recommended V_{BS} voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of the component.

Calculation Examples of Bootstrap Capacitance B

Based on operating conditions, UV_{BS} function, and allowable recommended $V_{B(x)}$-$V_{S(x)}$

To avoid unexpected under-voltage protection and to keep V_{BS} within recommended value, bootstrap capacitance should be selected based on the operating conditions. Bootstrap voltage ripple is influenced by bootstrap resistor, load condition, output frequency, and switching frequency. Check the bootstrap voltage under the maximum load condition in the system. *Figure 35* shows example of $V_{B(x)}$-$V_{S(x)}$ ripple voltage during operation.

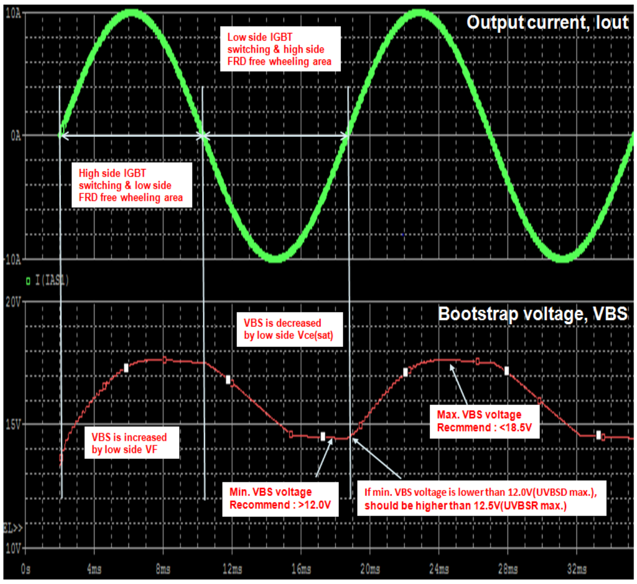


Figure 35. Recommendation of Bootstrap Ripple Voltage during Operation

5.6.4 Selection of Bootstrap Diode

When high side IGBT or diode conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage. A withstand voltage higher than 1200 V is recommended. It is important that the diode should be a fast recovery (recovery time < 100 ns) device to minimize the amount of charge that is fed back from the bootstrap capacitor into the V_{CC} supply. Similarly, the high voltage reverse leakage current is important if the capacitor has to store a charge for long periods of time. Recommended diodes are as below.

- STM: STTH112(DO-41), STTH112U(SMB)
- Vishay: EGF1T(DO-214BA), SF1200(SOD-57)

5.6.5 Selection of Bootstrap Resistor

A resistor R_{BS} must be added in series with the bootstrap diode to slow down the dV_{BS}/dt and to limit inrush current at initial C_{BS} charging. It also determines the time to charge the bootstrap capacitor. That is, if the minimum ON pulse width of low-side IGBT or the minimum OFF pulse width of high-side IGBT is t_O, the bootstrap capacitor has to be charged ΔV during this period. Therefore, the value of bootstrap resistance can be calculated by the following equation.

$$R_{BS} = \frac{(V_{DD} - V_{BS}) \times t_O}{C_{BS} \times \Delta V_{BS}} \tag{5}$$

For the selection of R_{BS}, pulse power rating should be considered for initial charging of bootstrap capacitor. To use a large bootstrap capacitor, high pulse power rating is required for the bootstrap resistor. An example of resistor pulse power rating is shown in *Figure 36*.

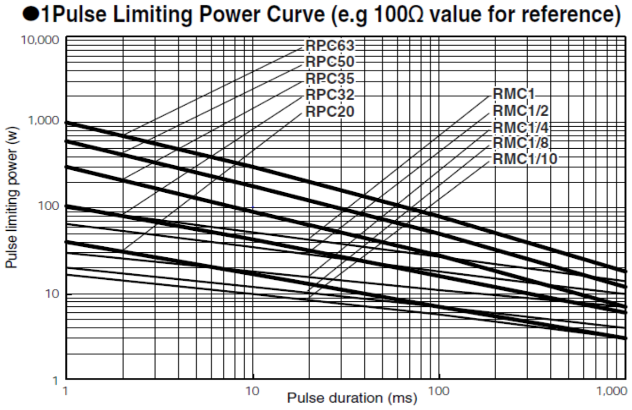


Figure 36. Example of Pulse Power Curve of Resistor (from KAMAYA OHM)

5.7 Thermal Sensing Unit (TSU)

The junction temperature of power devices should not exceed the maximum junction temperature. Even though there is some margin between the T_{jmax} specified on the datasheet and the T_{jmax} at which power devices are destroyed, attention should be paid to ensure the junction temperature stays well below the T_{jmax}. An NTC had to be mounted on the heat sink or very close to the module if over-temperature protection was required in the application.

5.7.1 Basic Concept

Thermal Sensing Unit (TSU) uses the technology based on the temperature dependency of transistor V_{BE}; V_{BE} decrease 2 mV as temperature increase 1ºC.

The TSU has analog voltage output reflects the temperature of the LVIC. The relationship between V_{TS} voltage output and LVIC temperature is shown in *Figure 38* and *Table 18* shows the raw data. Also, the TSU have 2 kind of temperature profile, one is 0 ~ 150ºC, another is -25 ~ 125 ºC. It does not have any self-protection function, and, therefore, it should be used appropriately based on application requirement. It should be noted that there is a time lag from IGBT temperature to LVIC temperature. So it is very difficult to respond quickly when temperature rises sharply in a transient condition such as shoot-through event. Even though TSU has some limitation, it will be definitely useful in enhancing the system reliability.

Figure 37 shows the LVIC location of FSBB10CH120DF.

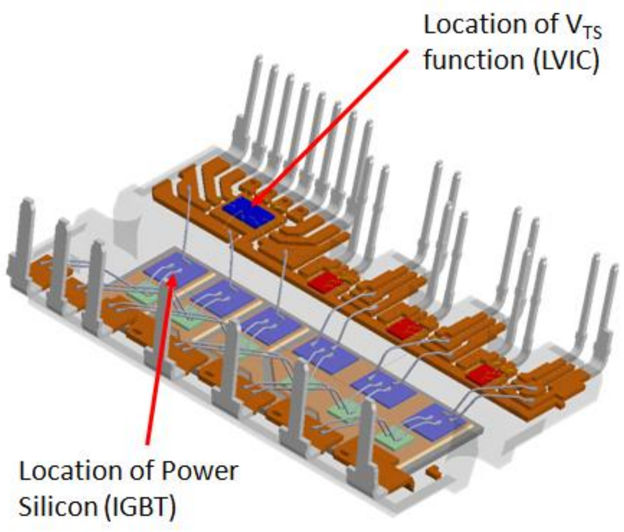
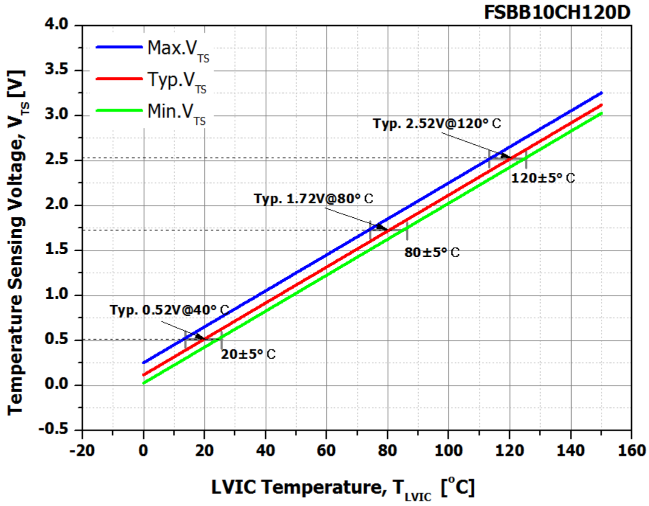
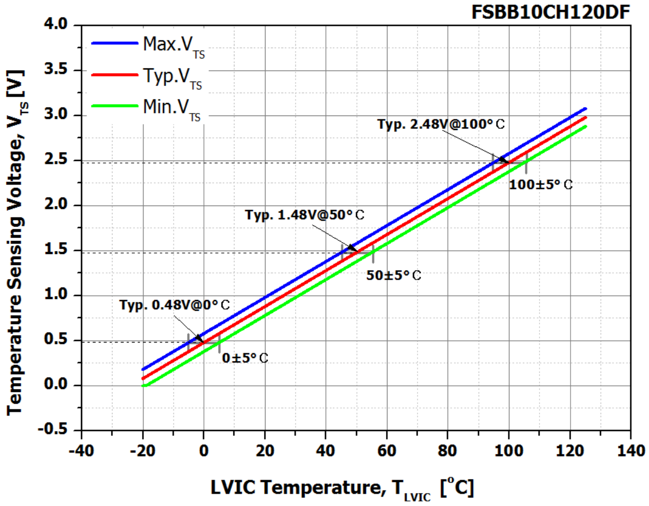


Figure 37. Location of V_{TS} Function (LVIC)



(a) FSBBxxCH120D



(b) FSBBxxCH120DF

Figure 38. LVIC Temperature vs. V_{TS} Graph

Figure 39 shows the equivalent circuit diagram of TSU inside IC and a typical application diagram. This output voltage is clamped to 5.2 V by an internal Zener diode, but in case the maximum input range of Analog to Digital converter of MCU is below 5.2 V, an external Zener diode should be inserted between an A/D input pin and the analog ground pin of MCU. An amplifier can be used to change the range of voltage input to the Analog to Digital converter to have better resolution of the temperature. It is recommended to add a ceramic capacitor of 1000 pF between V_{TS} and Com (Ground) to make the V_{TS} more stable.

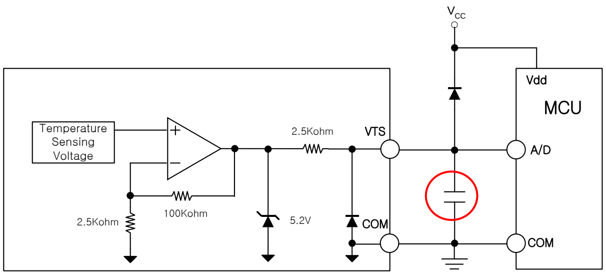
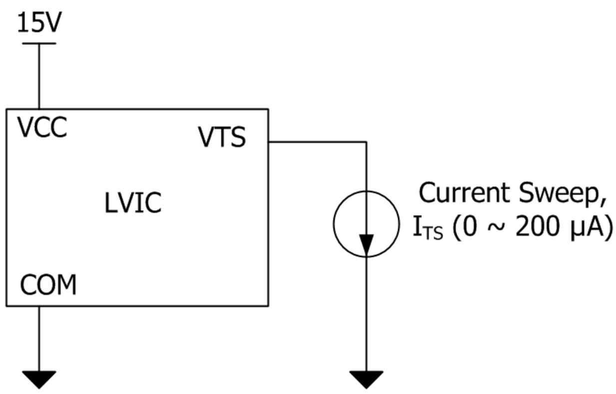
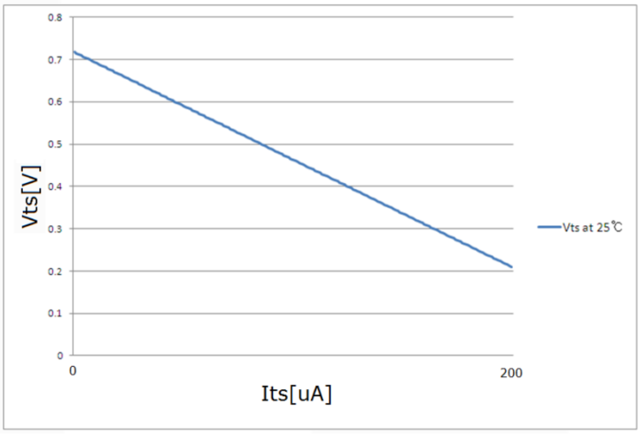


Figure 39. Internal Block Diagram and Interface Circuit of TSU



(a) Test Methods.



(b) Test Result

Figure 40. Load Variation of V_{TS}

Figure 40 shows the sourcing capability of V_{TS} pin at 25ºC and the test method. V_{TS} voltage decreases as the sourcing current increases. Therefore, the load connected to V_{TS} pin should be minimized to maintain the accurate voltage output level without degradation. The relationship between V_{TS} voltage and LVIC temperature can be expressed as the following equations.

[FSBB10CH120D]

$$VTS,min = 0.02*TLVIC + 0.140 - 0.100\ [V] \quad (6)$$

$$VTS,typ = 0.02*TLVIC + 0.140\ [V] \quad (7)$$

$$VTS,max = 0.02*TLVIC + 0.140 + 0.100\ [V] \quad (8)$$

[FSBBxxCH120DF]

$$V_{TS,min} = 0.02*T_{LVIC} + 0.480 - 0.100\ [V] \quad (9)$$

$$V_{TS,typ} = 0.02*T_{LVIC} + 0.480\ [V] \quad (10)$$

$$V_{TS,max} = 0.02*T_{LVIC} + 0.480 + 0.100\ [V] \quad (11)$$

The maximum variation of V_{TS} is ± 0.1 V due to process variation which is equivalent ±5ºC approximately. This is regardless of the temperature because the slopes of three lines are identical. If the ambient temperature information is available, for example, through NTC in the system, V_{TS} can be measured to adjust the offset before the motor starts to operate.

As temperature decrease further below 0ºC (-25ºC), V_{TS} decreases linearly until it reaches zero volts. If the temperature of LVIC increases above 150ºC (125ºC), which is above the maximum operating temperature, V_{TS} would increase theoretically up to 5.2 V until it gets clamped by the internal Zener diode.

Table 18. (a) V_{TS} Table of FSBB10CH120D

T [℃]	Min [V]	Typ [V]	Max [V]	T [℃]	Min [V]	Typ [V]	Max [V]	T [℃]	Min [V]	Typ [V]	Max [V]	T [℃]	Min [V]	Typ [V]	Max [V]
0	0.040	0.140	0.240	38	0.800	0.900	1.000	76	1.560	1.660	1.760	114	2.320	2.420	2.520
1	0.060	0.160	0.260	39	0.820	0.920	1.020	77	1.580	1.680	1.780	115	2.340	2.440	2.540
2	0.080	0.180	0.280	40	0.840	0.940	1.040	78	1.600	1.700	1.800	116	2.360	2.460	2.560
3	0.100	0.200	0.300	41	0.860	0.960	1.060	79	1.620	1.720	1.820	117	2.380	2.480	2.580
4	0.120	0.220	0.320	42	0.880	0.980	1.080	80	1.640	1.740	1.840	118	2.400	2.500	2.600
5	0.140	0.240	0.340	43	0.900	1.000	1.100	81	1.660	1.760	1.860	119	2.420	2.520	2.620
6	0.160	0.260	0.360	44	0.920	1.020	1.120	82	1.680	1.780	1.880	120	2.440	2.540	2.640
7	0.180	0.280	0.380	45	0.940	1.040	1.140	83	1.700	1.800	1.900	121	2.460	2.560	2.660
8	0.200	0.300	0.400	46	0.960	1.060	1.160	84	1.720	1.820	1.920	122	2.480	2.580	2.680
9	0.220	0.320	0.420	47	0.980	1.080	1.180	85	1.740	1.840	1.940	123	2.500	2.600	2.700
10	0.240	0.340	0.440	48	1.000	1.100	1.200	86	1.760	1.860	1.960	124	2.520	2.620	2.720
11	0.260	0.360	0.460	49	1.020	1.120	1.220	87	1.780	1.880	1.980	125	2.540	2.640	2.740
12	0.280	0.380	0.480	50	1.040	1.140	1.240	88	1.800	1.900	2.000	126	2.560	2.660	2.760
13	0.300	0.400	0.500	51	1.060	1.160	1.260	89	1.820	1.920	2.020	127	2.580	2.680	2.780
14	0.320	0.420	0.520	52	1.080	1.180	1.280	90	1.840	1.940	2.040	128	2.600	2.700	2.800
15	0.340	0.440	0.540	53	1.100	1.200	1.300	91	1.860	1.960	2.060	129	2.620	2.720	2.820
16	0.360	0.460	0.560	54	1.120	1.220	1.320	92	1.880	1.980	2.080	130	2.640	2.740	2.840
17	0.380	0.480	0.580	55	1.140	1.240	1.340	93	1.900	2.000	2.100	131	2.660	2.760	2.860
18	0.400	0.500	0.600	56	1.160	1.260	1.360	94	1.920	2.020	2.120	132	2.680	2.780	2.880
19	0.420	0.520	0.620	57	1.180	1.280	1.380	95	1.940	2.040	2.140	133	2.700	2.800	2.900
20	0.440	0.540	0.640	58	1.200	1.300	1.400	96	1.960	2.060	2.160	134	2.720	2.820	2.920
21	0.460	0.560	0.660	59	1.220	1.320	1.420	97	1.980	2.080	2.180	135	2.740	2.840	2.940
22	0.480	0.580	0.680	60	1.240	1.340	1.440	98	2.000	2.100	2.200	136	2.760	2.860	2.960
23	0.500	0.600	0.700	61	1.260	1.360	1.460	99	2.020	2.120	2.220	137	2.780	2.880	2.980
24	0.520	0.620	0.720	62	1.280	1.380	1.480	100	2.040	2.140	2.240	138	2.800	2.900	3.000
25	0.540	0.640	0.740	63	1.300	1.400	1.500	101	2.060	2.160	2.260	139	2.820	2.920	3.020
26	0.560	0.660	0.760	64	1.320	1.420	1.520	102	2.080	2.180	2.280	140	2.840	2.940	3.040
27	0.580	0.680	0.780	65	1.340	1.440	1.540	103	2.100	2.200	2.300	141	2.860	2.960	3.060
28	0.600	0.700	0.800	66	1.360	1.460	1.560	104	2.120	2.220	2.320	142	2.880	2.980	3.080
29	0.620	0.720	0.820	67	1.380	1.480	1.580	105	2.140	2.240	2.340	143	2.900	3.000	3.100
30	0.640	0.740	0.840	68	1.400	1.500	1.600	106	2.160	2.260	2.360	144	2.920	3.020	3.120
31	0.660	0.760	0.860	69	1.420	1.520	1.620	107	2.180	2.280	2.380	145	2.940	3.040	3.140
32	0.680	0.780	0.880	70	1.440	1.540	1.640	108	2.200	2.300	2.400	146	2.960	3.060	3.160
33	0.700	0.800	0.900	71	1.460	1.560	1.660	109	2.220	2.320	2.420	147	2.980	3.080	3.180
34	0.720	0.820	0.920	72	1.480	1.580	1.680	110	2.240	2.340	2.440	148	3.000	3.100	3.200
35	0.740	0.840	0.940	73	1.500	1.600	1.700	111	2.260	2.360	2.460	149	3.020	3.120	3.220
36	0.760	0.860	0.960	74	1.520	1.620	1.720	112	2.280	2.380	2.480	150	3.040	3.140	3.240
37	0.780	0.880	0.980	75	1.540	1.640	1.740	113	2.300	2.400	2.500				

b) V_{TS} Table of FSBB10CH120DF

T [℃]	Min [V]	Typ [V]	Max [V]	T [℃]	Min [V]	Typ [V]	Max [V]	T [℃]	Min [V]	Typ [V]	Max [V]	T [℃]	Min [V]	Typ [V]	Max [V]
-20	0.000	0.080	0.180	17	0.720	0.820	0.920	54	1.460	1.560	1.660	91	2.200	2.300	2.400
-19	0.000	0.100	0.200	18	0.740	0.840	0.940	55	1.480	1.580	1.680	92	2.220	2.320	2.420
-18	0.020	0.120	0.220	19	0.760	0.860	0.960	56	1.500	1.600	1.700	93	2.240	2.340	2.440
-17	0.040	0.140	0.240	20	0.780	0.880	0.980	57	1.520	1.620	1.720	94	2.260	2.360	2.460
-16	0.060	0.160	0.260	21	0.800	0.900	1.000	58	1.540	1.640	1.740	95	2.280	2.380	2.480
-15	0.080	0.180	0.280	22	0.820	0.920	1.020	59	1.560	1.660	1.760	96	2.300	2.400	2.500
-14	0.100	0.200	0.300	23	0.840	0.940	1.040	60	1.580	1.680	1.780	97	2.320	2.420	2.520
-13	0.120	0.220	0.320	24	0.860	0.960	1.060	61	1.600	1.700	1.800	98	2.340	2.440	2.540
-12	0.140	0.240	0.340	25	0.880	0.980	1.080	62	1.620	1.720	1.820	99	2.360	2.460	2.560
-11	0.160	0.260	0.360	26	0.900	1.000	1.100	63	1.640	1.740	1.840	100	2.380	2.480	2.580
-10	0.180	0.280	0.380	27	0.920	1.020	1.120	64	1.660	1.760	1.860	101	2.400	2.500	2.600
-9	0.200	0.300	0.400	28	0.940	1.040	1.140	65	1.680	1.780	1.880	102	2.420	2.520	2.620
-8	0.220	0.320	0.420	29	0.960	1.060	1.160	66	1.700	1.800	1.900	103	2.440	2.540	2.640
-7	0.240	0.340	0.440	30	0.980	1.080	1.180	67	1.720	1.820	1.920	104	2.460	2.560	2.660
-6	0.260	0.360	0.460	31	1.000	1.100	1.200	68	1.740	1.840	1.940	105	2.480	2.580	2.680
-5	0.280	0.380	0.480	32	1.020	1.120	1.220	69	1.760	1.860	1.960	106	2.500	2.600	2.700
-4	0.300	0.400	0.500	33	1.040	1.140	1.240	70	1.780	1.880	1.980	107	2.520	2.620	2.720
-3	0.320	0.420	0.520	34	1.060	1.160	1.260	71	1.800	1.900	2.000	108	2.540	2.640	2.740
-2	0.340	0.440	0.540	35	1.080	1.180	1.280	72	1.820	1.920	2.020	109	2.560	2.660	2.760
-1	0.360	0.460	0.560	36	1.100	1.200	1.300	73	1.840	1.940	2.040	110	2.580	2.680	2.780
0	0.380	0.480	0.580	37	1.120	1.220	1.320	74	1.860	1.960	2.060	111	2.600	2.700	2.800
1	0.400	0.500	0.600	38	1.140	1.240	1.340	75	1.880	1.980	2.080	112	2.620	2.720	2.820
2	0.420	0.520	0.620	39	1.160	1.260	1.360	76	1.900	2.000	2.100	113	2.640	2.740	2.840
3	0.440	0.540	0.640	40	1.180	1.280	1.380	77	1.920	2.020	2.120	114	2.660	2.760	2.860
4	0.460	0.560	0.660	41	1.200	1.300	1.400	78	1.940	2.040	2.140	115	2.680	2.780	2.880
5	0.480	0.580	0.680	42	1.220	1.320	1.420	79	1.960	2.060	2.160	116	2.700	2.800	2.900
6	0.500	0.600	0.700	43	1.240	1.340	1.440	80	1.980	2.080	2.180	117	2.720	2.820	2.920
7	0.520	0.620	0.720	44	1.260	1.360	1.460	81	2.000	2.100	2.200	118	2.740	2.840	2.940
8	0.540	0.640	0.740	45	1.280	1.380	1.480	82	2.020	2.120	2.220	119	2.760	2.860	2.960
9	0.560	0.660	0.760	46	1.300	1.400	1.500	83	2.040	2.140	2.240	120	2.780	2.880	2.980
10	0.580	0.680	0.780	47	1.320	1.420	1.520	84	2.060	2.160	2.260	121	2.800	2.900	3.000
11	0.600	0.700	0.800	48	1.340	1.440	1.540	85	2.080	2.180	2.280	122	2.820	2.920	3.020
12	0.620	0.720	0.820	49	1.360	1.460	1.560	86	2.100	2.200	2.300	123	2.840	2.940	3.040
13	0.640	0.740	0.840	50	1.380	1.480	1.580	87	2.120	2.220	2.320	124	2.860	2.960	3.060
14	0.660	0.760	0.860	51	1.400	1.500	1.600	88	2.140	2.240	2.340	125	2.880	2.980	3.080
15	0.680	0.780	0.880	52	1.420	1.520	1.620	89	2.160	2.260	2.360				
16	0.700	0.800	0.900	53	1.440	1.540	1.640	90	2.180	2.280	2.380				

6 Print Circuit Board (PCB) Design

6.1 General Application Circuit Example

Figure 41 shows a general application circuitry of interface schematic with control signals connected directly to a MCU. *Figure 42* shows guidance of PCB layout for Motion SPM® 3 Module.

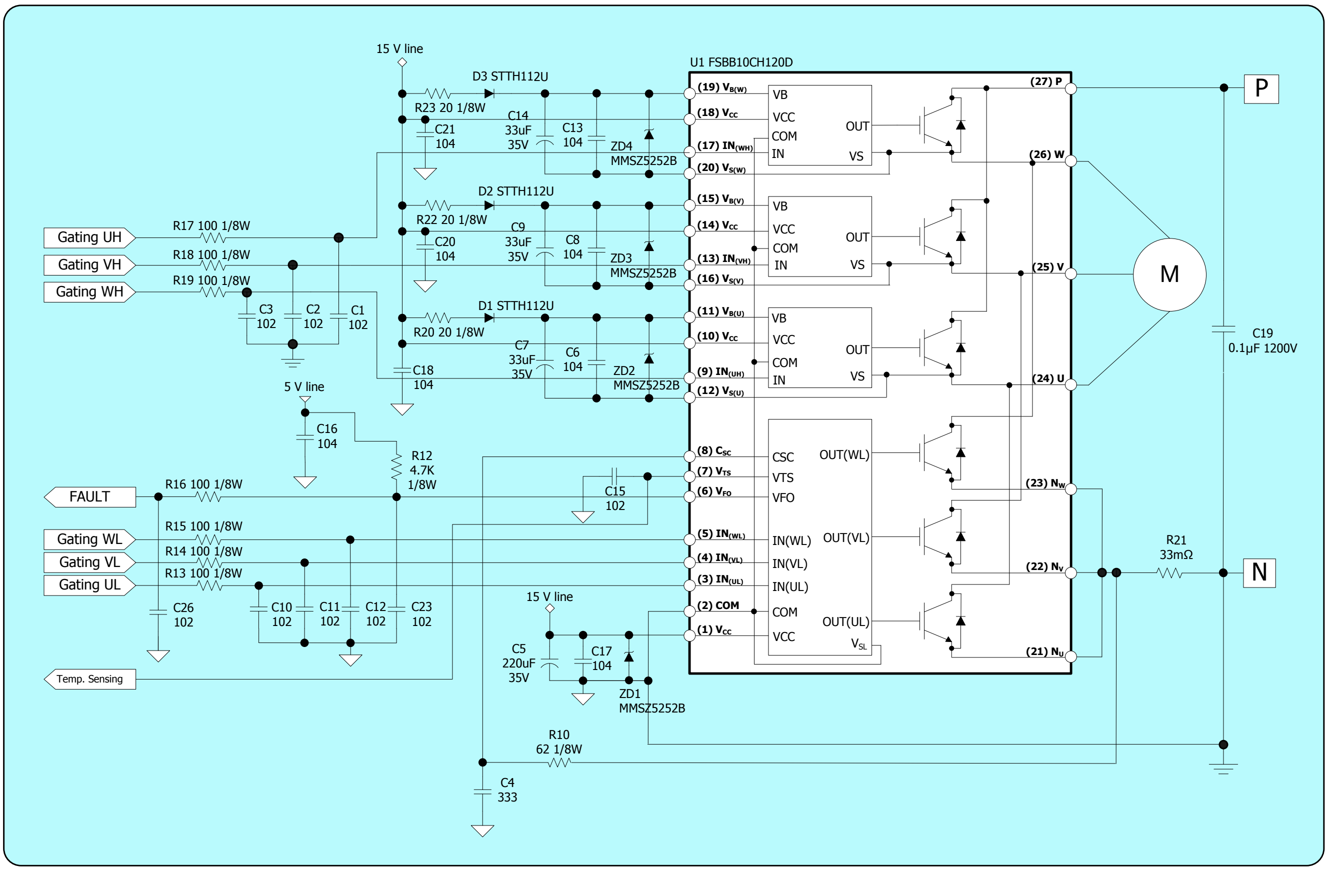


Figure 41. General Application Circuitry for Motion SPM 3 Module

6.2 PCB Layout Guidance

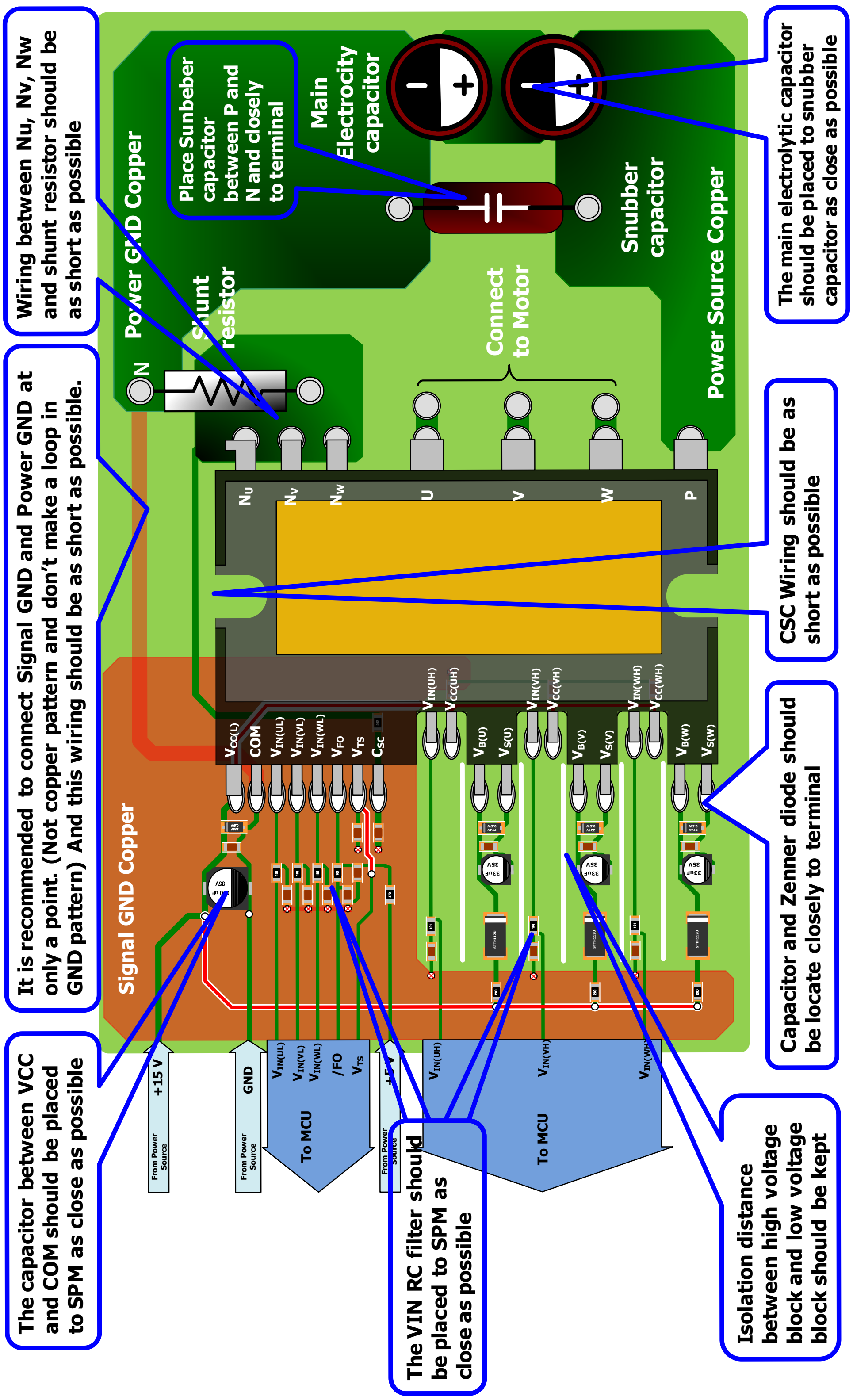
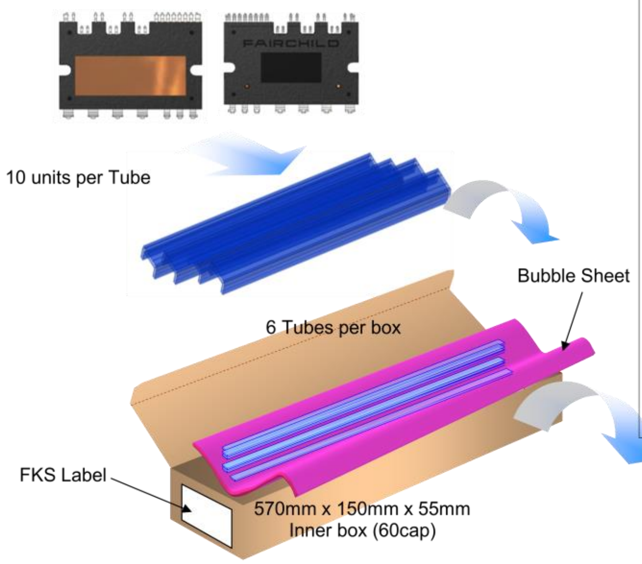


Figure 42. Print Circuit Board (PCB) Layout Guidance for Motion SPM® 3 Module

7 Packing Information

SPMCA-027 Tube Packing Configuration: Figure 1.0



Packaging Description:

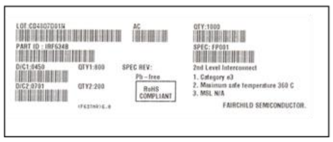
SPMCA-027 parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent.These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains six tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

*SPMCC-027(PKG-MOD27BA),SPMCD-027(PKG-MOD27BA), SPMCE-027(PKG-MOD27BB),SPMCF-027(PKG-MODBD), SPMCG-027(PKG-MOD27BC),SPMEA-027(PKG-MOD27BA),SPMEC-027(PKG-MOD27BA), SPMGA-027(PKG-MOD27BA), SPMGC-027(PKG-MOD27BA), SPMHA-027(PKG-MOD27BA), SPMHC-027(PKG-MOD27BA), SPMIA-027(PKG-MOD27BA), SPMIC-027(PKG-MOD27BA),SPMMA-027(PKG-MOD26BC), SPMMB-027(PKG-MOD26BD) also use packing data.

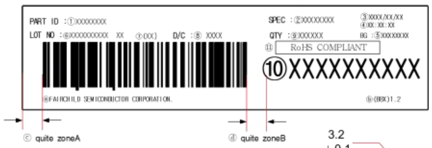
SPMCA-027 Packaging Information: Figure 2.0

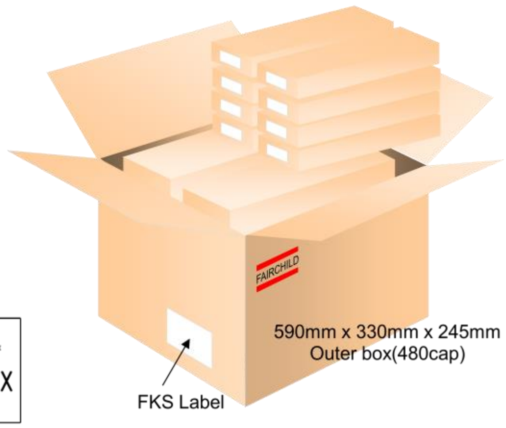
SPMCA-027 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	10
Inner Box Dimension (mm)	570x150x55
Max qty per Box	60
Outer Box Dimension (mm)	590x330x245
Max qty per Box	480
Weight per unit (gm)	-
Note/Comments	

Inner Box Barcode Label Sample

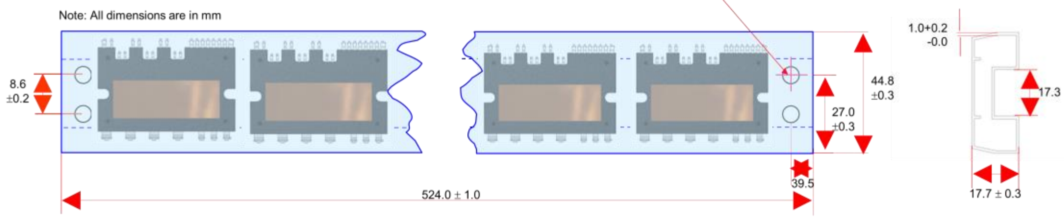


Outer Box Barcode Label Sample





SPMCA-027 Tube Information: Figure 3.0



NOTES:
A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED
B : DRAWING FIEL NAME : PKG-MOD27BAREV1

Figure 43. Packing Information

Related Resources – Product Datasheets and Application Notes

AN-9086- SPM 3 Package Mounting Guidance

RD-404 – Reference Design

FSBB10CH120D – Product Information

FSBB10CH120DF – Product Information

PUBLICATION ORDERING INFORMATION

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