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AN-9760

SPM® PCB设计指南

引言

逆变器系统电路板正变得越来越紧凑和复杂，同时对功率密度的要求也越来越高。使用飞兆半导体的智能功率模块 (SPM®) 即可从容应对挑战。PCB布局设计对于改善可靠性、提升性能和制造性，同时最大程度降低噪声至关重要。

本应用指南描述了PCB布局设计的多个考虑因素和指导原则。

考虑因素

- 寄生电感、电阻和电容
- 由流过寄生电感的 di/dt 引起的电压尖峰
- 电源地、信号地的布局走线
- 无源组件的布局

通用PCB指南

图 1 显示PCB布局整体设计指南，按重要性排序并编号为1至12。

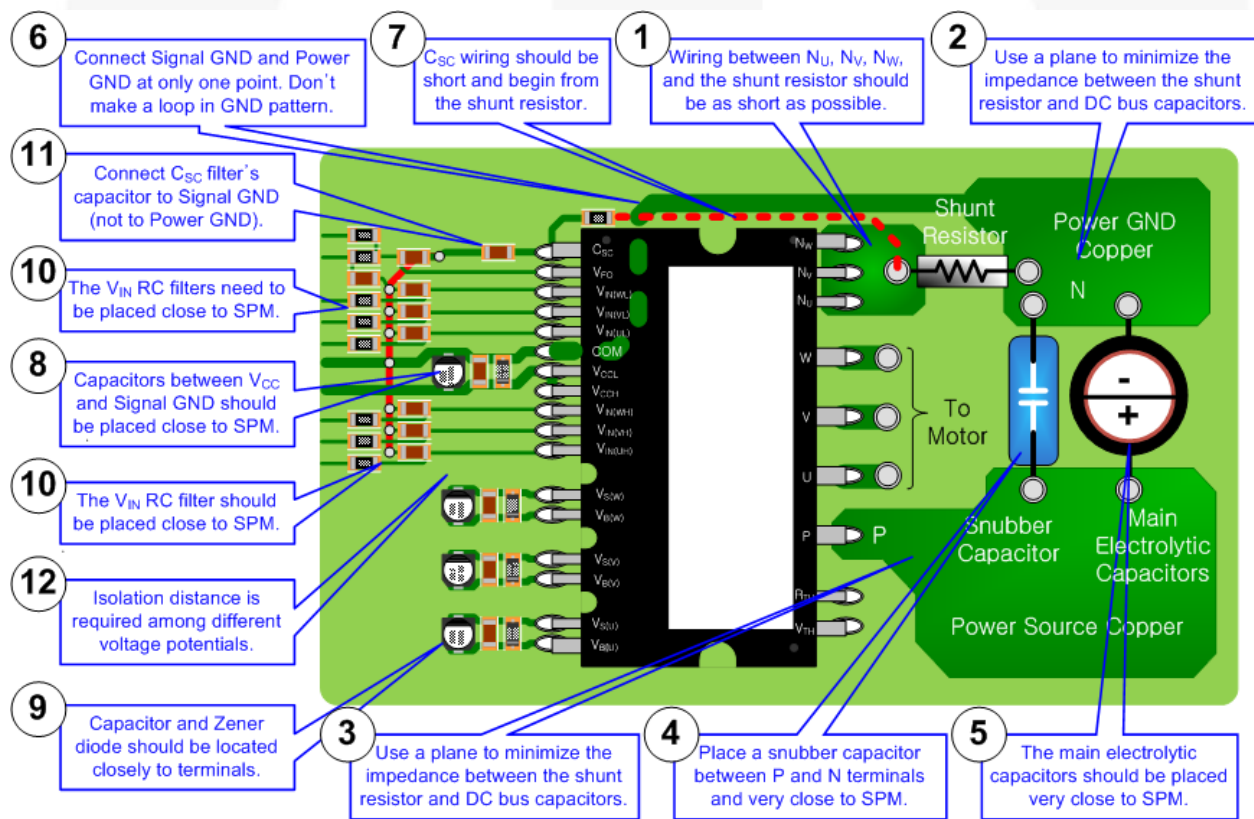


图 1. SPM 整体布局

杂散电感的影响

高开关噪声可能导致逆变器系统故障。只要IGBT打开和关断，就会由电路板主电流路径上的杂散电感产生浪涌电压。图 2 和 图 3 包括Ls1和Ls2，它们是PCB布局中的杂散电感。在IGBT打开和关断的瞬间会出现很高的di/dt。这个di/dt是由电压VLS1和VLS2引起的。为了最大程度地降低寄生电感，使走线应尽可能短是非常重要的。

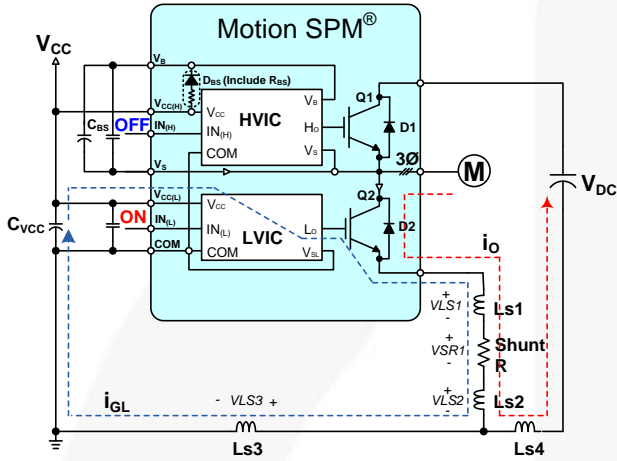


图 2. LVIC栅极驱动路径

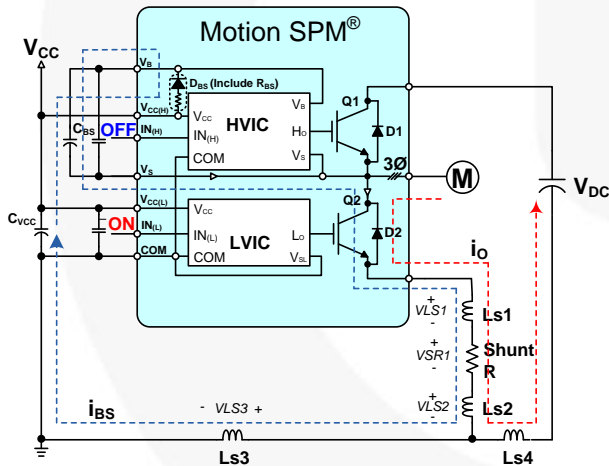


图 3. 自举电容充电路径

图 2 显示了当低端输入信号导通时低端栅极电流 (i_{GL}) 的路径，该电流经过 IGBT Q2 的栅极到达发射极和LVIC，并且从 V_{cc} 到达 L_O 。低端 IGBT 栅极充电回路包含寄生电感和分流电阻，因为 LVIC V_{SL} 未连接 Q2 发射极。

图 3 表示自举电流的路径：当 Q2 或 D2 导通时，(i_{BS}) 经过 IGBT Q2 的集电极到达发射极和 V_{cc} ，再经过 V_B 到达 V_S 。此自举电容 (C_{BS}) 的充电电流回路也包含寄生电感和分流电阻。

一旦 i_o 有快速变化， $L di/dt$ 引起的电压就会影响 IGBT 发射极到 IC 的 COM 端的电压。因此，若该电压尖峰超过 IC

能够耐受的最大电压值，就会损坏 IC。通常，SPM 中的 IC 击穿电压为 25V，例如：

$$V_{CC} + V_{LS1} + V_{SR1} + V_{LS2} + V_{LS3} < 25V \quad (1)$$

若 V_{CC} 为 15V， $V_{LS1} + V_{SR1} + V_{LS2} + V_{LS3}$ 应低于 10V。

构成 L_{S1} 和 L_{S2} 的 PCB 布线应当尽可能短，因为这些走线位于驱动电机的大电流路径上。

在使用多个分流电阻感测多相电流的应用中，最大程度地降低 L_{S1} 和 L_{S2} 会更困难。这种情况下建议使用表贴封装电阻。要使用无感电阻。

自感的计算公式为：

$$L_s = 0.2L \left[\ln \left(\frac{2 \times L}{W + T} \right) + 0.2235(W + T)/L \right] \text{ [nH]} \quad (2)$$

其中：

- L 表示 PCB 布线长度，单位 mm；
- W 表示 PCB 布线宽度，单位 mm；
- T 表示 PCB 布线厚度，单位 mm。

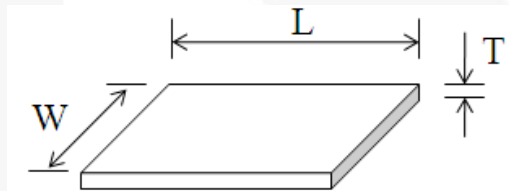


图 4. PCB 布线定义

图 5 显示了在不同的 PCB 布线宽度下 PCB 布线长度与杂散电感的关系，其中镀铜厚度为 1 盎司（即 0.035mm）。

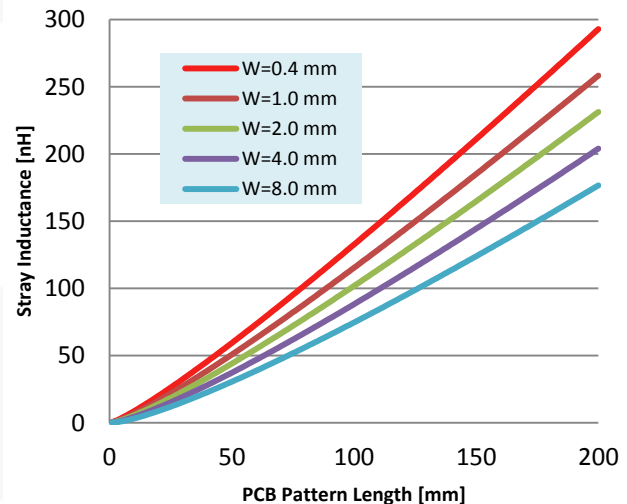


图 5. 1oz 铜片 PCB 杂散电感图

图 6 和 图 7 是一个实际应用的 PCB 布线图 走线上的蓝色线条表示信号路径。图 8 和 图 9 是利用示波器得到的实测值。图 6 中 图 7 以黄色箭头标出测量点。这些表明了 PCB 布线中杂散电感的重要性。

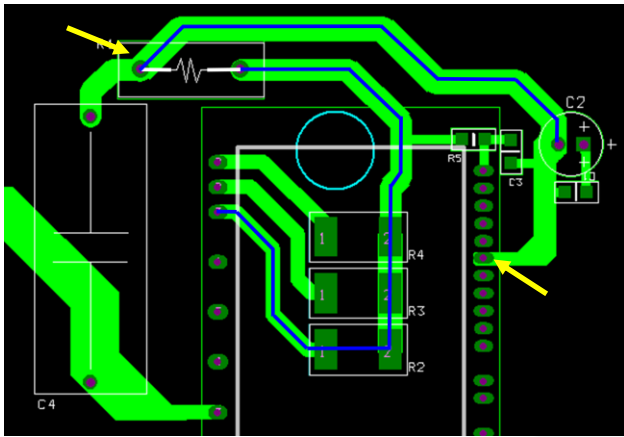


图 6. 改善前的PCB布线

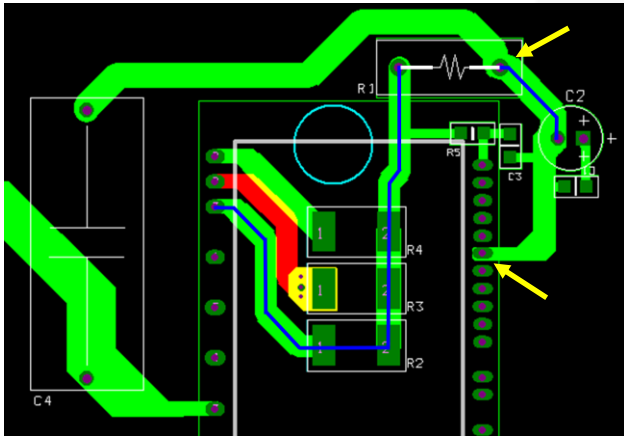


图 7. 改善后的PCB布线

改善PCB布线之前的杂散电感约为120nH，它被降低至35nH左右，如公式 (2) 所示。产生的电压可计算如下：

$$V_s = L \times \frac{di}{dt} \quad [V] \quad (3)$$

若 IGBT 开关时的 di/dt 为 $250A/\mu s$ ，则 V_s 计算如下：

$$V_{s_修改前} = 120nH \times 250A/\mu s = 30V$$

$$V_{s_修改后} = 30nH \times 250A/\mu s = 8.75V$$

PCB 布线改善前的实测峰值电压为 31.58V，改善后为 5.94V。

虽然这种测量并非100%可靠，但31.58V也超过了SPM内部IC的击穿电压。重复尖峰会逐步损坏IC，并可能最终导致器件故障。设计人员需尽量减少主电路路径的寄生电感，以便增强可靠性并降低EMI噪声。

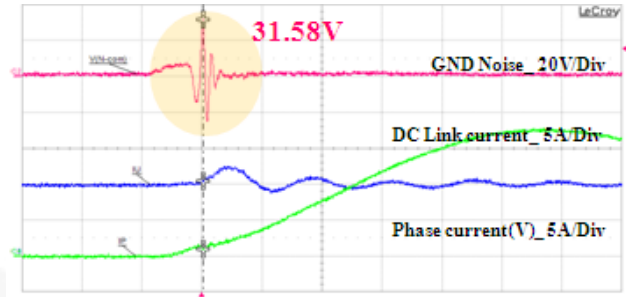


图 8. 改善前的地线噪声

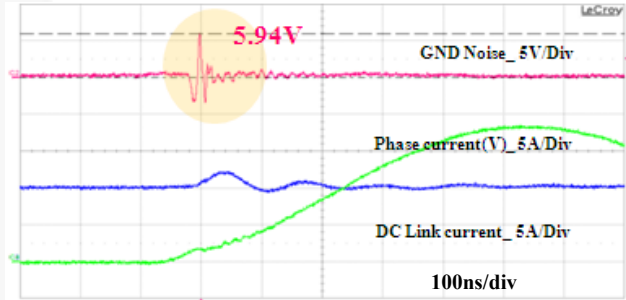


图 9. 改善后的地线噪声

C_{sc}信号的电流感测

C_{sc}图 10输入信号对于检测过流情况，并防止系统损坏而言非常重要。显示了不同的C_{sc}接线点。通过C_{sc}布线可最大程度减小L_{s1}的噪声影响。当C_{sc}接线是在A点连接时，C_{sc}电压受走线电阻上方的L_{s1}的影响。该走线的电阻使跳变电平下降，因为它相当于为分流电阻增加一个串联电阻。L_{s1}在流过反向恢复电流时会产生电压尖峰，因此需要一个具有较大时间常数的滤波器，以避免误触发。建议连接点为图 10中的B点。它也可以应用于电流反馈电路中。应当尽量减小L_{s2}，以获得可靠的电流保护和测量性能。

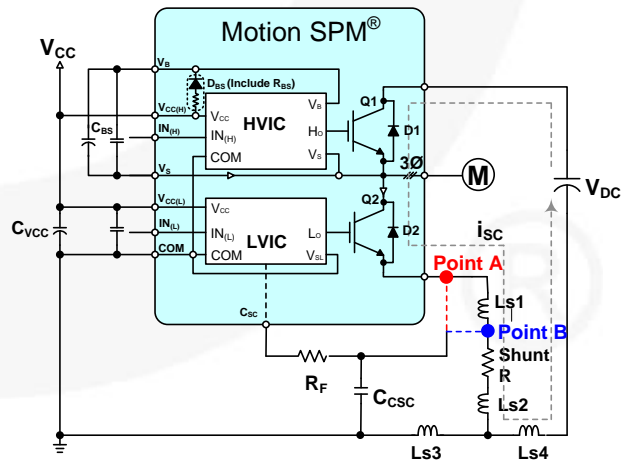


图 10. PCB布局中的电流感测点

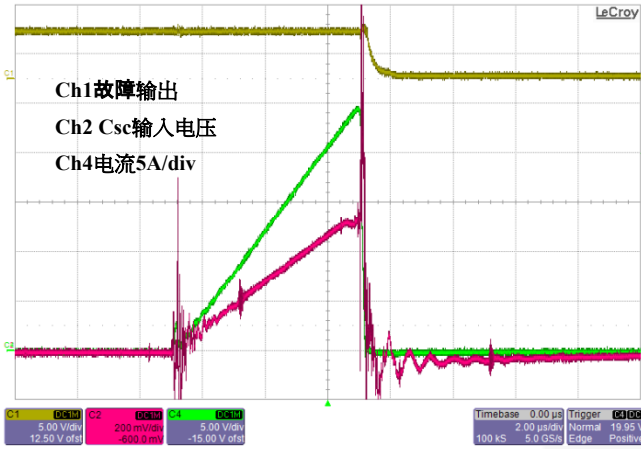


图 11. C_{sc}来自A点时的波形

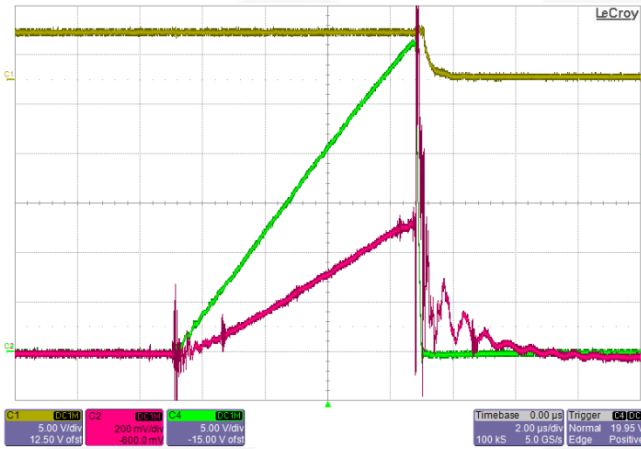


图 12. C_{sc}来自B点时的波形

图 11 和 图 12 显示了两个C_{sc}测量点的不同之处。该测试中使用了一个20mΩ的分流电阻。C_{sc}阈值电平为0.5V，因此，过流触发电平为25A直流。就实际电流而言，从A点测量有较低的触发电平值，但C_{sc}电压基本相同。由于使用了时间常数为1.8μs的RC滤波器，并且从内部比较器到PWM关断和故障输出之间存在额外传输延迟，因此电流达到触发电平后将上升。请不要被实际的触发电平所迷惑，并得出结论说A点的结果更好。

V_{cc}和COM之间电容的位置

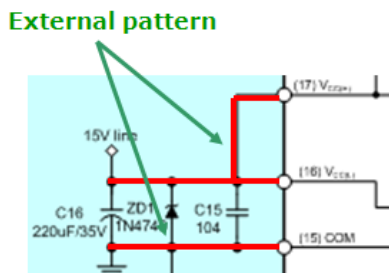


图 13. V_{cc}-COM之间的器件布局 (SPM®)

V_{cc}和COM之间的电容应靠近SPM放置，如图 13所示。图 14 和 图 15 显示在1oz铜片和20mil宽度下，V_{cc}上的纹波随着电容和V_{cc}-COM之间的距离而改变。建议使用齐纳二极管防止浪涌电压。

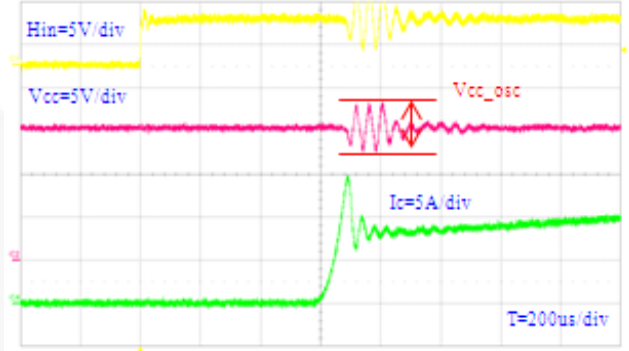


图 14. C16到V_{cc}和COM的距离为20mm

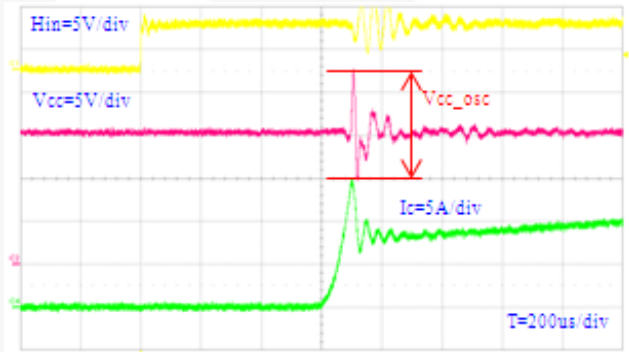


图 15. C16到V_{cc}和COM的距离为5mm

自举电容的位置

V_b和V_s图 16之间的电容应靠近SPM放置，如 所示。更长的PCB布线会导致更高的峰值浪涌电压。当V_s在开关瞬间为负值时，V_{bs}可上升至超过V_{cc}。建议加入一个齐纳二极管，以防止浪涌电压。

External pattern

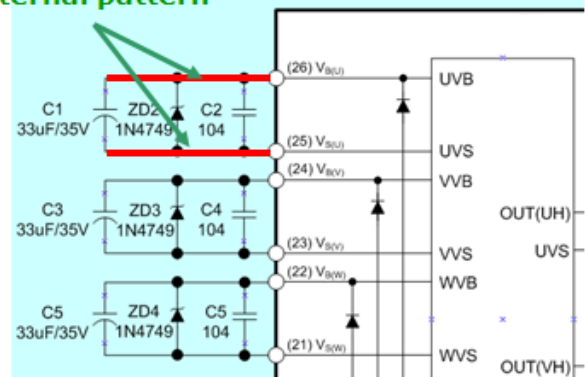


图 16. V_{bs}处的器件布局 (SPM®)

图 17 和 图 18显示V_{BS}的纹波电压随着电容到V_B和V_S的距离不同的变化。

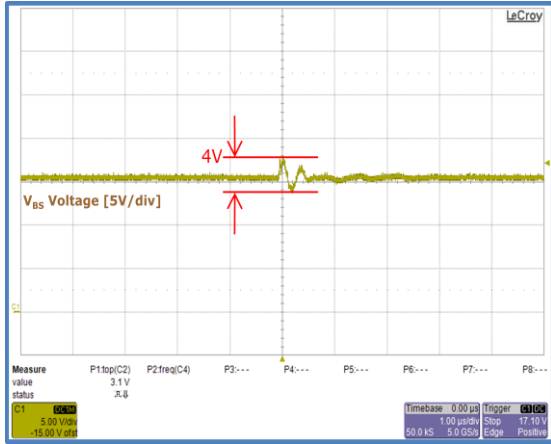


图 17. 实验结果 (C1到V_{BS}距离为10mm)

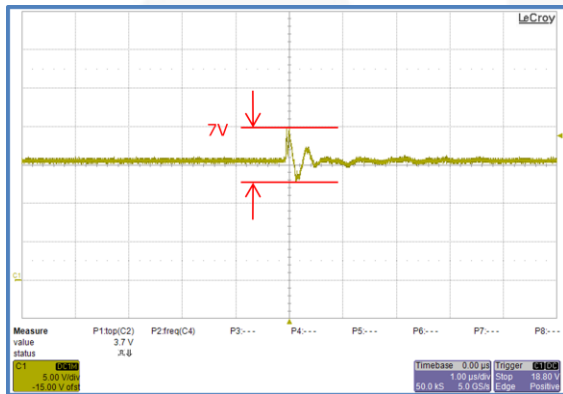


图 18. 实验结果 (C1到V_{BS}距离为50mm)

缓冲电容的位置

一般建议使用0.1~2.2μF薄膜电容作为缓冲电容。若在错误的位置安装了缓冲电容，如图 16中的位置A，则无法有效抑制浪涌电压。位置B具有最佳的噪声抑制性能，但该缓冲电容的充放电电流无法反映在分流电阻上，从而使电流反馈测量或过流保护功能出现错误。位置C是一个合理的折衷位置，其抑制性能优于位置A，且不会影响电流检测信号精度。因此，通常使用位置C。

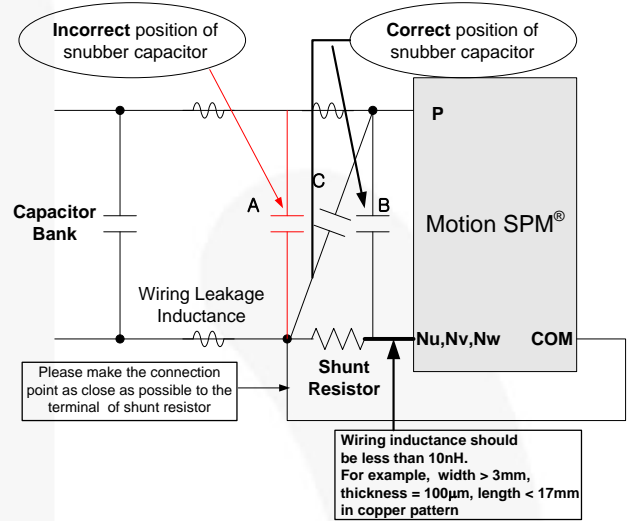


图 20. 直流链路缓冲电容位置

用于输入信号的RC滤波器

V_{IN} RC滤波器可防止错误的IGBT开关动作。采用RC滤波器时，请记住，可能会发生PWM伏秒失真现象，并且可能会降低PWM性能。

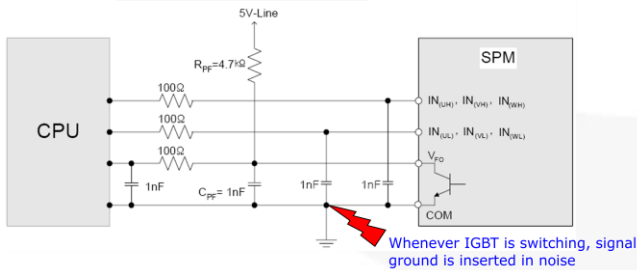


图 19. SPM®RC滤波器中的元件布局

若PCB布局良好，则内部下拉电阻即可胜任工作，但通常还是会使用额外的强下拉电阻使其工作更可靠。

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[FNA40560 — 智能功率模块Motion SPM®](#)

[FNA40860 — 智能功率模块Motion SPM®](#)

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[RD-344 — FNA41560 参考设计（单检流电阻方案）](#)

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