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AND8009/D

ECLinPS Plus™
SPICE Modeling Kit

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APPLICATION NOTE

Objective

The objective of "AND8009 ECLinPS Plus SPICE Modeling Kit" is to provide sufficient circuit schematic and SPICE parameter information to allow system level interconnect modeling of the ECLinPS Plus logic line devices. The kit is not intended to provide sufficient information to perform whole device logic modeling.

Schematic Information

The kit contains representative input and output schematics, netlists, and waveforms used for the ECLinPS Plus devices. The buffer, package, and ESD subcircuit models may be connected to simulate driver and receiver interconnect characteristics as shown in Figure 1. A specific device may be modeled as shown in Figure 2. No Function Logic modeling is provided.
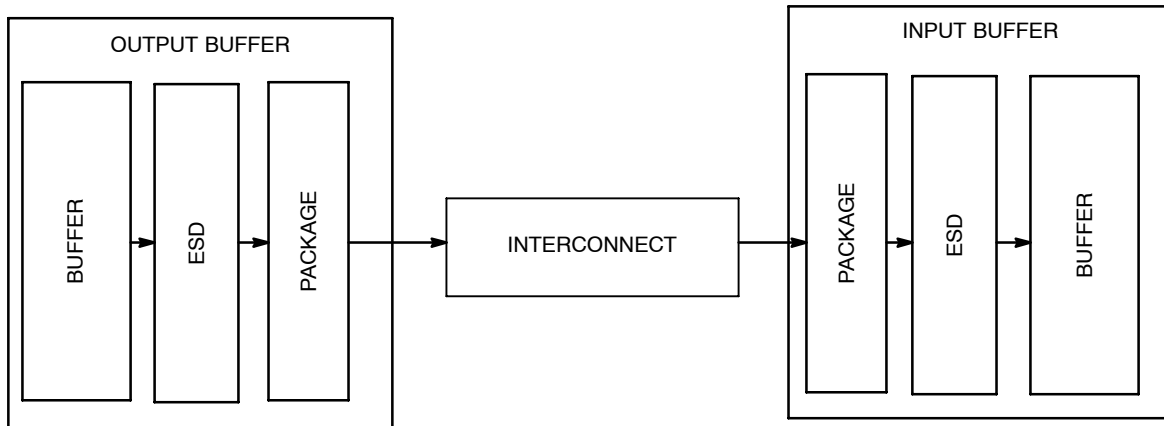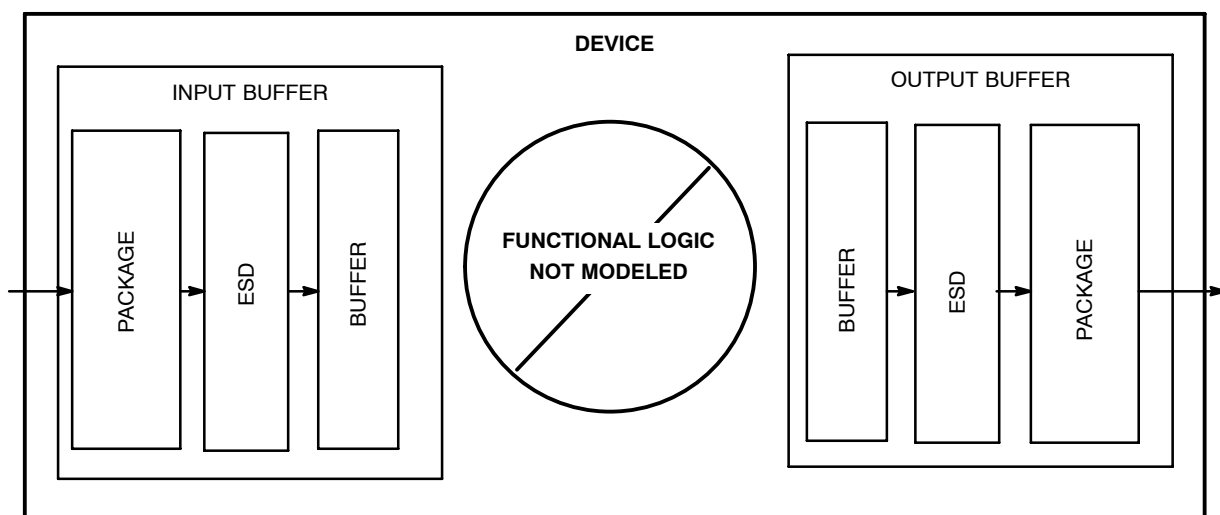

Figure 1. Interconnect Model Template

Figure 2. DEVICE Model Template

1

There are four terminals on all transistor models: Emitter, Base, Collector, and Substrate (biased to V_{EE}). It should be noted that circuits can be used single ended by replacing INB with V_{BB}. Table 1 describes the nomenclature used in the schematics and netlists.

To simulate a different operating modes all levels, except V_{CS}, are adjusted with respect to V_{CC}. The V_{CS} is adjusted with respect to V_{EE} ($\approx V_{EE} + 1.1$ V $\pm$ 50 mV)

Table 1. Schematics and Netlist Nomenclature

Parameter	Function Description
V_{CC}	3.3 V FOR LVPECL OR (0 V) FOR LVECL
V_{CCO}	1.6 V – 2.0 V HSTL Output Positive Supply
V_{CS}	Internal Reference Voltage ($\approx$ VEE + 1.1 V $\pm$ 50 mV)
V_{HSTL}	HSTL Internal Constant Voltage Source
V_{EE}	–3.3 V FOR LVECL OR (0 V) FOR LVPECL
GND	0 V
V_{TT}	V_{CC} – 2 V TERMINATION PLANE
IN	TRUE INPUT TO CKT
INB or $\overline{IN}$	INVERTED INPUT TO CKT
Q	TRUE OUTPUT OF CKT
QB or $\overline{Q}$	INVERTED OUTPUT OF CKT

Input Buffer

A typical input buffer schematic (Figure 3) and netlist are representing structures currently in use on most existing devices in this family. Specific devices may have unique input buffer models per Table 2. The ESD and package models should be added for more accurate model behavior. An internal input pulldown resistor is shown in the ESD network, Figure 26. Some devices may also display an internal pullup resistor to V_{CC}. Refer to specific device data sheet pinout and logic diagram for internal input resistor. The input buffers may be shown as differential, but may be modified to represent a single−ended structure by using a DC bias on the non driven input (at the signal pin common mode voltage). It is unnecessary to include an ESD or package model for the V_{BB} pins of the models because V_{BB} is intended as an internal node for most applications. If V_{BB} is modeled as an external node it is usually bypassed because it is a constant voltage, and adding ESD and Package parameters provide no additional benefit.

Output Buffer

An output buffer schematic and netlist may or may not require the temperature compensation (TC) network structure depending on the specific device series. All 100 series devices will require the TC network. A 10 series device does not include a TC network. ESD, package, and termination models must be added for proper buffer behavior. Output buffers are shown as differential. When simulating a single−ended output, both differential outputs should utilize ESD, package, and termination models to maintain properly balanced loading.

Package

Various simplified input and output package case models may be found in the Appendix Section, Package RLC. Specific device package pin models may be modified according to IBIS model parasitics values.

EP16 Buffer Model

The EP16 interconnect has been completely modeled to provide a working schematic and output waveforms as examples of the ECLinPS Plus line. The typical input buffer may be driven with the output buffer, OBUF01. (See Figure 28, simplified EP16 SPICE model and Figure 29 typical output waveform.)

SPICE Netlists

The netlists are organized as a group of subcircuits. In each subcircuit model netlist, the model name is followed by a list of external node interconnects.

Temperature Compensation Network for 100EP

The output netlists include temperature compensation network circuitry for 100EP style output buffers. The circuit components of the temperature compensation networks are shown in Figure 29. For simulating 10EP style outputs these components should either be deleted or commented out of the subcircuit netlists. Subcircuit models such as the Input or Output Buffer, Package, Input ESD and Output ESD should connect to supplies through hierarchical, passed parameters such as V_{CC}, V_{EE}, etc., for proper simulation and not separately attached to independent power supplies.

SPICE Parameter Information

In addition to the schematics and netlists is a listing of the SPICE parameters for the transistors referenced in the schematics and netlists. These parameters represent a typical device of a given transistor. Varying the typical parameters will affect the DC and AC performance of the structures; but for the type of modeling intended by this note, the actual delay times are not necessary and are not modeled, as a result variation of the device parameters are meaningless. The performance levels are more easily varied by other methods and will be discussed in the next section. The resistors referenced in the schematics are polysilicon and have no parasitic capacitance in the real circuit and none is required in the model. The schematics display the only devices needed in the SPICE netlists.

Modeling Information

The bias drivers for the devices are not detailed since their circuitry would result in a substantial increase of model complexity and simulation time. Instead, these internal reference voltages (V_{BB}, V_{CS}, V_{HSTL}, etc.) should be driven with ideal constant voltage sources.

The schematics and SPICE parameters will provide a typical output waveshape, which can be seen in Figures 29, 30, and 31. Simple adjustments can be made to the models allowing output characteristics to simulate conditions at or near the corners of the data book specifications. Consistent cross−point voltages need to be maintained.

- To adjust rise and fall times:

  Produce the desired rise and fall times output slew rates by adjusting collector load resistors to change the gates tail current. The V_{CS} voltage will affect the tail current in the output differential, which will interact with the load resistor and collector resistor to determine t_r and t_f at the output.

- To adjust the V_{OH}:

  Adjust the V_{OH} and V_{OL} level by the same amount by varying V_{CC}. The output levels will follow changes in V_{CC} at a 1:1 ratio.

- To adjust the V_{OL} only:

  Adjust the V_{OL} level independently of the V_{OH} level by increasing or decreasing the collector load resistance. Note that the V_{OH} level will also change slightly due to a $I_{BASE}R$ drop across the collector load resistor. V_{OL} can be changed by varying the VCS supply, and therefore the gate current through the current source resistor.

Summary

The information included in this kit provides adequate information to run a SPICE level system interconnect simulation. Device input or output models are presented in Table 2. For EP and LVEP series devices not listed in Table 2, consult www.onsemi.com (Technical Support).

Table 2. ECLinPS PLUS INPUT/OUTPUT SELECTION TABLE

Device	Package A	Package B	Input ESD	Input Buffer	Output Buffer	Output ESD
EP01	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
EP05	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
EP08	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
EP11	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
EP14	20−lead TSSOP	N/A	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
EP16	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
EP17	20−lead SO	20−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF06	OUT_ESD
EP29	20−lead TSSOP	N/A	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
EP31	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
EP32	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
EP33	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF02	OUT_ESD
EP35	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
EP40	20−lead TSSOP	N/A	IN_ESD	TYPICAL INBUF	OBUF09	OUT_ESD
EP51	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
EP52	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
EP56	20−lead SO	20−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF04	OUT_ESD
EP57	20−lead TSSOP	N/A	IN_ESD	TYPICAL INBUF	OBUF04	OUT_ESD
EP58	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
EP89	8−lead SO	8−lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF05	OUT_ESD
EP90	20−lead TSSOP	N/A	IN_ESD	TYPICAL INBUF	OBUF04	OUT_ESD
EP016	32−lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF02	OUT_ESD
EP016A	32−lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF02	OUT_ESD
EP101	32−lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF06	OUT_ESD
EP105	32−lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF06	OUT_ESD
EP116	32−lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF06	OUT_ESD
EP131	32−lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF02	OUT_ESD

Table 2. ECLinPS PLUS INPUT/OUTPUT SELECTION TABLE

Device	Package A	Package B	Input ESD	Input Buffer	Output Buffer	Output ESD
EP139	20–lead SO	20–lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF07	OUT_ESD
EP140	8–lead SO	N/A	IN_ESD	TYPICAL INBUF	OBUF09	OUT_ESD
EP142	32–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
EP195	32–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF04	OUT_ESD
EP196	32–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF04	OUT_ESD
EP210S	32–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF10	OUT_ESD
EP223	64–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF11	OUT_ESD
EP445	32–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
EP446	32–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF04	OUT_ESD
EP451	32–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
EP809	32–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF11	OUT_ESD
LVEP11	8–lead SO	8–lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF08	OUT_ESD
LVEP14	20–lead TSSOP	N/A	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
LVEP16	8–lead SO	8–lead TSSOP	IN_ESD	TYPICAL INBUF	OBUF08	OUT_ESD
LVEP17	20–lead TSSOP	24–lead QFN	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
LVEP34	16–lead SO*	16–lead TSSOP*	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
LVEP56	20–lead TSSOP	24–lead QFN	IN_ESD	TYPICAL INBUF	OBUF01	OUT_ESD
LVEP111	32–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
LVEP210	32–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
LVEP221	52–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
LVEP222	52–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
LVEP224	64–lead LQFP	N/A	IN_ESD	TYPICAL INBUF	OBUF03	OUT_ESD
NV4N840M	QFN–32	–	–	50 Ω to V_{CC}	OBUF12	–
NB4L16M	QFN–16	–	–	50 Ω to V_{CC}	OBUF14	–
NB4N527S	QFN–16	–	–	INBUF02	OBUF13	–
NB4N855S	Micro–10	–	–	INBUF02	OBUF13	–
NB4N507A	SOIC–16	–	–	INBUF04	OBUF15	–

*For package model, please consult manufacturer at www.onsemi.com (Technical Support).

Netlists and Schematics
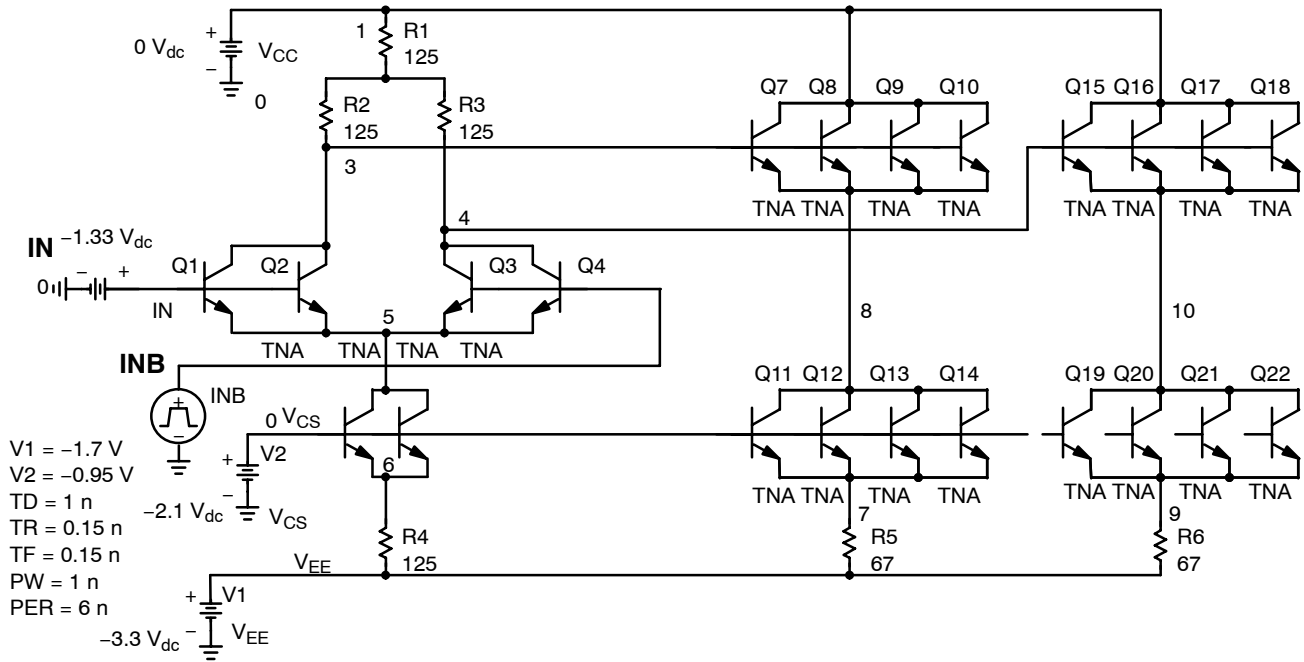

Figure 3. Typical INBUF

```
.SUBCKT TYPICAL INBUF IN INB VCS VEE
Q_Q1      3 IN 5 TNA
Q_Q2      3 IN 5 TNA
Q_Q3      4 INB 5 TNA
Q_Q4      4 INB 5 TNA
Q_Q5      5 VCS 6 TNA
Q_Q6      5 VCS 6 TNA
Q_Q7      1 3 8 TNA
Q_Q8      1 3 8 TNA
Q_Q9      1 3 8 TNA
Q_Q10     1 3 8 TNA
Q_Q11     8 VCS 7 TNA
Q_Q12     8 VCS 7 TNA
Q_Q13     8 VCS 7 TNA
Q_Q14     8 VCS 7 TNA
Q_Q15     1 4 10 TNA
Q_Q16     1 4 10 TNA
Q_Q17     1 4 10 TNA
Q_Q18     1 4 10 TNA
Q_Q19     10 VCS 9 TNA
Q_Q20     10 VCS 9 TNA
Q_Q21     10 VCS 9 TNA
Q_Q22     10 VCS 9 TNA
R_R1      2 1   125
R_R2      3 2   125
R_R3      4 2   125
R_R4      VEE 6  125
R_R5      VEE 7  67
R_R6      VEE 9  67
V_V1      VEE 0 −3.3Vdc
V_V2      VCS 0 −2.1Vdc
V_IN      IN 0 −1.33Vdc
V_VCC     1 0 0Vdc
V_INB     INB 0
+PULSE −1.7V −0.95V 1n 0.15n 0.15n 1n 6n
.END TYPICAL INBUF
```
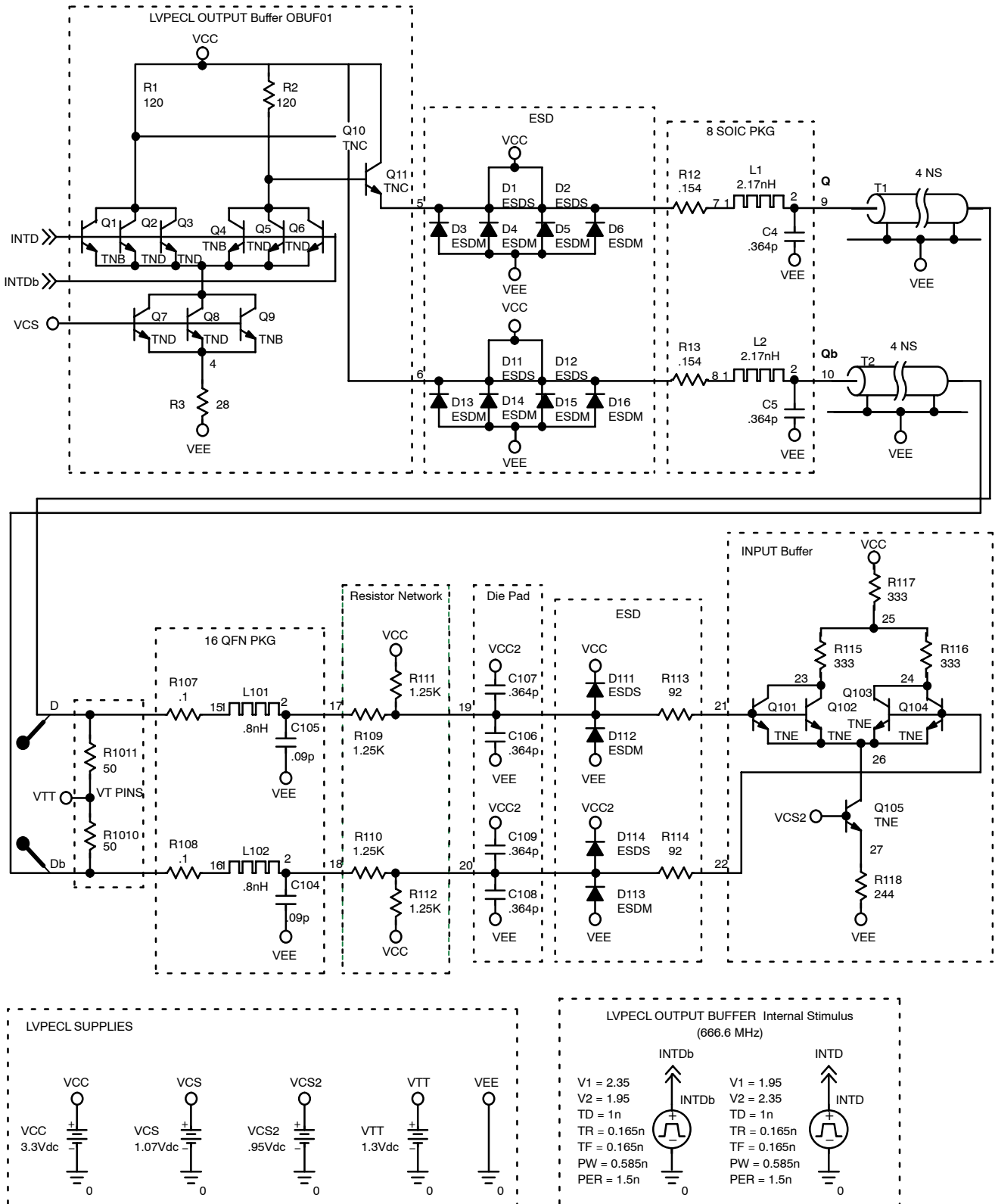
Figure 4.

```
* OBUF01 driving INBUF02
V_INTD          INTD 0  +PULSE 2.35 1.95 1n 0.165n 0.165n 0.585n 1.5n
V_INTDb          INTDB 0  +PULSE 1.95 2.35 1n 0.165n 0.165n 0.585n 1.5n
V_VCC          $G_VCC 0 3.3Vdc
V_VCS          $G_VCS 0 1.07Vdc
V_VCS2          $G_VCS2 0 .95Vdc
V_VTT          $G_VTT 0 1.3Vdc
.SUBCKT OBUF01 INTD INTDb VCC VCS VEE VTT D DB
C_C4           0 9  .364p
C_C5           0 10  .364p
D_D1           5 $G_VCC ESDS
D_D2           5 $G_VCC ESDS
D_D3           0 5 ESDM
D_D4           0 5 ESDM
D_D5           0 5 ESDM
D_D6           0 5 ESDM
D_D11          6 $G_VCC ESDS
D_D12          6 $G_VCC ESDS
D_D13          0 6 ESDM
D_D14          0 6 ESDM
D_D15          0 6 ESDM
D_D16          0 6 ESDM
L_L1           7 9  2.17nH
L_L2           8 10  2.17nH
Q_Q1           2 INTD 1 TNB
Q_Q2           2 INTD 1 TND
Q_Q3           2 INTD 1 TND
Q_Q4           3 INTDB 1 TNB
Q_Q5           3 INTDB 1 TND
Q_Q6           3 INTDB 1 TND
Q_Q7           1 $G_VCS 4 TND
Q_Q8           1 $G_VCS 4 TND
Q_Q9           1 $G_VCS 4 TNB
Q_Q10          $G_VCC 2 6 TNC
R_R1           2 $G_VCC  120
R_R2           3 $G_VCC  120
R_R3           0 4  28
R_R12          5 7  .154
R_R13          6 8  .154
T_T1           9 0 D 0 Z0=50 TD=4000ps
T_T2           10 0 DB 0 Z0=50 TD=4000ps
.END OBUF01
```

```
.SUBCKT INBUF02 D DB VCC VCS VEE
C_C104          0 18  .09p
C_C105          0 17  .09p
C_C106          0 19  .364p
C_C107          19 $G_VCC2  .364p
C_C108          0 20  .364p
C_C109          20 $G_VCC2  .364p
D_D111          19 $G_VCC ESDS
D_D112          0 19 ESDM
D_D113          0 20 ESDM
D_D114          20 $G_VCC2 ESDS
L_L101          15 17  .8nH
L_L102          16 18  .8nH
Q_Q101          23 21 26 TNE
Q_Q102          23 21 26 TNE
Q_Q103          24 22 26 TNE
Q_Q104          24 22 26 TNE
Q_Q105          26 $G_VCS2 27 TNE
Q_Q11           $G_VCC 3 5 TNC
R_R107          D 15  .1
R_R108          DB 16  .1
R_R109          19 17  1.25K
R_R110          18 20  1.25K
R_R111          19 $G_VCC  1.25K
R_R112          $G_VCC 20  1.25K
R_R113          19 21  92
R_R114          22 20  92
R_R115          23 25  333
R_R116          24 25  333
R_R117          25 $G_VCC  333
R_R118          0 27  244
R_R1010         $G_VTT DB  50
R_R1011         D $G_VTT  50
.END INBUF02
```
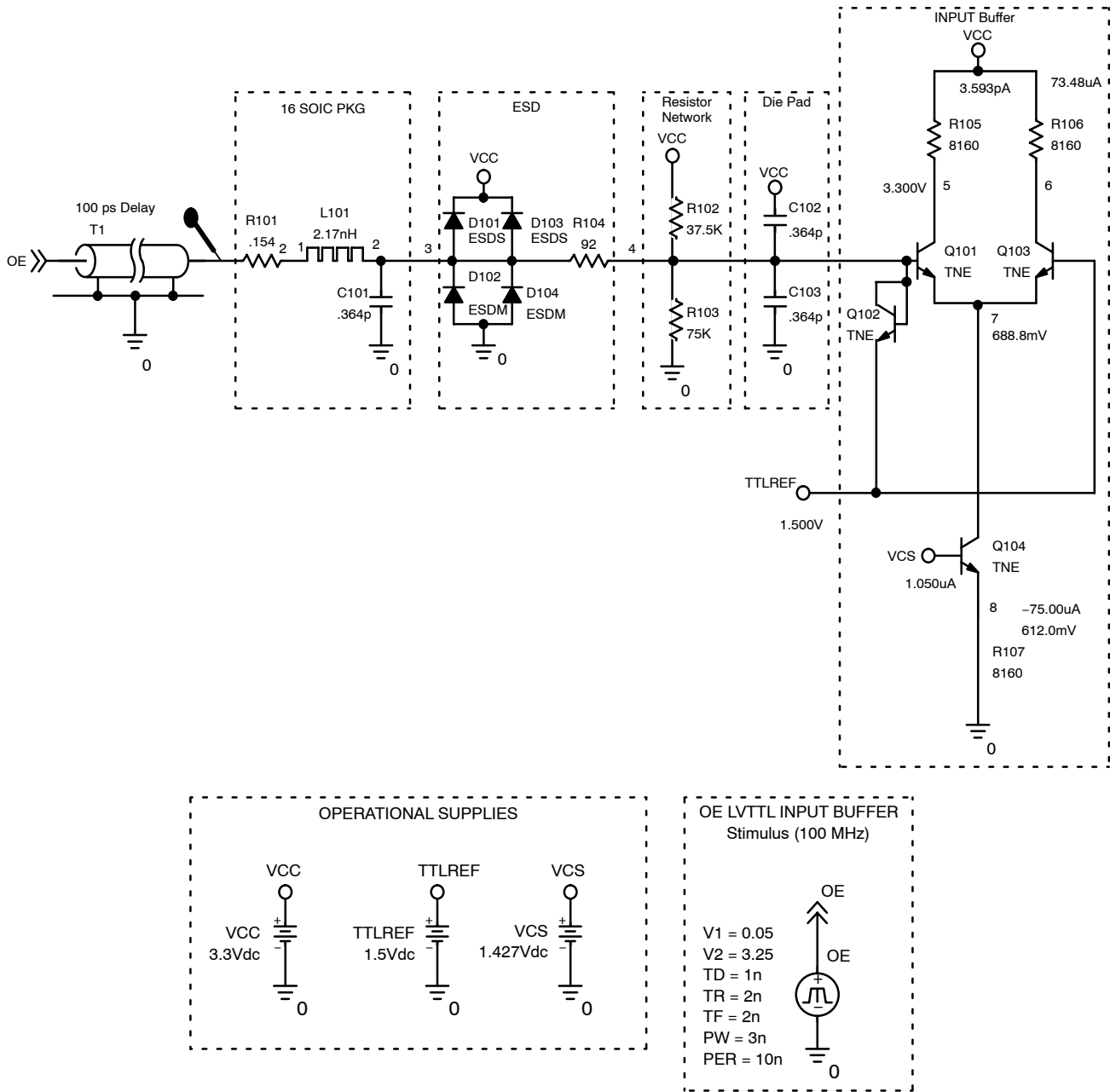
INBUF04 INPUT BUFFER

Figure 5. INBUF04 Input Buffer

```
NETLIST for INBUF04
V_OE       OE 0 PULSE 0.05 3.25 1n 2n 2n 3n 10n
V_TTLREF   $G_TTLREF 0 1.5Vdc
V_VCC      $G_VCC 0 3.3Vdc
V_VCS      $G_VCS 0 1.427Vdc
SUBCKT INBUF04
C_C101     0 3  .364p
C_C102     4 $G_VCC  .364p
C_C103     0 4  .364p
D_D101     3 $G_VCC ESDS
D_D102     0 3 ESDM
```

```
D_D103    3 $G_VCC ESDM
D_D104    0 3 ESDS
L_L101    2 3  2.17nH
Q_Q101    5 4 7 TNE
Q_Q102    4 4 $G_TTLREF TNE
Q_Q103    6 $G_TTLREF 7 TNE
Q_Q104    7 $G_VCS 8 TNE
R_R101    1 2  .154
R_R102    4 $G_VCC  37.5K
R_R103    4 0  75K
R_R104    3 4  92
R_R105    5 $G_VCC  8160
R_R106    6 $G_VCC  8160
R_R107    0 8  8160
T_T1      OE 0 1 0 Z0=50 TD=100ps
END INBUF04
```
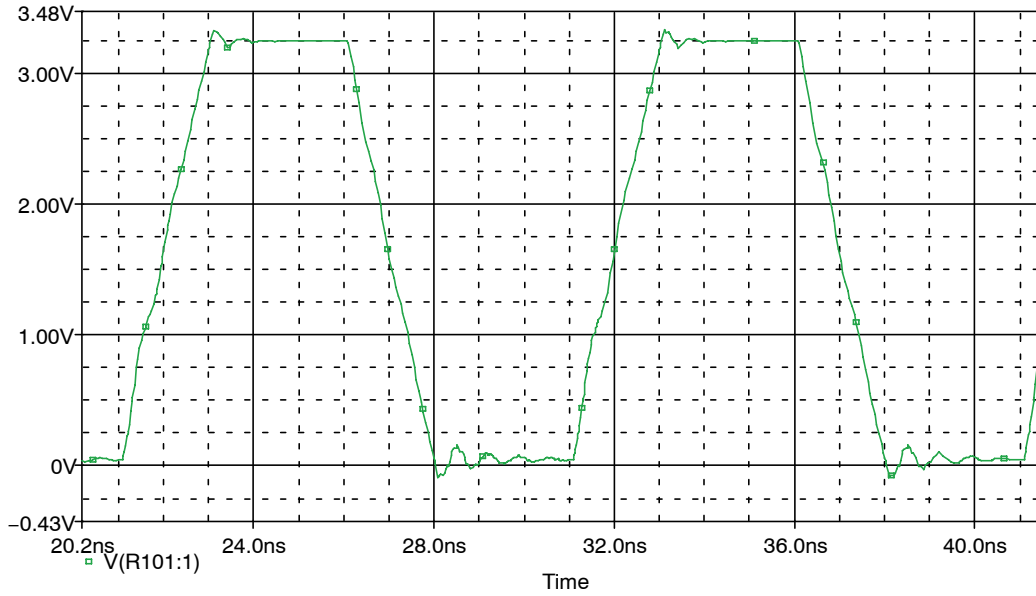

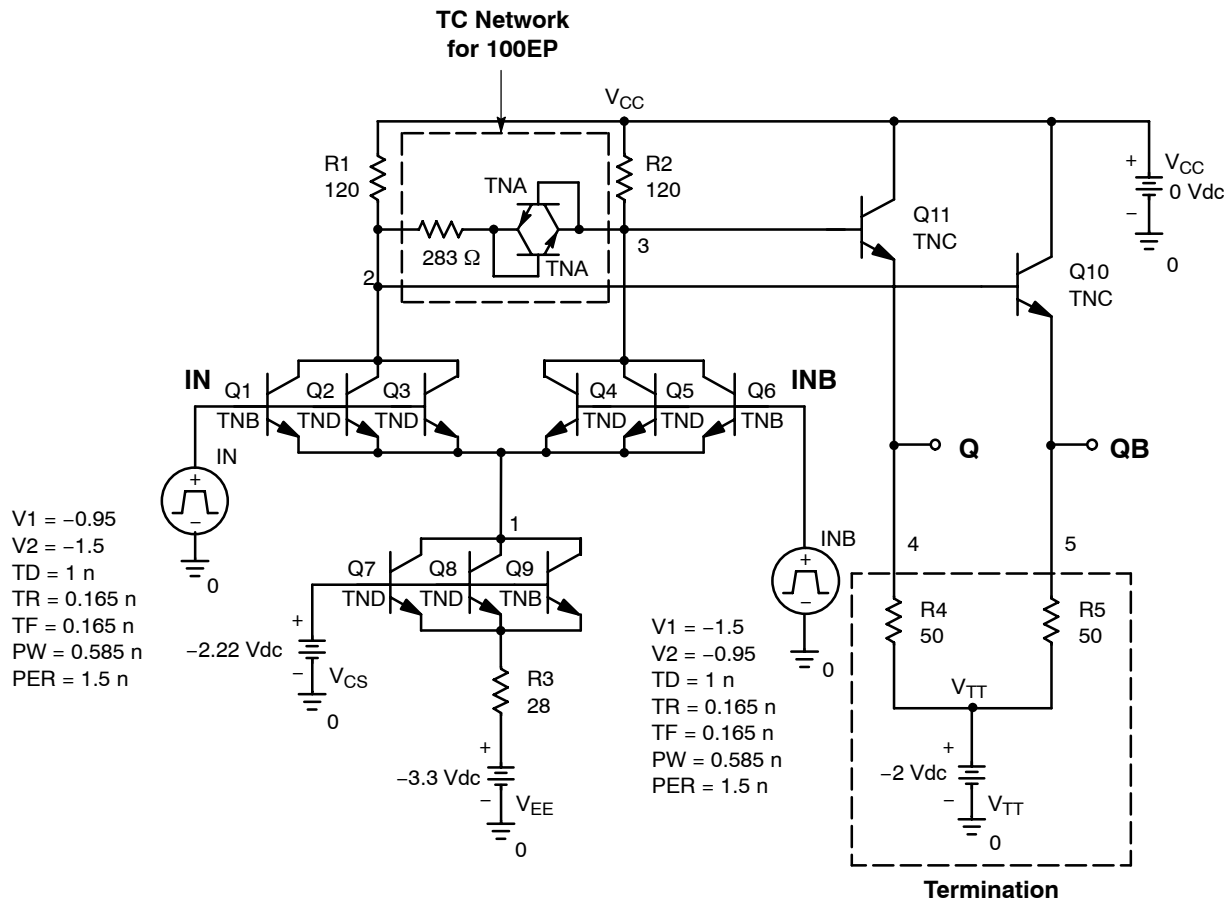**Figure 6. Typical LVCMOS Driving INBUF04 Input Buffer at 100 MHz**

**TC Network
for 100EP**

Figure 7. OBUF01

```
.SUBCKT OBUF01 IN INB VCS VCC VEE VTT
Q_Q1        2 IN 1 TNB
Q_Q2        2 IN 1 TND
Q_Q3        2 IN 1 TND
Q_Q4        3 INB 1 TND
Q_Q5        3 INB 1 TND
Q_Q6        3 INB 1 TNB
Q_Q7        1 VCS 10 TND
Q_Q8        1 VCS 10 TND
Q_Q9        1 VCS 10 TNB
Q_Q10       VCC 2 5 TNC
Q_Q11       VCC 3 4 TNC
R_R1        2 VCC  120
R_R2        3 VCC  120
R_R3        VEE 10  28
R_R4        VTT 4  50
R_R5        VTT 5  50
V_IN        IN 0
+PULSE −0.95 −1.5 1n 0.165n 0.165n 0.585n 1.5n
V_INB       INB 0
+PULSE −1.5 −0.95 1n 0.165n 0.165n 0.585n 1.5n
V_VCC       VCC 0 0Vdc
V_VEE       VEE 0 −3.3Vdc
V_VTT       VTT 0 −2Vdc
V_VCS       VCS 0 −2.22Vdc
.END OBUF01
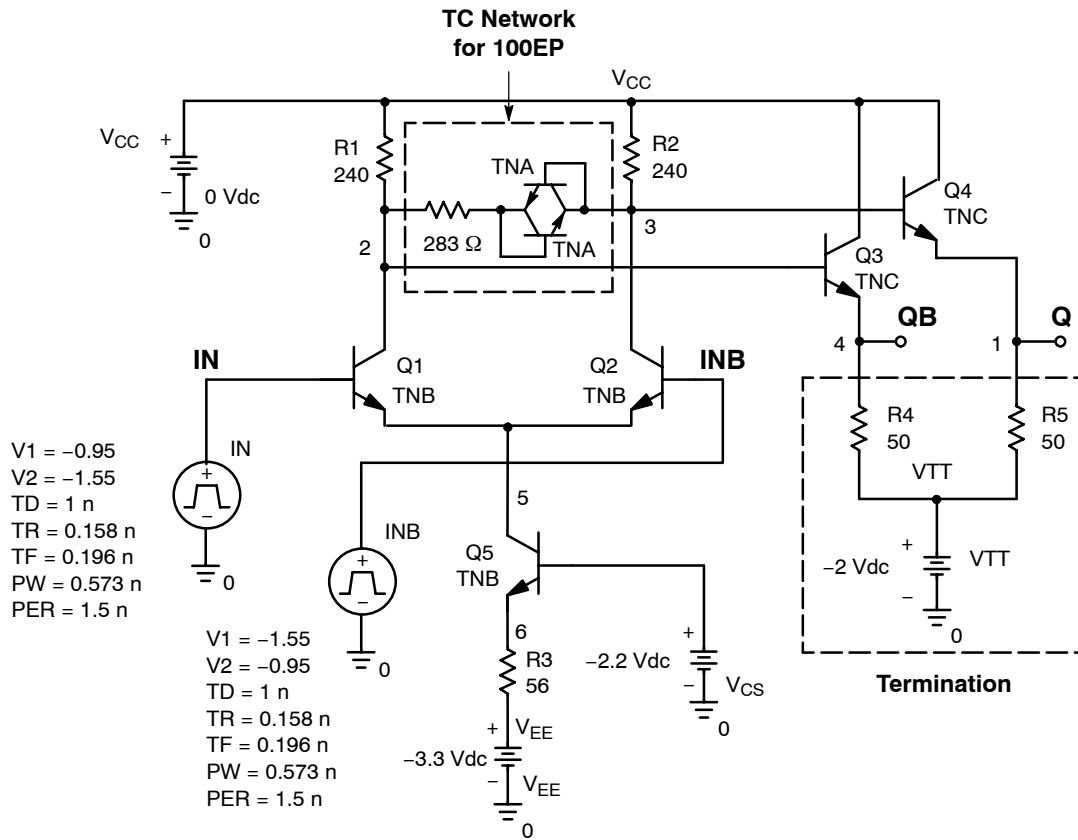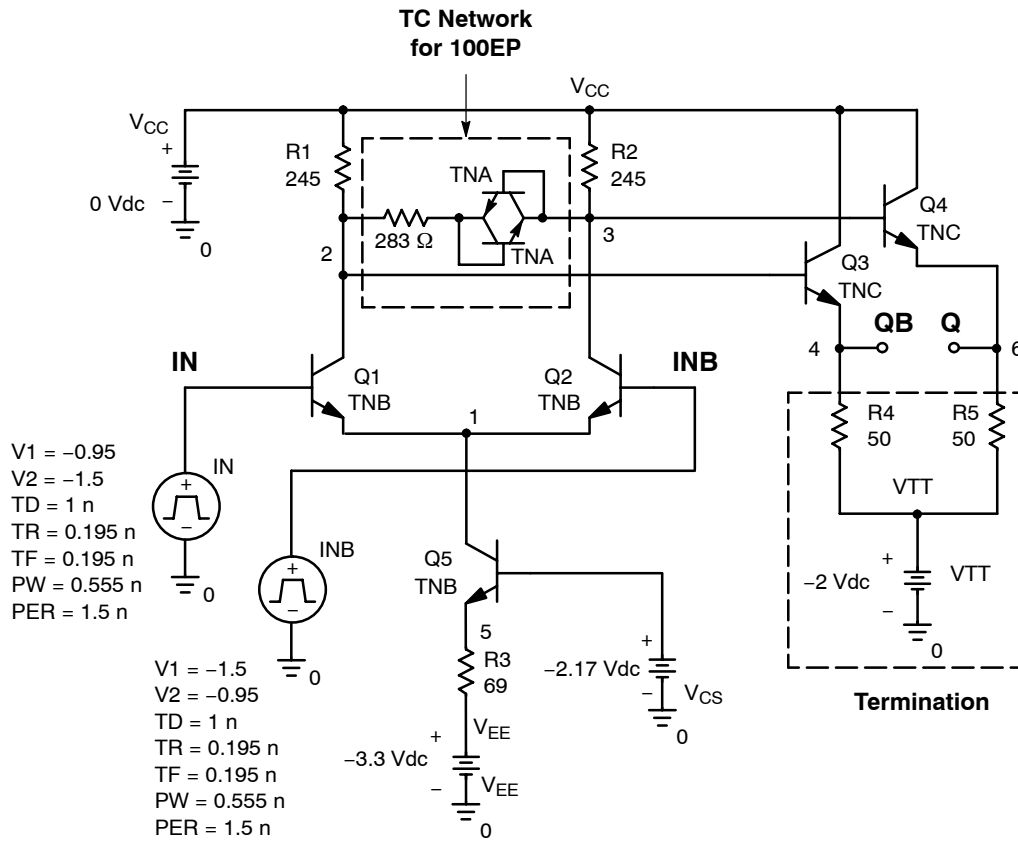```

**Figure 8. OBUF02**

```
.SUBCKT OBUF02 IN INB VCC VCS VEE VTT
Q_Q1       2 IN 5 TNB
Q_Q2       3 INB 5 TNB
Q_Q3       VCC 2 4 TNC
Q_Q4       VCC 3 1 TNC
Q_Q5       5 VCS 6 TNB
R_R1       2 VCC  240
R_R2       3 VCC  240
R_R3       VEE 6  56
R_R4       VTT 4  50
R_R5       VTT 1  50
V_IN       IN 0
+PULSE −0.95 −1.55 1n 0.158n 0.196n 0.573n 1.5n
V_INB      INB 0
+PULSE −1.55 −0.95 1n 0.158n 0.196n 0.573n 1.5n
V_VCC      VCC 0 0Vdc
V_VEE      VEE 0 −3.3Vdc
V_VTT      VTT 0 −2Vdc
V_VCS      VCS 0 −2.2Vdc
.END OBUF02
```

**TC Network
for 100EP**

Figure 9. OBUF03

```
.SUBCKT OBUF03 IN INB VCC VCS VEE VTT
Q_Q1        2 IN 1 TNB
Q_Q2        3 INB 1 TNB
Q_Q3        VCC 2 4 TNC
Q_Q4        VCC 3 6 TNC
Q_Q5        1 VCS 5 TNB
R_R1        2 VCC  245
R_R2        3 VCC  245
R_R3        VEE 5  69
R_R4        VTT 4  50
R_R5        VTT 6  50
V_IN        IN 0
+PULSE −0.95 −1.5 1n 0.195n 0.195n 0.555n 1.5n
V_INB       INB 0
+PULSE −1.5 −0.95 1n 0.195n 0.195n 0.555n 1.5n
V_VCC       VCC 0 0Vdc
V_VEE       VEE 0 −3.3Vdc
V_VTT       VTT 0 −2Vdc
V_VCS       VCS 0 −2.17Vdc
.END OBUF03
```

**TC Network
for 100EP**

Figure 10. OBUF04
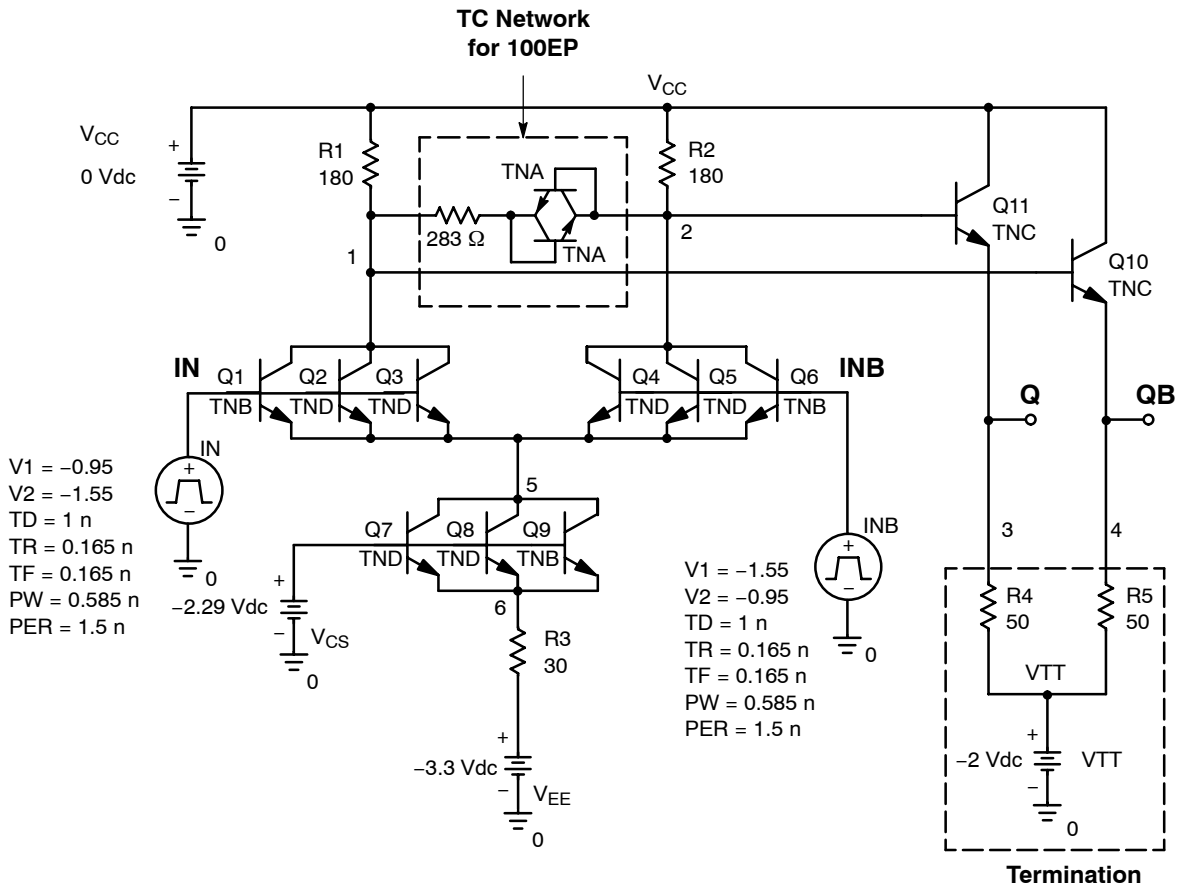
```
.SUBCKT OBUF04 IN INB VCS VCC VEE VTT
Q_Q1      1 IN 5 TNB
Q_Q2      1 IN 5 TND
Q_Q3      1 IN 5 TND
Q_Q4      2 INB 5 TND
Q_Q5      2 INB 5 TND
Q_Q6      2 INB 5 TNB
Q_Q7      5 VCS 6 TND
Q_Q8      5 VCS 6 TND
Q_Q9      5 VCS 6 TNB
Q_Q10     VCC 1 4 TNC
Q_Q11     VCC 2 3 TNC
R_R1      1 VCC   180
R_R2      2 VCC   180
R_R3      VEE 6   20
R_R4      VTT 3   50
R_R5      VTT 4   50
V_IN      IN 0
+PULSE −0.95 −1.55 1n 0.165n 0.165n 0.585n 1.5n
V_INB     INB 0
+PULSE −1.55 −0.95 1n 0.165n 0.165n 0.585n 1.5n
V_VCC     VCC 0 0Vdc
V_VEE     VEE 0 −3.3Vdc
V_VTT     VTT 0 −2Vdc
V_VCS     VCS 0 −2.29Vdc
.END OBUF04
```
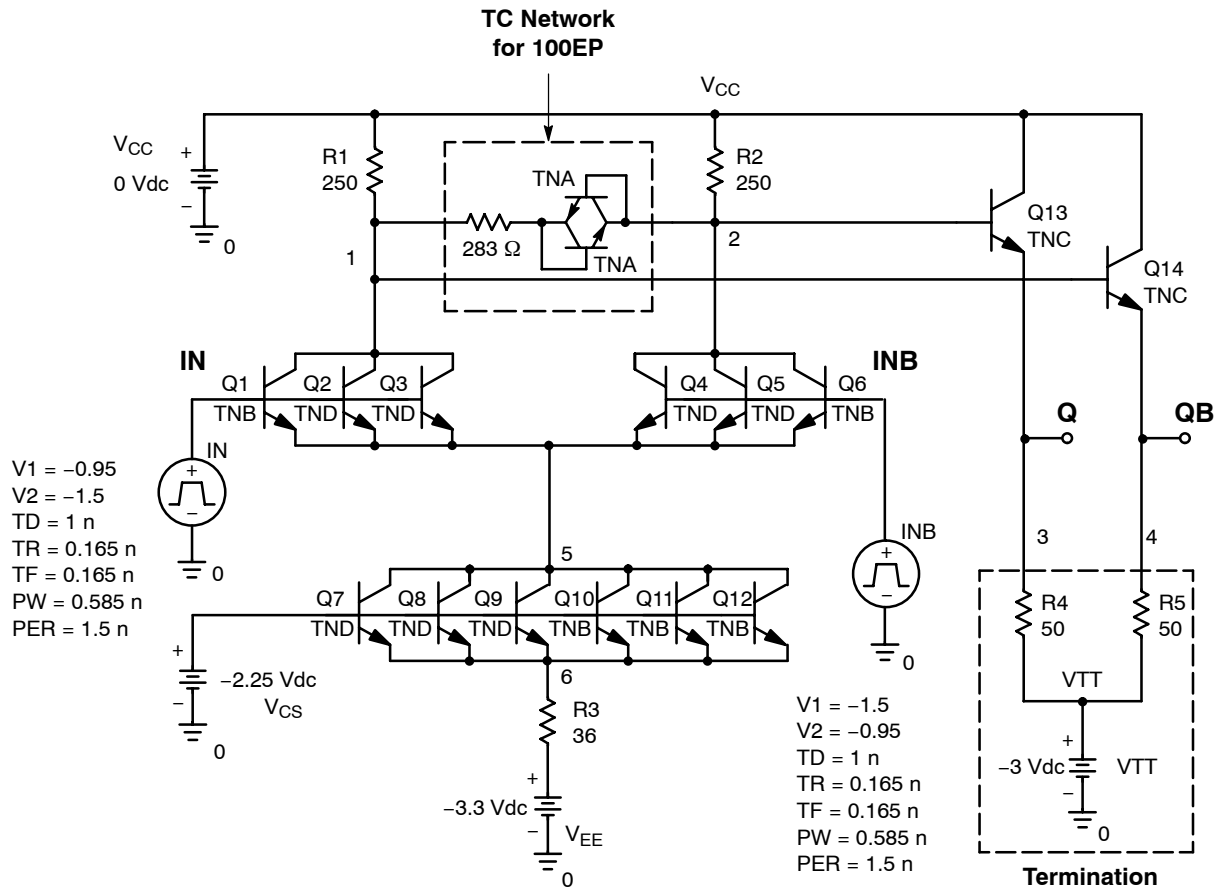
Figure 11. OBUF05

```
.SUBCKT OBUF05 IN INB VCS VCC VTT VEE
Q_Q1        1 IN 5 TNB
Q_Q2        1 IN 5 TND
Q_Q3        1 IN 5 TND
Q_Q4        2 INB 5 TND
Q_Q5        2 INB 5 TND
Q_Q6        2 INB 5 TNB
Q_Q7        5 VCS 6 TND
Q_Q8        5 VCS 6 TND
Q_Q9        5 VCS 6 TND
Q_Q10       5 VCS 6 TNB
Q_Q11       5 VCS 6 TNB
Q_Q12       5 VCS 6 TNB
Q_Q13       VCC 2 3 TNC
Q_Q14       VCC 1 4 TNC
R_R1        1 VCC 285
R_R2        2 VCC 285
R_R3        VEE 6 38
R_R4        VTT 3 50
R_R5        VTT 4 50
V_IN        IN 0 −1.33Vdc
+PULSE −0.95 −1.5 1n 0.165n 0.165n 0.585n 1.5n
V_INB       INB 0
+PULSE −1.5 −0.95 1n 0.165n 0.165n 0.585n 1.5n
V_VEE       VEE 0 −3.3Vdc
V_VCC       VCC 0 0Vdc
V_VTT       VTT 0 −3Vdc
V_VCS       VCS 0 −2.25Vdc
.END OBUF05
```
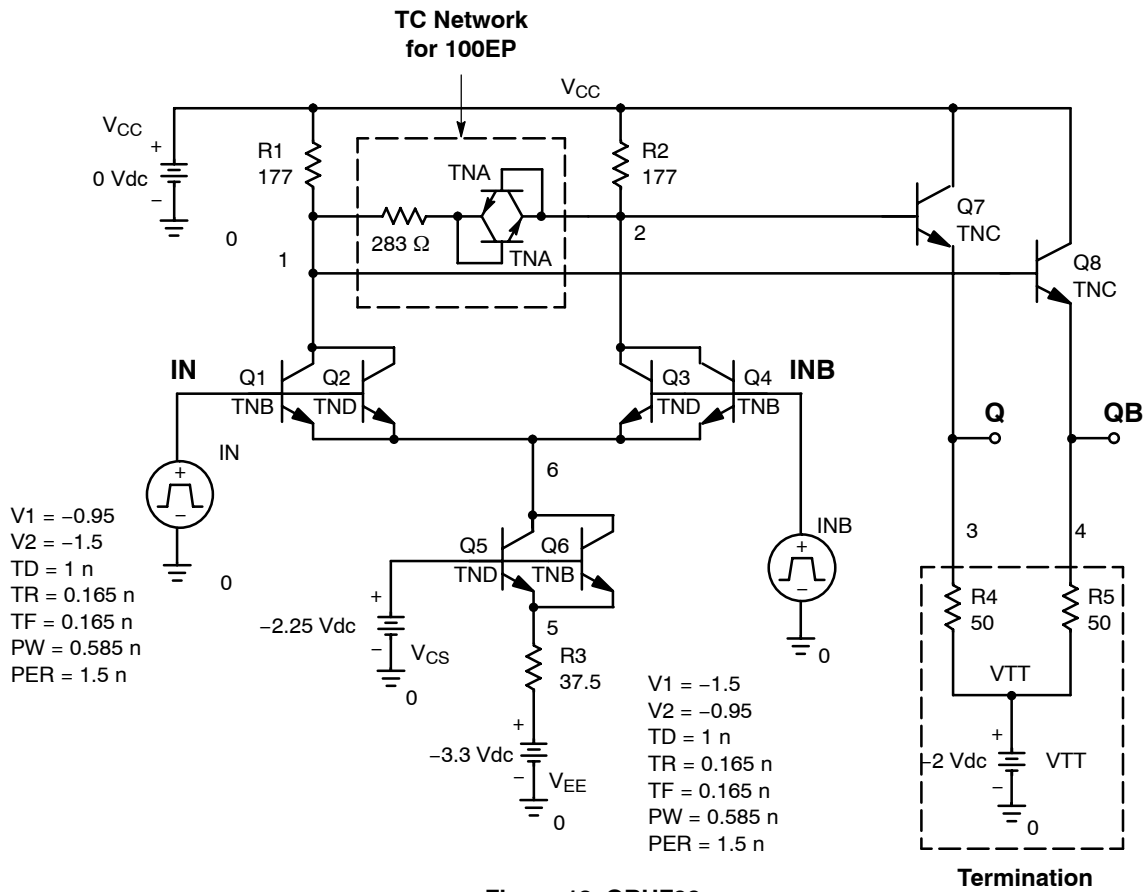
**TC Network
for 100EP**

V_{CC}

V_{CC}

V_{CC}
0 Vdc

R1
177

R2
177

283 Ω

TNA

TNA

0

1

2

Q7
TNC

Q8
TNC

IN

Q1
TNB

Q2
TND

Q3
TND

Q4
TNB

INB

Q

QB

IN

V1 = −0.95
V2 = −1.5
TD = 1 n
TR = 0.165 n
TF = 0.165 n
PW = 0.585 n
PER = 1.5 n

0

6

Q5
TND

Q6
TNB

−2.25 Vdc

V_{CS}

0

5

R3
37.5

INB

0

3

4

R4
50

R5
50

VTT

−3.3 Vdc

V_{EE}

0

V1 = −1.5
V2 = −0.95
TD = 1 n
TR = 0.165 n
TF = 0.165 n
PW = 0.585 n
PER = 1.5 n

−2 Vdc

VTT

0

Termination

Figure 12. OBUF06

```
.SUBCKT OBUF06 IN INB VCC VCS VEE VTT
Q_Q1       1 IN 6 TNB
Q_Q2       1 IN 6 TND
Q_Q3       2 INB 6 TND
Q_Q4       2 INB 6 TNB
Q_Q5       6 VCS 5 TND
Q_Q6       6 VCS 5 TNB
Q_Q7       VCC 2 3 TNC
Q_Q8       VCC 1 4 TNC
R_R1       1 VCC  177
R_R2       2 VCC  177
R_R3       VEE 5  37.5
R_R4       VTT 3  50
R_R5       VTT 4  50
V_IN       IN 0
+PULSE −0.95 −1.5 1n 0.165n 0.165n 0.585n 1.5n
V_INB      INB 0
+PULSE −1.5 −0.95 1n 0.165n 0.165n 0.585n 1.5n
V_VEE      VEE 0 −3.3Vdc
V_VCC      VCC 0 0Vdc
V_VTT      VTT 0 −2Vdc
V_VCS      VCS 0 −2.25Vdc
.END OBUF06
```

**TC Network
for 100EP**

V1 = −0.95
V2 = −1.5
TD = 1 n
TR = 0.195 n
TF = 0.195 n
PW = 0.555 n
PER = 1.5 n

V1 = −1.5
V2 = −0.95
TD = 1 n
TR = 0.195 n
TF = 0.195 n
PW = 0.555 n
PER = 1.5 n

Termination
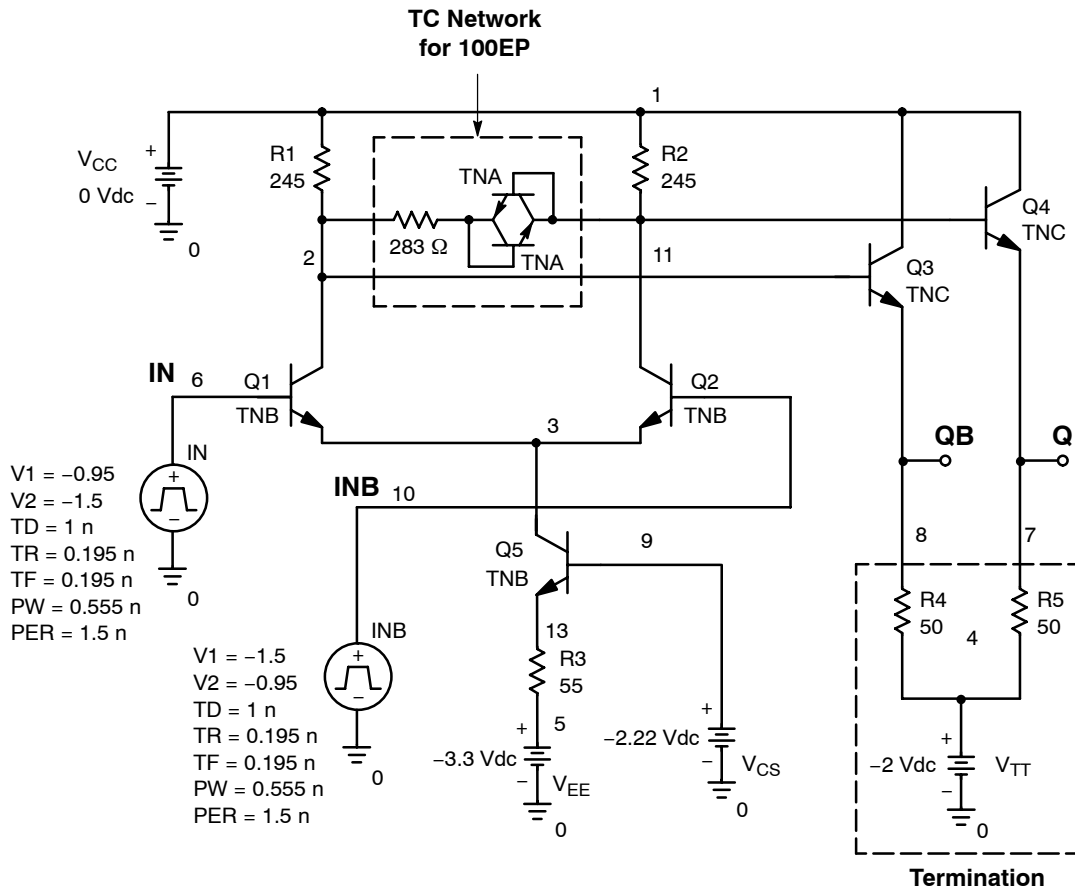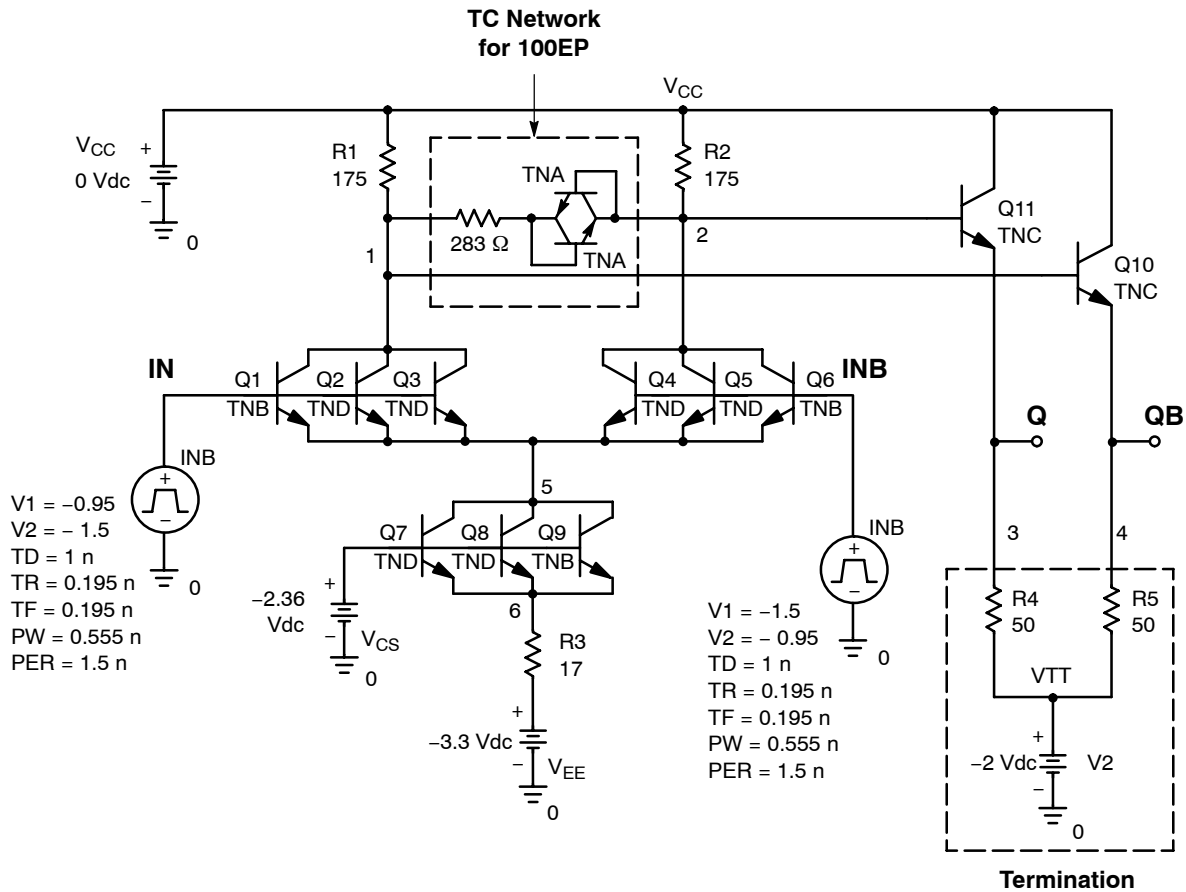
Figure 13. OBUF07

```
.SUBCKT OBUF07
Q_Q1        2 6 3 TNB
Q_Q2        11 10 3 TNB
Q_Q3        1 2 8 TNC
Q_Q4        1 11 7 TNC
Q_Q5        3 9 13 TNB
R_R1        2 1  245
R_R2        11 1  245
R_R3        5 13  55
R_R4        4 8  50
R_R5        4 7  50
V_IN        6 0
+PULSE −0.95 −1.5 1n 0.195n 0.195n 0.555n 1.5n
V_INB       10 0
+PULSE −1.5 −0.95 1n 0.195n 0.195n 0.555n 1.5n
V_VEE       5 0 −3.3Vdc
V_VCC       1 0 0Vdc
V_VTT       4 0 −2Vdc
V_VCS       9 0 −2.22Vdc
.END OBUF07
```

**TC Network
for 100EP**

Figure 14. OBUF08

```
.SUBCKT OBUF08 IN INB VCC VCS VEE VTT
Q_Q1        1 IN 5 TNB
Q_Q2        1 IN 5 TND
Q_Q3        1 IN 5 TND
Q_Q4        2 INB 5 TND
Q_Q5        2 INB 5 TND
Q_Q6        2 INB 5 TNB
Q_Q7        5 VCS 6 TND
Q_Q8        5 VCS 6 TND
Q_Q9        5 VCS 6 TNB
Q_Q10       VCC 1 4 TNC
Q_Q11       VCC 2 3 TNC
R_R1        1 VCC   175
R_R2        2 VCC   175
R_R3        VEE 6   17
R_R4        VTT 3   50
R_R5        VTT 4   50
V_INB       INB 0
+PULSE −1.5 −0.95 1n 0.195n 0.195n 0.555n 1.5n
V_IN        IN 0
+PULSE −0.95 −1.5 1n 0.195n 0.195n 0.555n 1.5n
V_VEE       VEE 0 −3.3Vdc
V_VTT       VTT 0 −2Vdc
V_VCS       VCS 0 −2.36Vdc
V_VCC       VCC 0 0Vdc
.END OBUF08
```

**TC Network
for 100EP**

Figure 15. OBUF09
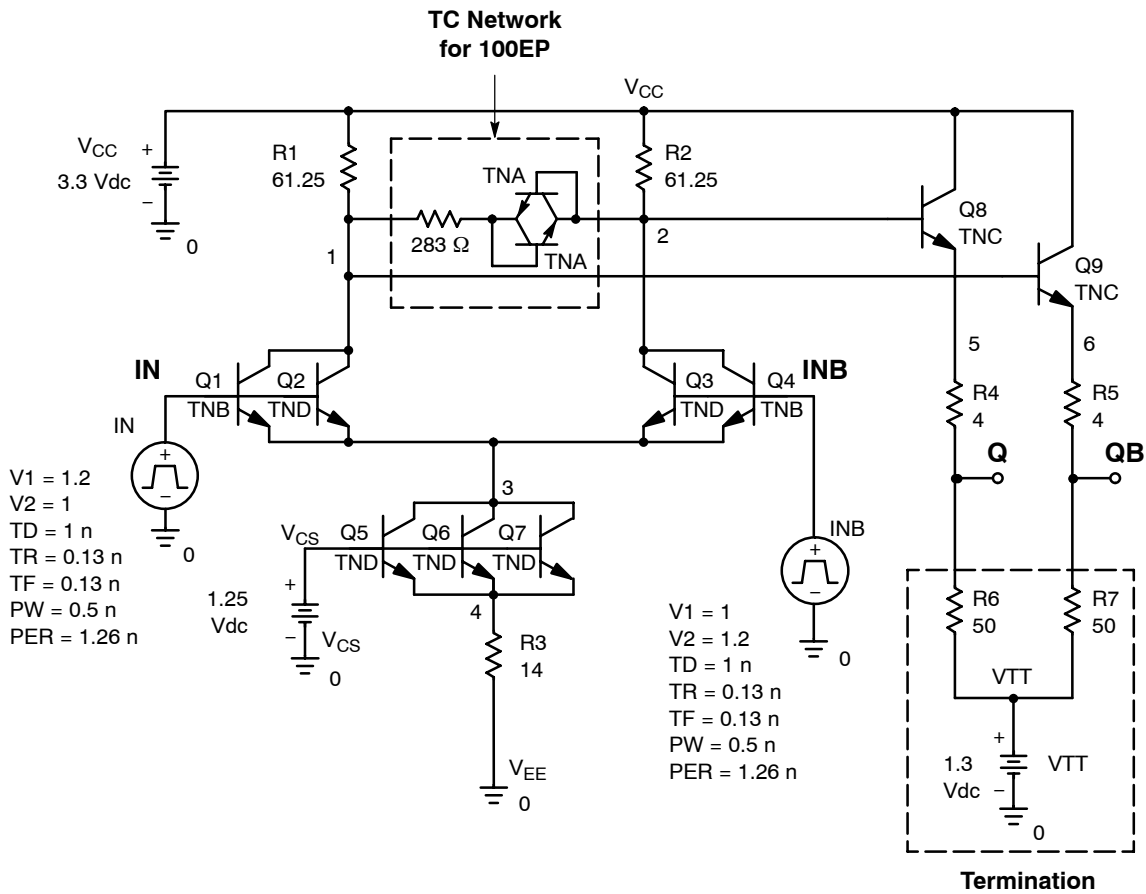
```
.SUBCKT OBUF09 IN INB VCC VCS VTT VEE Q QB
Q_Q1      1 IN 3 TNB
Q_Q2      1 IN 3 TND
Q_Q3      2 INB 3 TND
Q_Q4      2 INB 3 TNB
Q_Q5      3 VCS 4 TND
Q_Q6      3 VCS 4 TND
Q_Q7      3 VCS 4 TND
Q_Q8      VCC 2 5 TNC
Q_Q9      VCC 1 6 TNC
R_R1      1 VCC  61.25
R_R2      2 VCC  61.25
R_R3      VEE 4  14
R_R4      Q 5  4
R_R5      QB 6  4
R_R6      VTT Q  50
R_R7      VTT QB  50
V_INB     INB 0
+PULSE 1 1.2 1n 0.13n 0.13n 0.5n 1.26n
V_IN      IN 0
+PULSE 1.2 1 1n 0.13n 0.13n 0.5n 1.26n
V_VCS     VCS 0 1.25Vdc
V_VCC     VCC 0 3.3Vdc
V_VTT     VTT 0 1.3Vdc
.END OBUF09
```
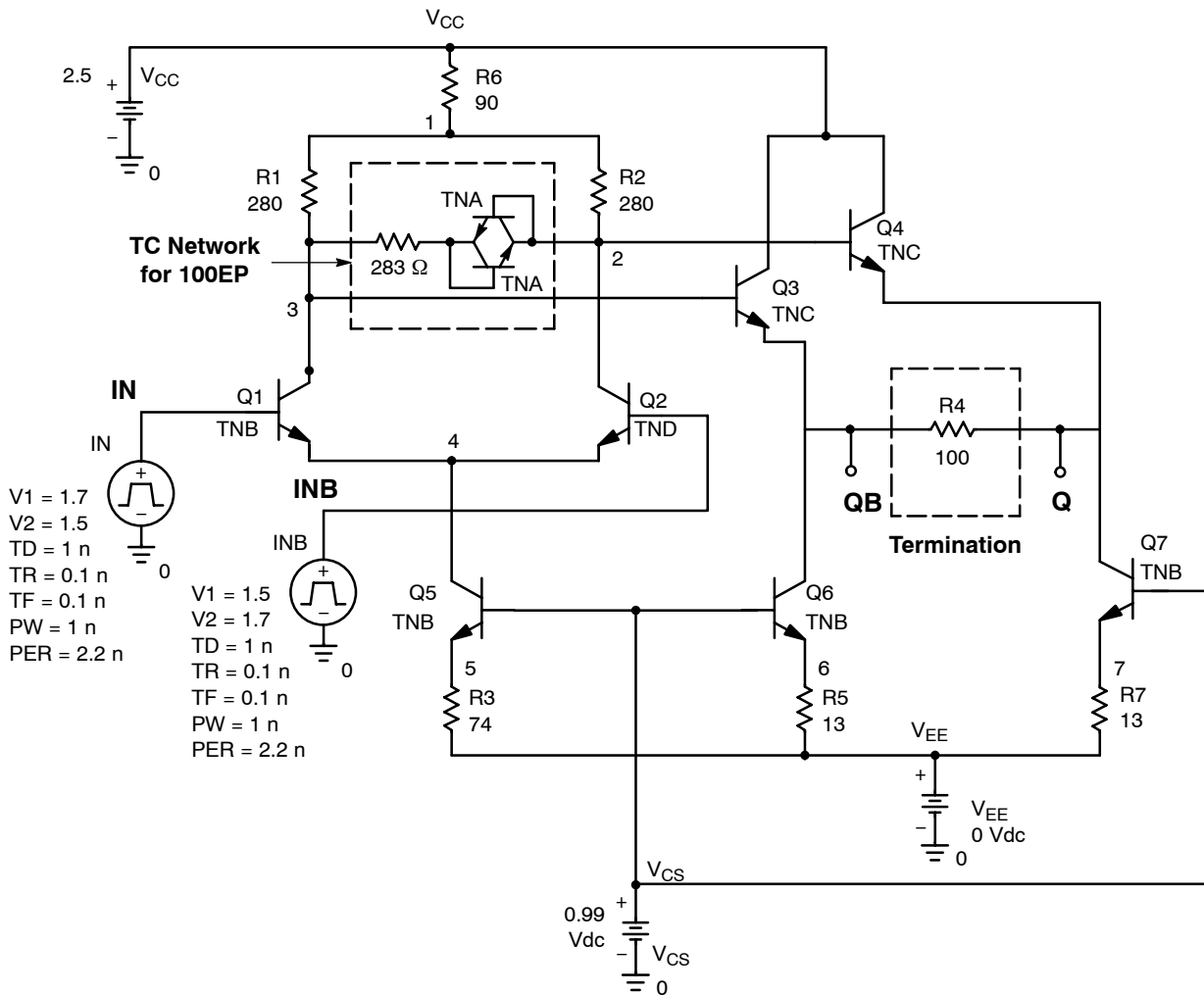
Figure 16. OBUF10

```
.SUBCKT OBUF10 IN INB VCC VCS VEE Q QB
Q_Q1      3 IN 4 TNB
Q_Q2      2 INB 4 TNB
Q_Q3      VCC 3 QB TNC
Q_Q4      VCC 2 Q TNC
Q_Q5      4 VCS 5 TNB
Q_Q6      QB VCS 6 TNB
Q_Q7      Q VCS 7 TNB
R_R1      3 1  295
R_R2      2 1  295
R_R3      VEE 5  64.3
R_R4      QB Q  100
R_R5      VEE 6  10
R_R6      1 VCC  61.25
R_R7      VEE 7  10
V_IN      IN 0
+PULSE 1.5 1.7 1n 0.1n 0.1n 1n 2.6n
V_INB     INB 0
+PULSE 1.7 1.5 1n 0.1n 0.1n 1n 2.6n
V_VCC     VCC 0 2.5
V_VEE     VEE 0 0Vdc
V_VCS     VCS 0 0.99Vdc
.END OBUF10
```
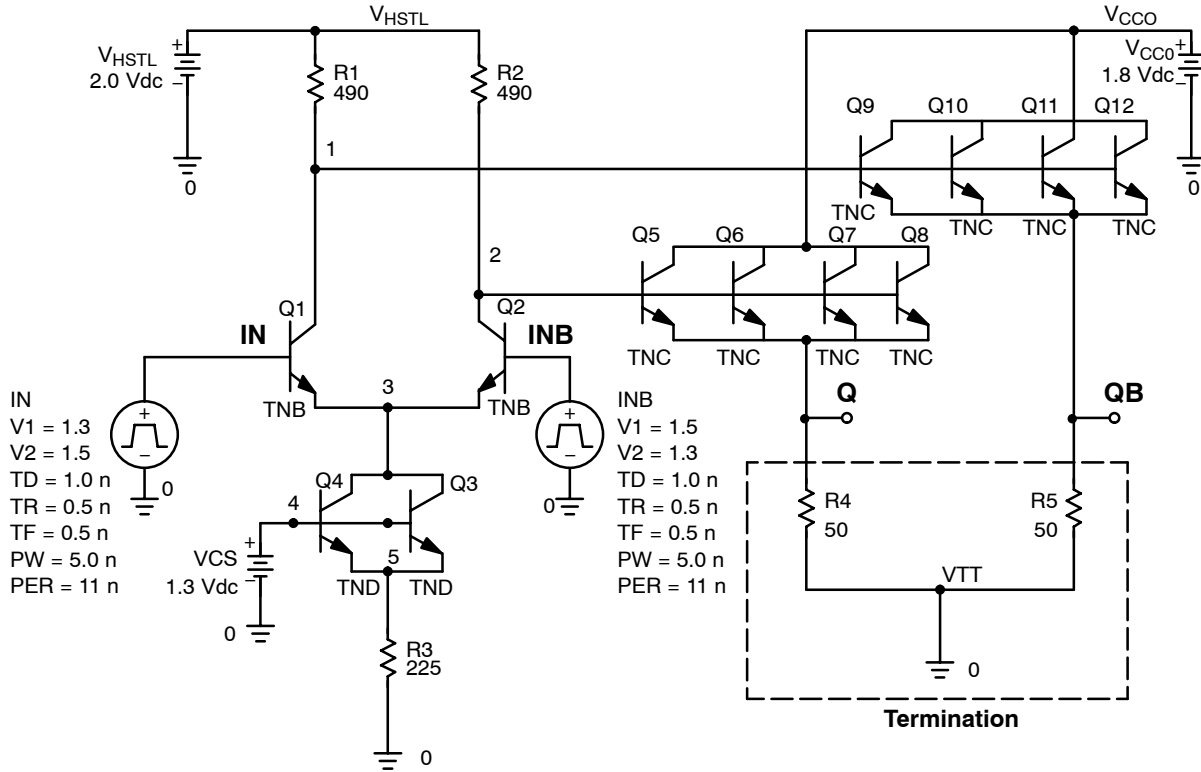
Figure 17. OBUF11

```
.SUBCKT OBUF11 IN INB VCCO VHSTL Q QB
Q_Q1      1 IN 3 TNB
Q_Q2      2 INB 3 TNB
Q_Q3      3 4 5 TND
Q_Q4      3 4 5 TND
Q_Q5      VCCO 2 Q TNC
Q_Q6      VCCO 2 Q TNC
Q_Q7      VCCO 2 Q TNC
Q_Q8      VCCO 2 Q TNC
Q_Q9      VCCO 1 QB TNC
Q_Q10     VCCO 1 QB TNC
Q_Q11     VCCO 1 QB TNC
Q_Q12     VCCO 1 QB TNC
R_R1      1 VHSTL  490
R_R2      2 VHSTL  490
R_R3      0 5  225
R_R4      0 Q  50
R_R5      0 QB  50
V_IN      IN 0
+PULSE 1.3 1.5 1n 0.5n 0.5n 5n 11n
V_INB     INB 0
+PULSE 1.5 1.3 1n 0.5n 0.5n 5n 11n
V_VCCO    VCCO 0 1.8Vdc
V_VHSTL   VHSTL 0 2.0Vdc
V_VCS     4 0 1.3Vdc
.END OBUF11
```
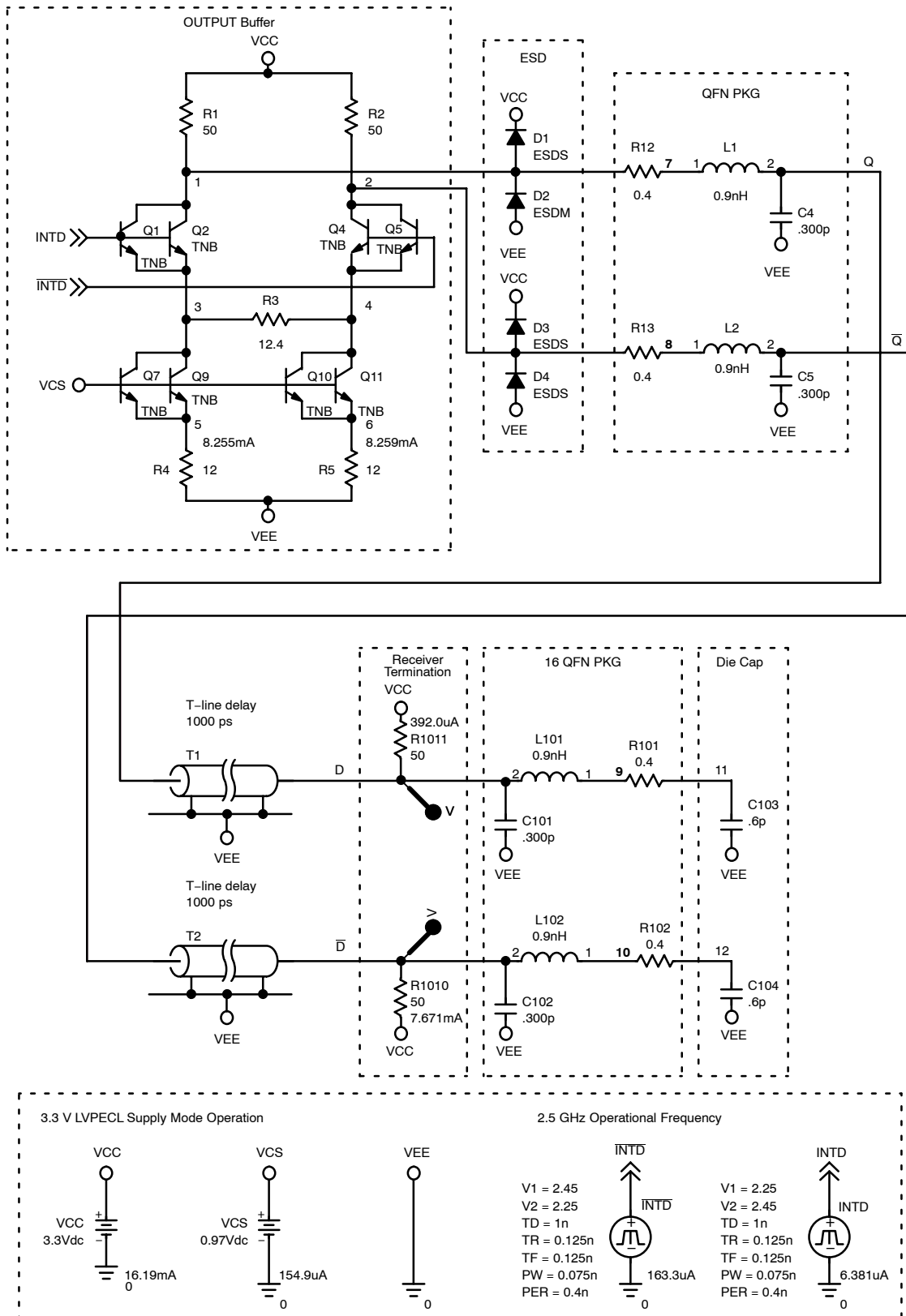
Figure 18. OBUF12 Driving Typical Receiver with Termination and 1000 ps T−Line Delay

Netlist for OBUF12 Driving Typical Receiver with Termination and 1000 ps T-line delay
```
V_VCC    $G_VCC 0 3.3Vdc
V_VCS    $G_VCS 0 0.97Vdc
V_INTD   INTD 0  +PULSE 2.25 2.45 1n 0.125n 0.125n 0.075n 0.4n
V_INTDb  INTDB 0  +PULSE 2.45 2.25 1n 0.125n 0.125n 0.075n 0.4n
```

```
.SUBCKT OBUF12 VCC VCS VEE INT INTb Q Qb
Q_Q1     1 INTD 3 TNB
Q_Q10    4 $G_VCS 6 TNB
Q_Q11    4 $G_VCS 6 TNB
Q_Q2     1 INTD 3 TNB
Q_Q4     2 INTDB 4 TNB
Q_Q5     2 INTDB 4 TNB
Q_Q7     3 $G_VCS 5 TNB
Q_Q9     3 $G_VCS 5 TNB
D_D1     1 $G_VCC ESDS
D_D2     0 1 ESDM
D_D3     2 $G_VCC ESDS
D_D4     0 2 ESDS
C_C4     0 Q  .300p
C_C5     0 QB  .300p
R_R1     1 $G_VCC  50
R_R2     2 $G_VCC  50
R_R3     4 3  12.4
R_R4     0 5  12
R_R5     0 6  12
L_L1     7 Q  0.9nH
L_L2     8 QB  0.9nH
.END OBUF12
.SUBCKT RECEIVER VCC VEE D Db
T_T1     Q 0 D 0 Z0=50 TD=1000ps
T_T2     QB 0 DB 0 Z0=50 TD=1000ps
C_C101   0 D  .300p
C_C102   0 DB  .300p
C_C103   0 11  .6p
C_C104   0 12  .6p
L_L101   9 D  0.9nH
L_L102   10 DB  0.9nH
R_R101   11 9  0.4
R_R1010  DB $G_VCC  50
R_R1011  D $G_VCC  50
R_R102   12 10  0.4
R_R12    1 7  0.4
R_R13    2 8  0.4
.END RECEIVER
```
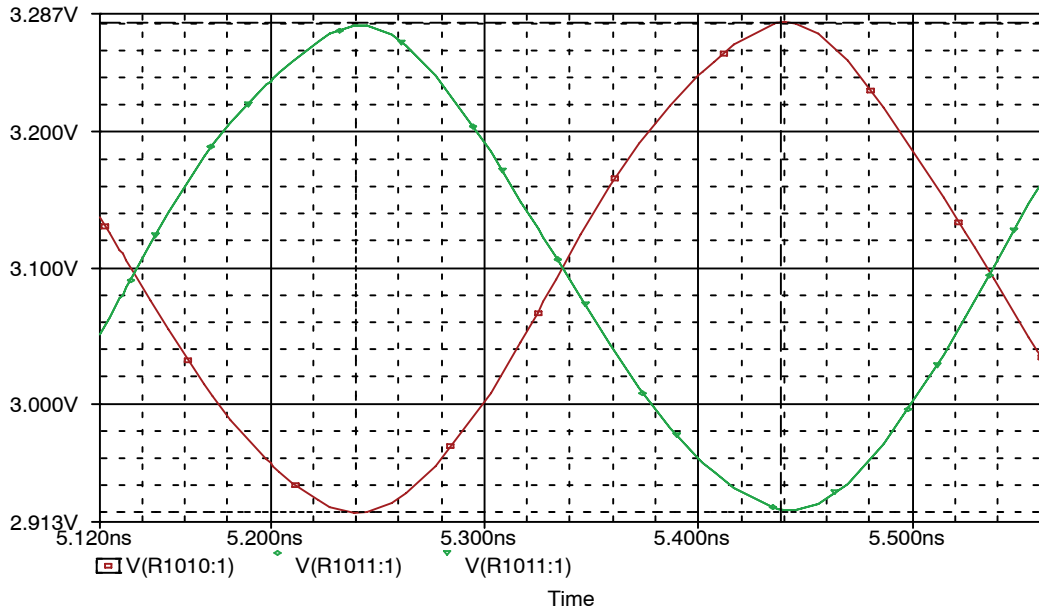
Figure 19. OBUF12 at 2.5 GHz Operation Frequency; V_{OUTamp} at 360 mV$_{PP}$; V_{OH} at 3.28 V; V_{OL} at 2.92 V; t_r/t_f (20% – 80%) is 86 ps (With Receiver Load)
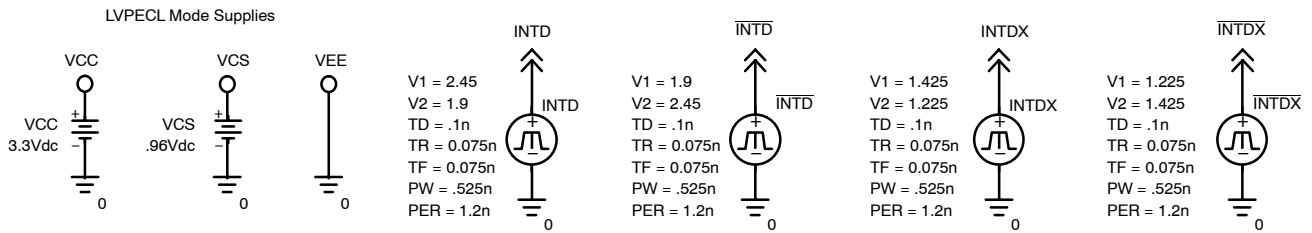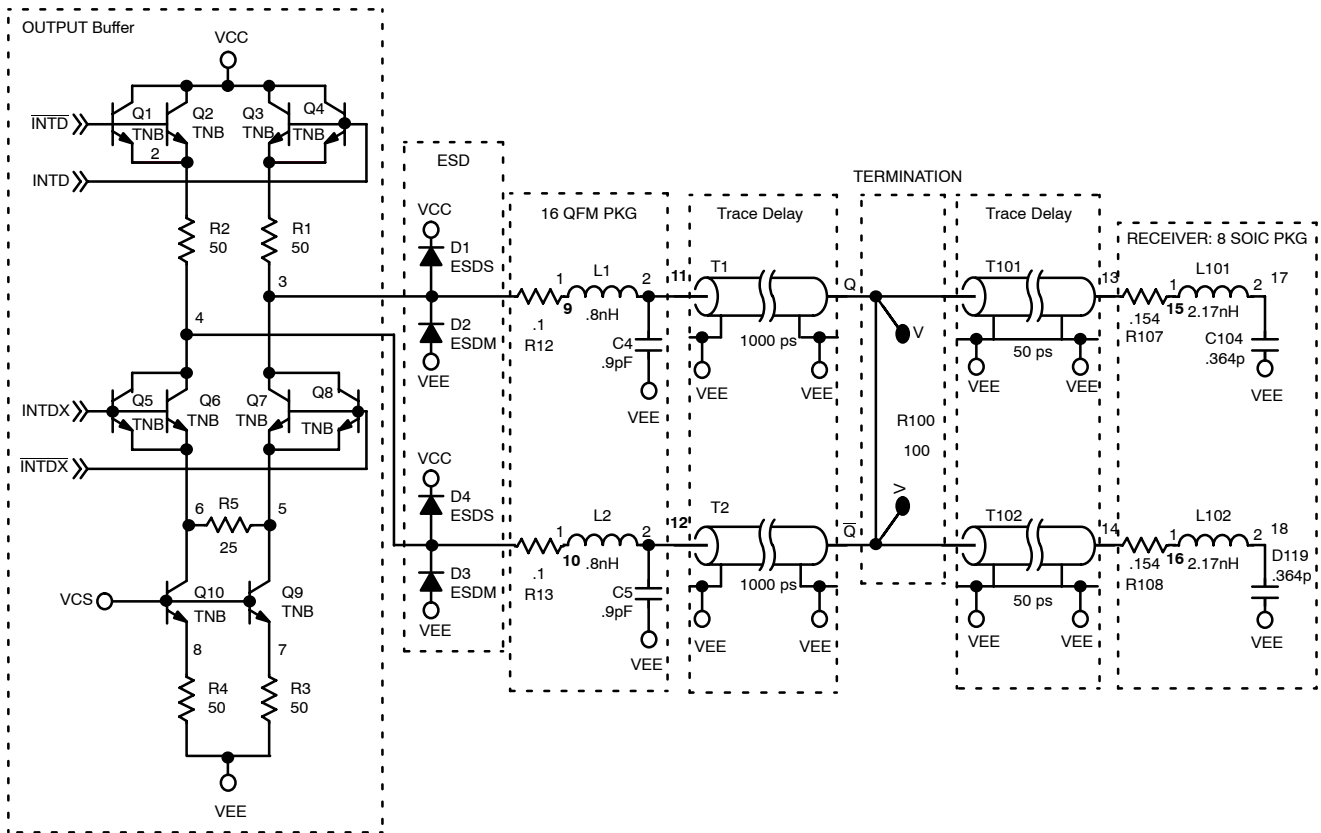
Figure 20. OBUF13 With Termination And Receiver Package Load

```
SPICE NETLIST for OBUF13:
V_VCC       $G_VCC 0 3.3Vdc
V_VCS       $G_VCS 0 .96Vdc
V_INTD      INTD 0  PULSE 2.45 1.9 .1n 0.075n 0.075n .525n 1.2n
V_INTDb     INTDB 0  PULSE 1.9 2.45 .1n 0.075n 0.075n .525n 1.2n
V_INTDX     INTDX 0  PULSE 1.225 1.425 .1n 0.075n 0.075n .525n 1.2n
V_INTDXb    INTDXB 0  PULSE 1.425 1.225 .1n 0.075n 0.075n .525n 1.2n


.SUBCKT OBUF13
C_C104      0 13  .364p
C_C4        0 11  .9pF
C_C5        0 12  .9pF
C_D119      0 14  .364p
D_D1        3 $G_VCC ESDS
D_D2        0 3 ESDM
D_D3        0 4 ESDM
```

```
D_D4         4 $G_VCC ESDS
L_L1         9 11  .8nH
L_L101       11 13  2.17nH
L_L102       12 14  2.17nH
L_L2         10 12  .8nH
Q_Q1         $G_VCC INTDB 2 TNB
Q_Q10        6 $G_VCS 8 TNB
Q_Q2         $G_VCC INTDB 2 TNB
Q_Q3         $G_VCC INTD 1 TNB
Q_Q4         $G_VCC INTD 1 TNB
Q_Q5         4 INTDX 6 TNB
Q_Q6         4 INTDX 6 TNB
Q_Q7         3 INTDXB 5 TNB
Q_Q8         3 INTDXB 5 TNB
Q_Q9         5 $G_VCS 7 TNB
R_R1         3 1  50
R_R100       Q QB  100
R_R107       9 11  .154
R_R108       10 12  .154
R_R12        3 9  .1
R_R13        4 10  .1
R_R2         4 2  50
R_R3         0 7  50
R_R4         0 8  50
R_R5         5 6  25
T_T1         11 0 Q 0 Z0=50 TD=1000ps
T_T101       Q 0 9 0 Z0=50 TD=50ps
T_T102       QB 0 10 0 Z0=50 TD=50ps
T_T2         12 0 QB 0 Z0=50 TD=1000ps
.END OBUF13
```
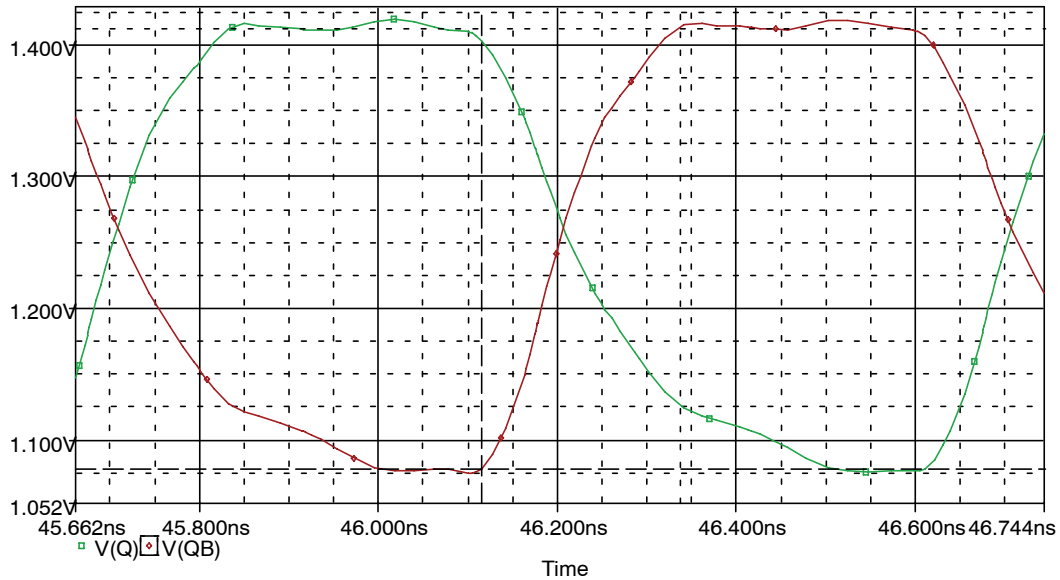

Figure 21. OBUF13 Typical Waveform at 1.0 GHz with Termination and Receiver Package Load (95ps t_r/t_f)
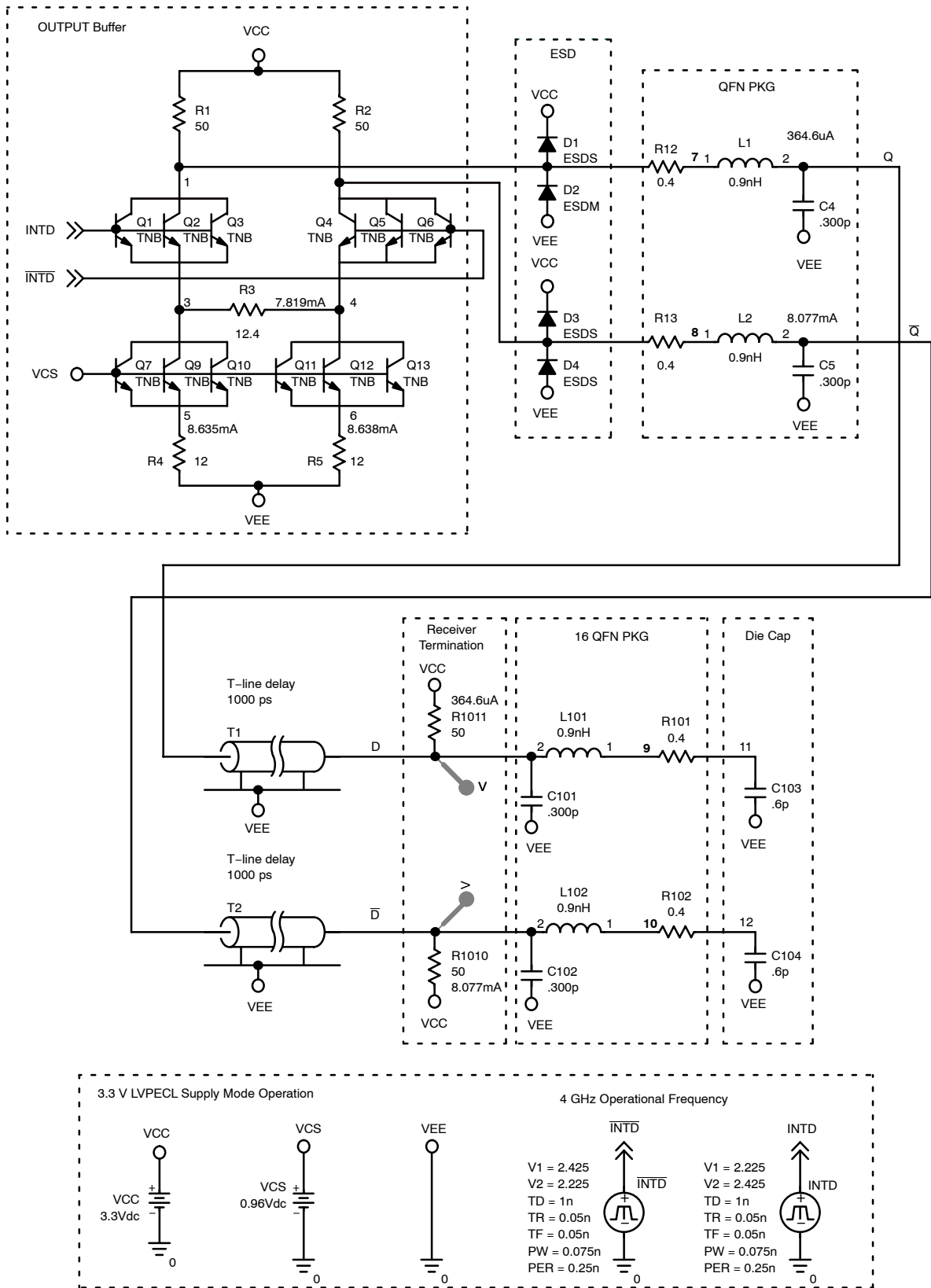
Figure 22. OBUF14 With Termination And Reciever Package Load

NETLIST for OBUF14

```
V_INTD          INTD 0  +PULSE 2.225 2.425 1n 0.05n 0.05n 0.075n 0.25n
V_INTDb         INTDB 0  +PULSE 2.425 2.225 1n 0.05n 0.05n 0.075n 0.25n
V_VCC           $G_VCC 0 3.3Vdc
V_VCS           $G_VCS 0 0.96Vdc


.SUBCKT OBUF14 VCC VCS INTD INTDb Q Qb
Q_Q1            1 INTD 3 TNB
Q_Q2            1 INTD 3 TNB
Q_Q3            1 INTD 3 TNB
Q_Q4            2 INTDB 4 TNB
Q_Q5            2 INTDB 4 TNB
Q_Q6            2 INTDB 4 TNB
Q_Q7            3 $G_VCS 5 TNB
Q_Q9            3 $G_VCS 5 TNB
Q_Q10           3 $G_VCS 5 TNB
Q_Q11           4 $G_VCS 6 TNB
Q_Q12           4 $G_VCS 6 TNB
Q_Q13           4 $G_VCS 6 TNB
R_R1            1 $G_VCC  50
R_R2            2 $G_VCC  50
R_R3            4 3  12.4
R_R4            0 5  12
R_R5            0 6  12
R_R12           1 7  0.4
R_R13           2 8  0.4
D_D1            1 $G_VCC ESDS
D_D2            0 1 ESDM
D_D3            2 $G_VCC ESDS
D_D4            0 2 ESDS
C_C4            0 Q  .300p
C_C5            0 QB  .300p
L_L1            7 Q  0.9nH
L_L2            8 QB  0.9nH
.END OBUF14
.SUBCKT RECEIVER VCC VCS D Db
T_T1            Q 0 D 0 Z0=50 TD=1000ps
T_T2            QB 0 DB 0 Z0=50 TD=1000ps
C_C101          0 D  .300p
C_C102          0 DB  .300p
C_C103          0 11  .6p
C_C104          0 12  .6p
L_L101          9 D  0.9nH
L_L102          10 DB  0.9nH
R_R101          11 9  0.4
R_R102          12 10  0.4
R_R1010         DB $G_VCC  50
R_R1011         D $G_VCC  50
.END RECEIVER
```
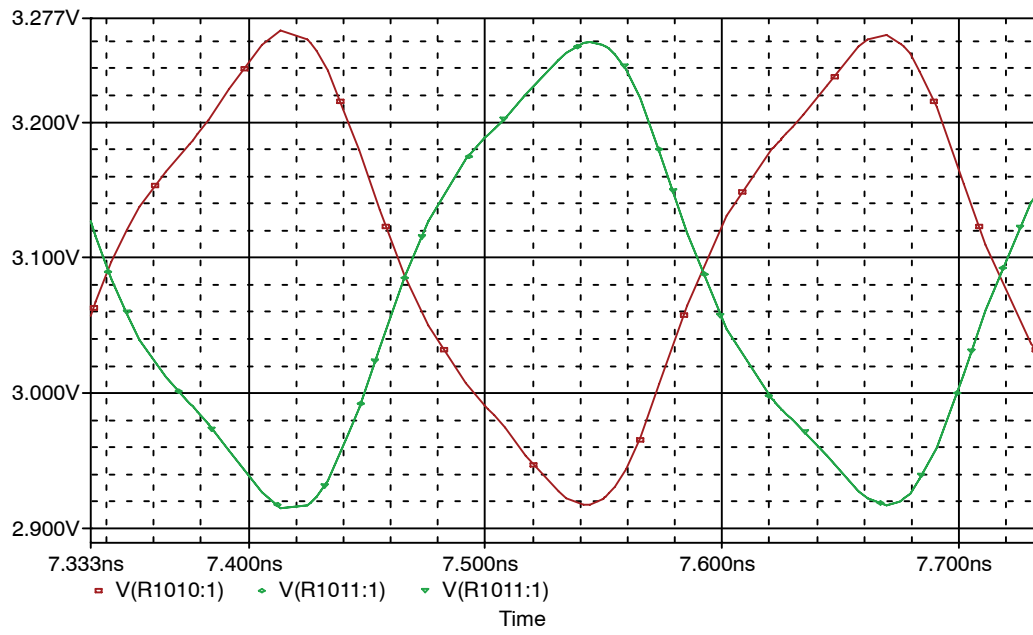
Figure 23. OBUF14 Typical Output Waveform at 4 GHz Operation; Amplitude 345 mV$_{PP}$; V$_{OL}$ 2.91, VOH 3.26 t$_r$/t$_f$ 60 ps
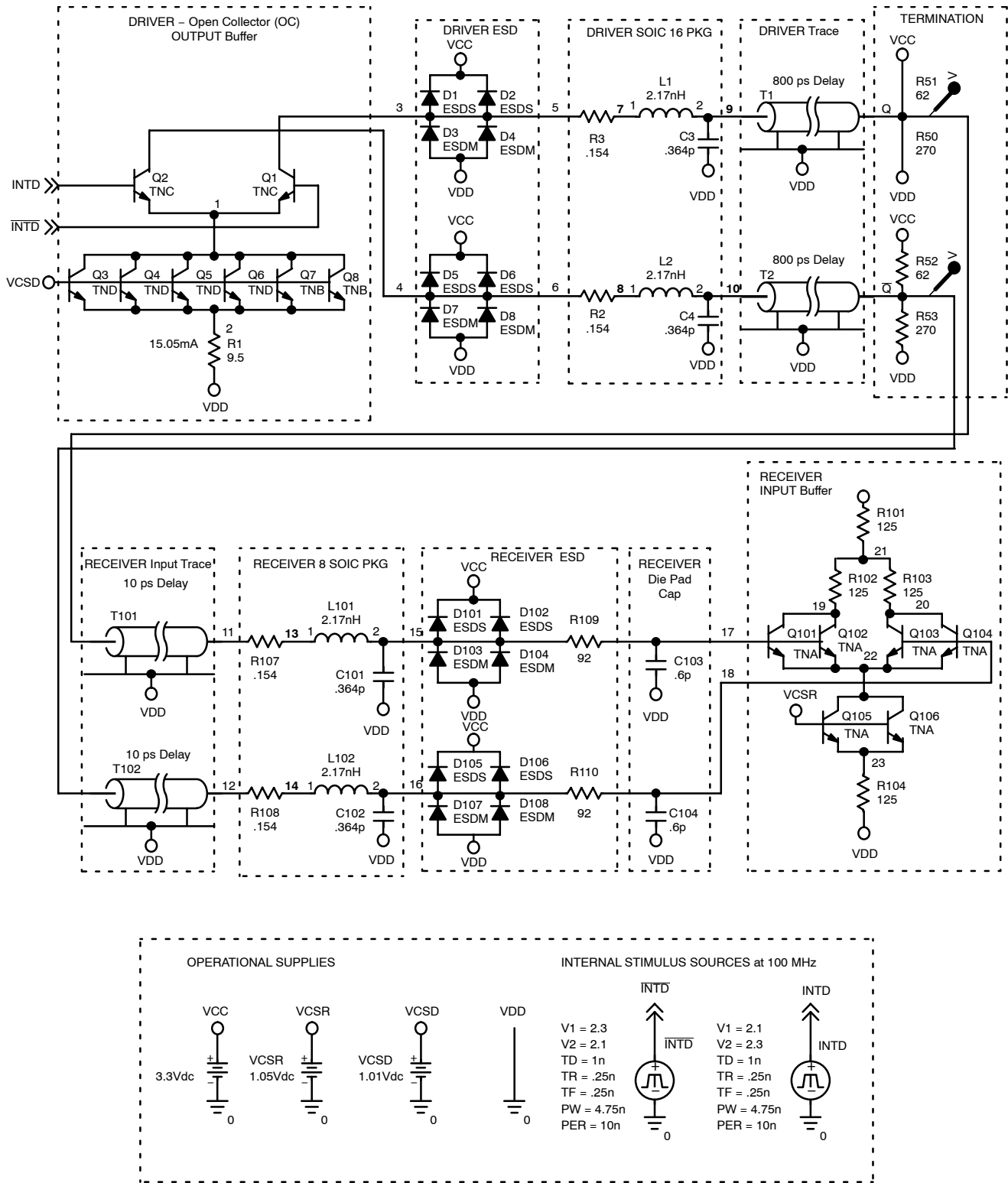
Figure 24. An OBUF15 Open Collector Output Buffer Driving A Typical LVPECL Receiver

NETLIST for OBUF15

```
V_INTD          INTD 0 PULSE 2.1 2.3 1n .25n .25n 4.75n 10n
V_INTDb         INTDB 0 PULSE 2.3 2.1 1n .25n .25n 4.75n 10n
V_VCC           $G_VCC 0 3.3Vdc
V_VCSD          $G_VCSD 0 1.01Vdc
V_VCSR          $G_VCSR 0 1.05Vdc
```

SUBCKT OBUF15

```
Q_Q1            3 INTDB 1 TNC
Q_Q2            4 INTD 1 TNC
Q_Q3            1 $G_VCSD 2 TND
Q_Q4            1 $G_VCSD 2 TND
Q_Q5            1 $G_VCSD 2 TND
Q_Q6            1 $G_VCSD 2 TND
Q_Q7            1 $G_VCSD 2 TNB
Q_Q8            1 $G_VCSD 2 TNB
R_R1            0 2  9.5
D_D1            3 $G_VCC ESDS
D_D2            3 $G_VCC ESDS
D_D3            0 3 ESDM
D_D4            0 3 ESDM
D_D5            4 $G_VCC ESDS
D_D6            4 $G_VCC ESDS
D_D7            0 4 ESDM
D_D8            0 4 ESDM
R_R2            4 8  .154
R_R3            3 7  .154
L_L1            7 9  2.17nH
L_L2            8 10  2.17nH
C_C3            0 9  .364p
C_C4            0 10  .364p
T_T1            9 0 Q 0 Z0=50 TD=800ps
T_T2            10 0 QB 0 Z0=50 TD=800ps
R_R50           Q 0  270
R_R51           Q $G_VCC  62
R_R52           QB $G_VCC  62
R_R53           0 QB  270
.END
```

SUBCKT RECEIVER

```
C_C101          0 15  .364p
C_C102          0 16  .364p
C_C103          0 17  .6p
C_C104          0 18  .6p
D_D101          15 $G_VCC ESDS
D_D102          15 $G_VCC ESDS
D_D103          0 15 ESDM
D_D104          0 15 ESDM
D_D105          16 $G_VCC ESDS
D_D106          16 $G_VCC ESDS
D_D107          0 16 ESDM
D_D108          0 16 ESDM
L_L101          13 15  2.17nH
L_L102          14 16  2.17nH
Q_Q101          19 17 22 TNA
Q_Q102          19 17 22 TNA
Q_Q103          20 18 22 TNA
Q_Q104          20 18 22 TND
Q_Q105          22 $G_VCSR 23 TNA
Q_Q106          22 $G_VCSR 23 TNA
R_R101          21 $G_VCC  125
R_R102          19 21  125
R_R103          20 21  125
```

```
R_R104          0  23   125
R_R107          11 13   .154
R_R108          12 14   .154
R_R109          15 17   92
R_R110          16 18   92
T_T101          Q  0 11 0 Z0=50 TD=10ps
T_T102          QB 0 12 0 Z0=50 TD=10ps
.END RECEIVER
```
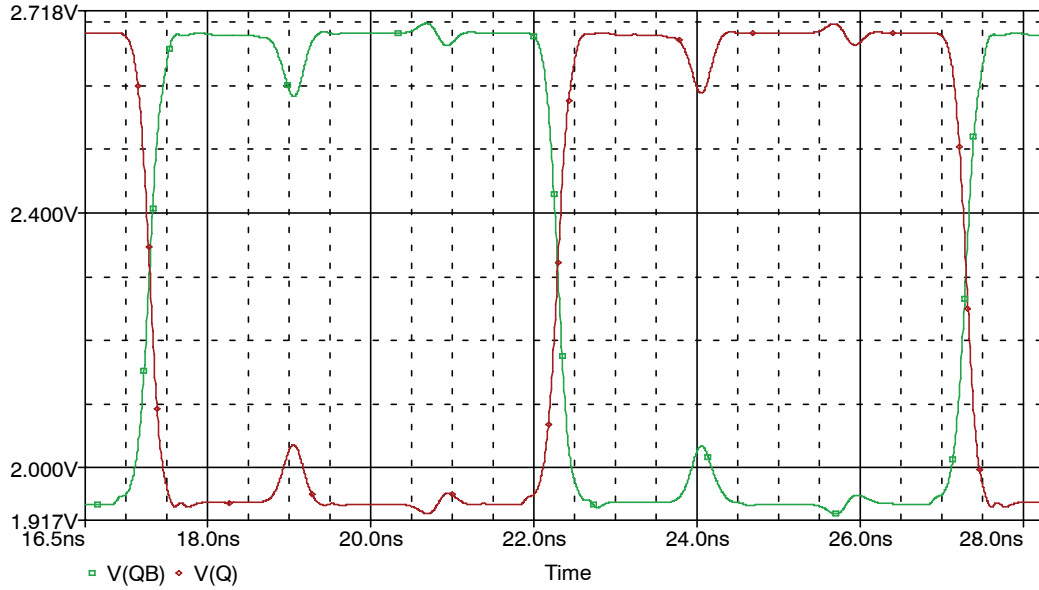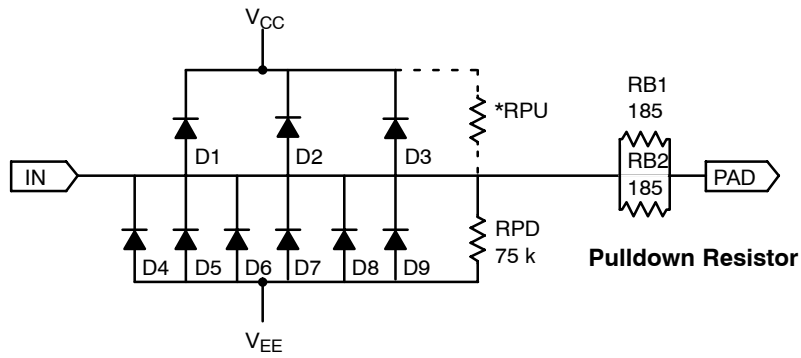

Figure 25. OBUF15 Output Driving LVPECL Receiver Typical Waveforms at 100 MHz; V_{OH} 1.94 V; V_{OL} 2.68 V; V_{amp} 736 mV; 199 ps t_r/t_f at 2.09 V and 2.53 V (20%/80%)

Figure 26. Input ESD

```
.SUBCKT IN_ESD VCC VEE IN PAD
D1        IN      VCC       ESDM
D2        IN      VCC       ESDM
D3        IN      VCC       ESDM
D4        VEE     IN        ESDM
D5        VEE     IN        ESDS
D6        VEE     IN        ESDM
D7        VEE     IN        ESDS
D8        VEE     IN        ESDM
D9        VEE     IN        ESDS
RPD       IN      VEE       75K
RPU       IN      VCC       36.5K
RB1       IN      PAD       185
RB2       IN      PAD       185
.ENDS IN_ESD
```
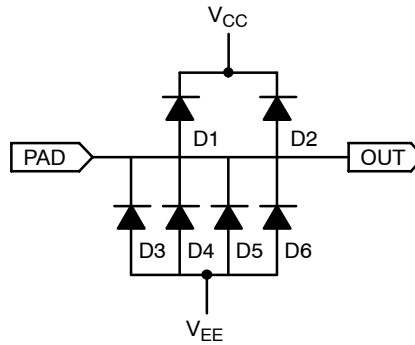

Figure 27. Output ESD

```
.SUBCKT OUT_ESD VCC VEE OUT
D1        OUT     VCC       ESDM
D2        OUT     VCC       ESDM
D3        VEE     OUT       ESDM
D4        VEE     OUT       ESDS
D5        VEE     OUT       ESDM
D6        VEE     OUT       ESDS
.ENDS OUT_ESD
```

The following is an example of a typical run−deck file which might be used to simulate Figure 28 to produce output waveform shown in Figure 29.

TYPICAL TEST CIRCUIT

```
VCC     VCC     0       0V
VEE     VEE     0       −3.3V
VCS     VCS     0       −2.2V
VTT     VTT     0       −2.0V
VIN     IN      0       PULSE(−1.7 −0.95 5NS 5NS 5NS 50NS 110NS)
VINB    INB     0       PULSE(−0.95 −1.7 5NS 5NS 5NS 50NS 110NS)
.GROUND 0
.TRAN   0.2NS   120NS
```
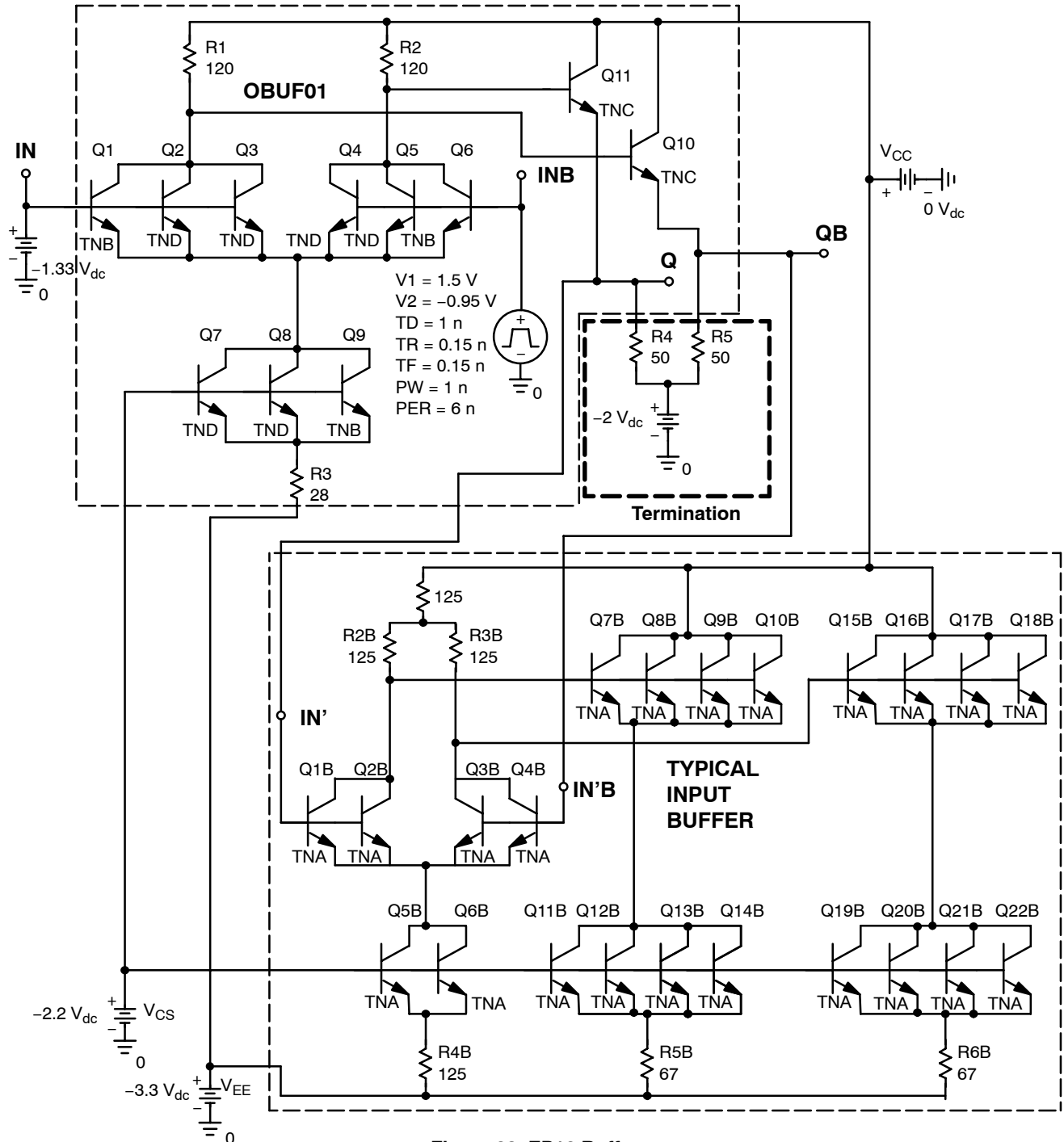

Figure 28. EP16 Buffer
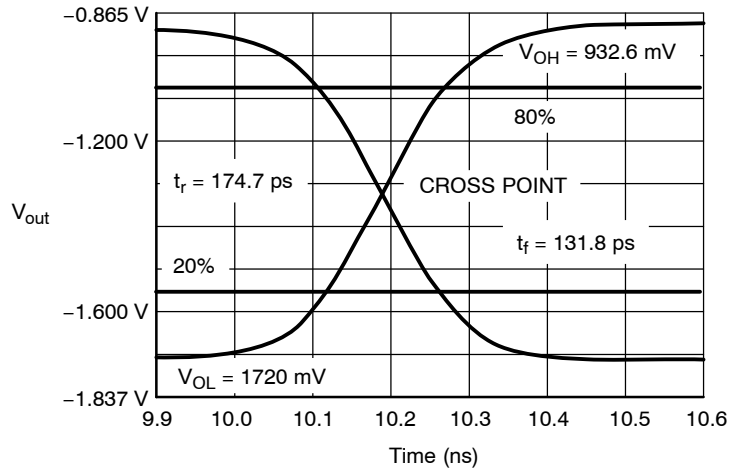
Figure 29. Typical Generic Output Waveform
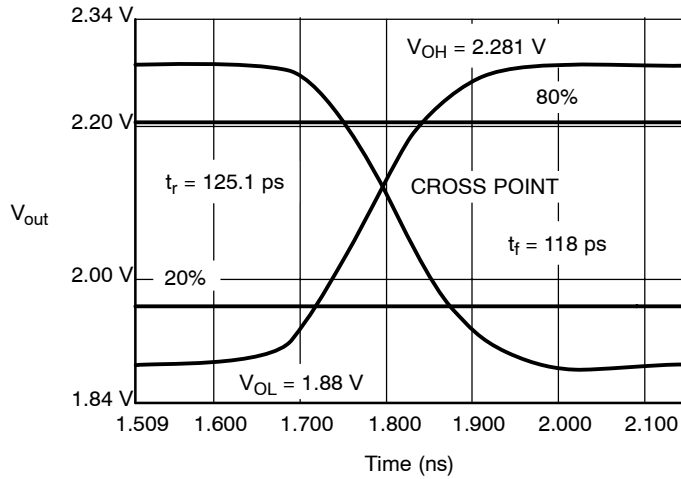
**Figure 30. OBUF09 Reduced Swing Output
Waveform (EP40/140)**
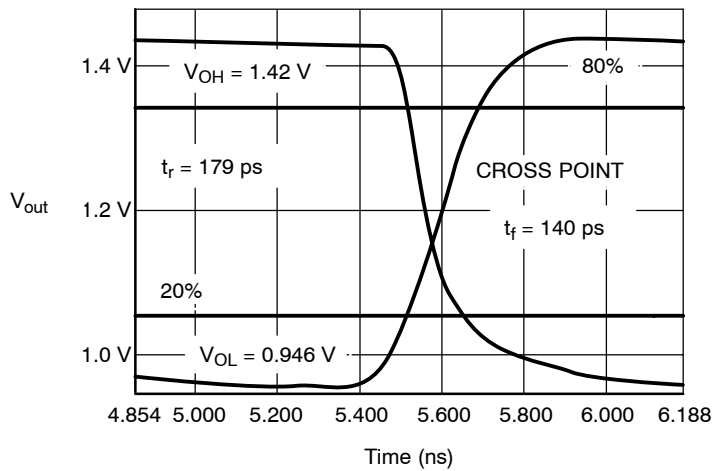
Figure 31. LVDS Output Waveform (EP210's)

```
******************   Transistor and Diodes Nominal SPICE Models*   *******************


*************************************************************************
.MODEL TNA NPN (IS=8.12e-18 BF=192 NF=1 VAF=75.6 IKF=1.49e-02
+ ISE=9.14e-17 NE=2 BR=15.8 VAR=2.76 IKR=2.2e-03 ISC=2.62e-16
+ NC=1.578 RB=327 IRB=4.8e-05 RBM=0.001 RE=10 RC=15 CJE=2.0e-14
+ VJE=.8867 MJE=.2868 TF=9.02e-12 ITF=7.6e-03 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS
+ CJC=5.6e-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=4.8e-15 VJS=.4193 MJS=.2563
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
*************************************************************************
.MODEL TNB NPN (IS=2.71e-17 BF=172 NF=1 VAF=71.4 IKF=4.38e-02
+ ISE=1.33e-15 NE=2 BR=17.9 VAR=2.76 IKR=3.0e-03 ISC=2.22e-16
+ NC=1.578 RB=67 IRB=6.47e-05 RBM=0.001 RE=3 RC=4 CJE=5.09e-14
+ VJE=.8867 MJE=.2868 TF=9.02e-12 ITF=2.53e-02 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS
+ CJC=20.6e-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=1.7e-14 VJS=.4193 MJS=.2563
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
*************************************************************************
.MODEL TNC NPN (IS=6.55e-17 BF=103 NF=1 VAF=90 IKF=2.91e-01
+ ISE=8.85e-15 NE=2 BR=15.7 NR=1 VAR=3.82 IKR=2.01e-02 ISC=1.48e-15
+ NC=2 RB=10.5 IRB=4.39e-04 RBM=0.29 RE=0.351 RC=9 CJE=3.5e-13
+ VJE=.8167 MJE=.1973 TF=8.99e-12 ITF=1.3e-01 XTF=5.67 VTF=1.86 PTF=41.43 TR=6.405e-10
+ CJC=1.4e-13 VJC=.6401 MJC=.2674 XCJC=1 CJS=9.3e-14 VJS=.5002 MJS=.1706
+ EG=1.135 XTI=4.177 XTB=0.6322 FC=0.961)
*************************************************************************
.MODEL TND NPN (IS=1.36e-17 BF=180 NF=1 VAF=87.6 IKF=2.19e-02
+ ISE=6.65e-16 NE=2 BR=16.9 VAR=2.76 IKR=1.5e-03 ISC=1.11e-16
+ NC=1.578 RB=136 IRB=3.24e-05 RBM=0.001 RE=6 RC=8 CJE=1.02e-13
+ VJE=.8867 MJE=.2868 TF=9.02e-12 ITF=1.27e-02 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS
+ CJC=10.3e-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=9.94e-15 VJS=.4193 MJS=.2563
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
*************************************************************************
.MODEL TNE NPN (IS=2.68e-18 BF=223 NF=1 VAF=56.0 IKF=3.96e-03
+ ISE=3.07e-17 NE=2 BR=13.9 VAR=2.76 IKR=7.23e-04 ISC=6.08e-17
+ NC=1.578 RB=386 IRB=1.3e-05 RBM=0.001 RE=26 RC=28 CJE=6.0e-15
+ VJE=.8867 MJE=.2868 TF=9.02PS ITF=2.6e-03 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS
+ CJC=3.4e-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=3.4e-15 VJS=.4193 MJS=.2563
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
*************************************************************************
.MODEL ESDM D (IS=1.55E-14 CJO=160fF RS=12 VJ=.58 M=.25 BV=9)
*************************************************************************
.MODEL ESDS D (IS=1.55E-14 CJO=29fF VJ=.624 M=.571)
*************************************************************************
*SPICE MODELS 4.5
```

APPENDIX: PACKAGE RLC MODELS

	Package	R (Ω)	L (nH)	C (pF)
1	SOIC−8		1.5	0.188
2	TSSOP−8	0.048	1.9	0.089
3	SOIC−20 W	0.136	3.04	0.158
4	TSSOP−20	0.033	1.76	0.98
5	QFN−24	0.055	1.29	0.05
6	LQFP−32	0.67	2.38	0.13
7	LQFP−52	0.88	3.3	0.072
8	LQFP−64	0.10	0.67	0.05
9	QFN−16	0.039	0.75	0.13
10	QFN−32	0.42	1.39	0.142
11	TSSOP−10	0.048	1.9	0.089
12	SOIC−16	0.152	2.714	0.364
13	TSSOP−16	0.044	0.82	0.41

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