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# **EPT SPICE Modeling Kit**

Prepared by Paul Shockman ON Semiconductor Logic Applications Engineering



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# **APPLICATION NOTE**

need to be adjusted. The parasitic capacitance and inductance should be adjusted accordingly.

### Modeling

The bias driver schematics for VCS and V1 generation are not included in this kit, as they are unnecessary for interconnection simulation. In addition their use would result in a relatively large in simulation time. Alternatively the internal reference voltages should be driven with ideal constant voltage sources.

Parameter	Typical Level	Worst Case
VCS	VEE+1.3V	±50mV
V1	VEE+2.1V	±50mV

This model kit is intended for simulations within the specified power supply range. If supply voltages drop below minimum specification, VCS and V1 can no longer be assumed to be constant. Thus, this model kit can not be used for power up or power down simulations. The 10K ohm resistor should NOT be simulated as simple SPICE resistor because it is fabricated by a diffusion step in wafer processing and there is an associated parasitic. The following subcircuit should be used to enhance the performance of the simulation.

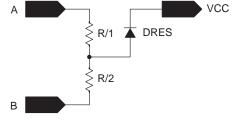


Figure 1. Resistor Model

#### Objective

The objective of this kit is to provide customers with enough schematic and SPICE parameter information to perform system level interconnect modeling with the ON Semiconductor ECLinPS Plus<sup>™</sup> Translator EPT family. The EPT devices MC100EPT2xD are single or dual supply 1 or 2 Bit translators between the TTL and ECL/PECL worlds. Single supply devices translate between TTL and PECL, dual supply devices translate to or from negative supplied ECL. All devices are designed as 100K compatible 100EPT2x.

The kit contains representative schematics and model files for the I/O circuits used by the EPT20 and EPT22 devices. The package model should be placed on all external inputs, outputs and supply pins.

#### Input and Output Schematics

The TTL–PECL Translator function uses circuit schematics LVTTL01 and LVTTL02 for references diagrams to the SPICE netlists.

All inputs and outputs of the ELT family are protected by ESD protection circuitry. The ESD circuit, IN\_ESD, is used for TTL Input and OUT\_ESD for PECL outputs.

If the user would like to just simulate the output behavior of an TTL output the TTL\_OUT circuit can be stimulated with internal signals.

To all external pins the package model, LINES, needs to be added. If users want to reduce simulation time and just simulate 1 channel or only the output of a circuit, they need to take care of the correct power supply management. The channels share power supply pins. Dynamic ICC current will add up at power pins. When a simulation is performed with only one channel, the package models of the power pins

.SUBCKT RESK A B VCC params: R=10000 \* Assumes Sheet Rho=5000HM, Resistor Width=10U, and Cap in Farads. Ra A 1 {R/2} TC=900U Rb 1 B {R/2} TC=900U D1 1 VCC DRES .MODEL DRES D + (IS=3.7E-16 + CJO=0.265E-16\*R+29E-16) .ENDS RESK

The nodes in the model files and the schematics are:

Name Node Description

VCC 100 3.3V High rail power supply

VEE 200 0.0V Lowest Rail Power supply

VCS 300 1.24 Current Source Base Voltage (VEE+1.3V)V

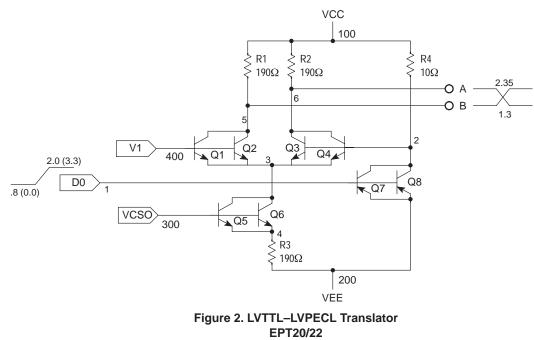
V1 400 2.1 Internal TTL Transfer Reference Supply

VTT 500 1.3V External termination sink supply (VCC-2V)

VIN 51 PULSE (.8 to 2.0, tr/tf 5NS, PW 20NS, PER 50NS)

Temperature coefficients are annotated (\* TC=).

For typical load ECL and PECL outputs should be terminated 50ohm to VTT=VCC—2V. TTL outputs are loaded with 20pF to GROUND and 5000HM to GROUND.



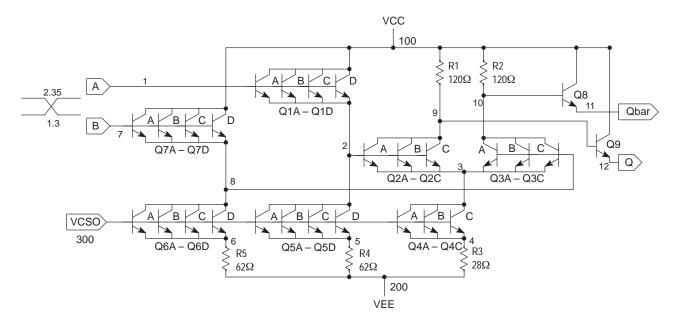
LVPECL output

For LVTTL01, the following transitors are used:

Q1 TRANA

\*\*\*

- Q2 TRANA
- Q3 TRANA
- Q4 TRANA
- Q5 TRANA
- Q6 TRANA Q7 TRANE
- 08 TRANE



#### Figure 3. LVTTL–LVPECL Translator EPT20/22 LVPECL output

For LVTTL02 the following transitors are used:

. . . . . .

 Q1A-D
 TRANA

 Q2A-C
 TRANB

 Q3A-C
 TRANB

 Q4A-C
 TRANB

 Q5A-D
 TRANA

 Q6A-D
 TRANA

 Q7A-D
 TRANA

 Q8
 TRAND

 Q9
 TRAND

.TRA	AN	0.2	2NS	120NS	5					
XLV	TTL01	100	D	200	300	400	1	5	6	LVTTL01
XLV	TTL02	100	C	200	300	5	б	11	12	LVTTL02
XIN	ESD	100	C	200	51	1	IN_ESD			
XOU	TESD	100	C	200	11	OUT_ESD				
XOU	TESDB	100	C	200	12	OUT_ESD				
XQB	TERM	500	C	12	RTERM					
XQTI	ERM	500	C	11	RTERM					
.SUI Q1 Q2	ВСКТ 1 5 5	LVTT) 400 400	3	100 20 200 200	0 300 TRANA TRANA	400 1 5 6	6			
Q3	6	2	3	200	TRANA					
Q4	6	2	3	200	TRANA					
Q5	3	300	4	200	TRANA					
Q6	3	300	4	200	TRANA					
Q7	2	1	200	200	TLS					
Q8	2	1	200	200	TLS					
R1	100	5	190							
* T(	C=0.20	5M, (	0.9U							
R2	100	6	190							

\* TC=0.26M, 0.9U R3 4 200 190 \* TC=0.26M, 0.9U R4 100 2 10000 \* TC=0.26M, 0.9U .ENDS LVTTL01

CIID		VTTLO	ე .	100	200	200	1	7	11	12
			2. 2		ZUU TRA		Т	/	ΤT	
Q1A Q1B			2 2							
Q1C			2		TRA TRA					
Q1D			2		TRA					
Q1D Q2A	9	2	ے 3	200		ANB				
Q2A Q2B	9	2	3			ANC				
Q2D Q2C	9	2		200		ANC				
Q2C Q3A	10	2 8		200		ANC				
03B	10	8		200		ANC				
Q3C	10	8	3			ANC				
Q4A	3	300	4			ANC				
04B	3	300	4			ANB				
Q4D Q4C	3	300				ANB				
Q5A	2	300		200		ANA				
Q5A Q5B	2	300		200		ANA				
Q5C	2 2	300		200		ANA				
Q5D	2	300		200		ANA				
Q5D Q6A	∠ 8	300		200		ANA				
Q6A Q6B	о 8	300				ANA				
06C	8	300				ANA				
~	8	300		200						
Q6D		300 7	8			ANA				
Q7A Q7B	100 100	7		200		ANA ANA				
Q7С	100	7		200		ANA				
Q7D		7		200		RANA	~			
Q7D Q8	100			1 20		RANI				
Q9	100	9		2 20		RANI				
Q9 R1	100	9		2020	0 1.	KANI	)			
		м, О.		20						
R2	100			20						
		M, 0.		20						
R3	4		28	R						
		бМ, О								
R4	5									
		бм, 0								
R5	6 0.2									
		бм, О								
-	S LVT		• • •	0						
· BND		1102								
* IN	PUT E	SD	51	= i1	n, 6	1 οι	ıt			
.SUB	CKT I	N_ESD	1(	00 2	00 5	1 61	1			
D1	5	1	-	100		ES14	4X1	.9M		
D2	5	1	-	100		ES14	4X1	.9M		
D3	5	1	-	100		ES14	4X1	.9M		
D4	2	00	ŗ	51		ES14	4X1	.9M		
D5	2	00	ŗ	51		ES14	4X1	.9S		
D6	2	00	ŗ	51		ES14	4X1	.9M		
D7	2	00	ļ	51		ES14	4X1	.9S		
D8	2	00	ļ	51		ES14	4X1	.9M		
D9	2	00	ļ	51		ES14	4X1	.9S		
RB1	5	1 61		1000						
*	TC=	0.26M	, (	0.9U						
.END	S IN_	ESD								

OUIFUI			
.SUBCKT	OUT_ESD	100	200 81
D1	81	100	ES14X19M
D2	81	100	ES14X19M
D3	200	81	ES14X19M
D4	200	81	ES14X19S
D5	200	81	ES14X19M
D6	200	81	ES14X19S
.ENDS OU	JT_ESD		
.SUBCKT		500	91
R1 91 5	500 50		

```
.ENDS
```

\* OUTPUT ESD

.END

.MODEL TRANA NPN (IS=8.12E-18 BF=192 NF=1 VAF=75.6 IKF=1.49E-02 + ISE=9.14E-17 NE=2 BR=15.8 VAR=2.76 IKR=2.2E-03 ISC=2.62E-16 + NC=1.578 RB=327 IRB=4.8E-05 RBM=0.001 RE=10 RC=15 CJE=2.0E-14 + VJE=.8867 MJE=.2868 TF=9.02E-12 ITF=7.6E-03 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS + CJC=5.6E-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=4.8E-15 VJS=.4193 MJS=.2563 + EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9) .MODEL TRANC NPN (IS=1.36E-17 BF=180 NF=1 VAF=87.6 IKF=2.19E-02 + ISE=6.65E-16 NE=2 BR=16.9 VAR=2.76 IKR=1.5E-03 ISC=1.11E-16 + NC=1.578 RB=136 IRB=3.24E-05 RBM=0.001 RE=6 RC=8 CJE=1.02E-13 + VJE=.8867 MJE=.2868 TF=9.02E-12 ITF=1.27E-02 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS + CJC=10.3E-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=9.94E-15 VJS=.4193 MJS=.2563 + EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9) .MODEL TRAND NPN (IS=6.55E-17 BF=103 NF=1 VAF=90 IKF=2.91E-01 + ISE=8.85E-15 NE=2 BR=15.7 NR=1 VAR=3.82 IKR=2.01E-02 ISC=1.48E-15 + NC=2 RB=10.5 IRB=4.39E-04 RBM=0.29 RE=0.351 RC=9 CJE=3.5E-13 + VJE=.8167 MJE=.1973 TF=8.99E-12 ITF=1.3E-01 XTF=5.67 VTF=1.86 PTF=41.43 TR=6.405E-10 + CJC=1.4E-13 VJC=.6401 MJC=.2674 XCJC=1 CJS=9.3E-14 VJS=.5002 MJS=.1706 + EG=1.135 XTI=4.177 XTB=0.6322 FC=0.961) .MODEL TRANB NPN (IS=2.71E-17 BF=172 NF=1 VAF=71.4 IKF=4.38E-02 + ISE=1.33E-15 NE=2 BR=17.9 VAR=2.76 IKR=3.0E-03 ISC=2.22E-16 + NC=1.578 RB=67 IRB=6.47E-05 RBM=0.001 RE=3 RC=4 CJE=5.09E-14 + VJE=.8867 MJE=.2868 TF=9.02E-12 ITF=2.53E-02 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS + CJC=20.6E-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=1.7E-14 VJS=.4193 MJS=.2563 + EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9) .MODEL TRANEPNP (IS=1.65e-17 BF=210 NF=1 VAF=7.5 IKF=6.51e-05 + ISE=7.75e-17 NE=1.813 BR=210 VAR=5.68 IKR=6.51e-05 ISC=7.75e-17 + NC=1.813 RB=349 IRB=1.77e-07 RBM=53 RE=119 RC=158 CJE=7.04e-15 + VJE=0.6578 MJE=0.149 TF=6.33e-10 ITF=2.2e-08 XTF=2.8 VTF=1.4 + PTF=41.56 TR=1e-9 CJC=7.04e-15 VJC=0.8034 MJC=0.1773 XCJC=.3 + CJS=4.79e-15 VJS=.4193 MJS=0.0902 + EG=1.158 XTI=2.015 XTB=0.1208 FC=0.9) .MODEL TLS LPNP (IS=1.65e-17 BF=210 NF=1 VAF=7.5 IKF=6.51e-05 + ISE=7.75e-17 NE=1.813 BR=210.1 NR=1 VAR=5.68 IKR=2.61e-04 ISC=7.75e-17 + NC=1.813 RB=349 IRB=1.8e-07 RBM=53 RE=119 RC=158 CJE=7.0e-15

+ VJE=.6578 MJE=.149 TF=6.33e-10 ITF=2.2e-08 XTF=.5356 VTF=.2365 PTF=0 TR=6.33e-10

+ CJC=7.0e-15 VJC=.8034 MJC=.1773 XCJC=1 CJS=4.8e-15 VJS=.5 MJS=.09022

+ EG=1.158 XTI=2.015 XTB=0.1208 FC=0.9)

```
.MODEL ES14X19M D (IS=1.55E-14 CJO=160FF RS=12 VJ=.58 M=.25 BV=9)
.MODEL ES14X19S D (IS=1.55E-14 CJO=29FF VJ=.624 M=.571)
.END
* PACKAGE: 8SOIC
* SPICE SUBCIRCUIT FILE OF COUPLED TRANSMISSION LINES
* CREATED FRI APR 25 16:47:54 1997
* BY PMG VERSION 3.6.2
* TRANSMISSION LINE MODEL
*
   CONDUCTOR PIN
*
      1
                 1
*
       2
                  2
*
       3
                 3
*
       4
                 4
*
       5
                 5
*
       6
                 6
*
       7
                 7
*
       8
                  8
* NUMBER OF LUMPS:
                     1
* FASTEST APPLICABLE EDGE RATE:
                             0.076 NS
* CONNECT CHIP SIDE TO N**I AND BOARD SIDE TO N**O
.SUBCKT LINES NO1I NO1O NO2I NO2O NO3I NO3O NO4I NO4O
+ N051 N050 N061 N060 N071 N070 N081 N080
LO1WB NO1I NO1M
                   1.367E-09
     N01M N010
L01
                     7.794E-10
      N01M 0
C01
                    2.445E-13
LO2WB NO2I NO2M
                   1.287E-09
L02
      N02M N02O
                   5.473E-10
      N02M 0
C02
                    1.888E-13
LO3WB NO3I NO3M
                   1.287E-09
      N03M N030
T.03
                   5.473E-10
      N03M 0
C03
                     1.901E-13
L04WB N04I
            N04M
                     1.367E-09
            N040
L04
      N04M
                     7.723E-10
C04
      N04M
              0
                     2.443E-13
      N051 N05M
N05M N050
L05WB N05I
                     1.367E-09
L05
                     7.710E-10
C05
      N05M 0
                     2.478E-13
LOGWB NOGI NOGM
                   1.287E-09
L06
      N06M N06O
                   5.489E-10
C06
      N06M 0
                    1.916E-13
LO7WB NO7I NO7M
                   1.287E-09
L07
      N07M N07O
                   5.495E-10
C07
      N07M 0
                    1.930E-13
LO8WB NO8I NO8M
                   1.367E-09
L08
      N08M N08O
                     7.786E-10
      N08M
                    2.451E-13
C08
            0
K0102 L01
             L02
                    0.1687
K0102WB L01WB L02WB 0.3400
C0102 N010
              N020
                     3.674E-14
K0103 L01
              L03
                     0.0702
K0103WB L01WB
              L03WB
                     0.1847
K0203 L02
              L03
                     0.1822
K0203WB L02WB
             L03WB
                     0.3505
C0203 N020 N030 3.521E-14
     L02
                     0.0682
к0204
              L04
K0204WB L02WB L04WB 0.1847
```

К0304	L03	L04	0.1694
K0304WB	L03WB	L04WB	0.3400
C0304	N030	N040	3.675E-14
K0305WB	L03WB	L05WB	0.1847
K0405WB	L04WB	L05WB	0.3455
K0406WB	L04WB	L06WB	0.1847
K0506	L05	L06	0.1697
K0506WB	L05WB	LOGWB	0.3400
C0506	N050	N060	3.720E-14
K0507	L05	L07	0.0682
K0507WB	L05WB	L07WB	0.1847
K0607	L06	L07	0.1824
K0607WB	L06WB	L07WB	0.3505
C0607	N060	N070	3.570E-14
K0608	L06	L08	0.0702
K0608WB	L06WB	L08WB	0.1847
K0708	L07	L08	0.1691
K0708WB	L07WB	L08WB	0.3400
C0708	N070	N080	3.632E-14
.ENDS L]	INES		

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