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AND8157/D

ECLinPS MAX™ (SiGe) SPICE Modeling Kit

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APPLICATION NOTE

Objective

The objective of this kit is to provide sufficient circuit schematic and SPICE parameter information to perform system level interconnect modeling for devices in ON Semiconductor's high performance ECLinPS MAX (SiGe) logic family. The family has output edge rates as low as 50 ps and power supply levels of as low as 2.5 V.

The kit is not intended to provide information necessary to perform circuit level or device behavioral LOGIC modeling on the ECLinPS MAX devices.

Schematic Information

The kit contains representative input and output schematics, netlists and waveforms for SPICE modeling and simulating the ECLinPS MAX family devices INPUT and OUTPUT structures. This application note will be modified as new devices are added. Table 1 describes the nomenclature used for modeling the schematic and netlist for ECLinPS MAX devices.

Table 1. Schematics and Netlist Nomenclature

Parameter	Function Description
V_{CC}	2.5 / 3.3 V for LVPECL and 0 V for LVNECL
V_{EE}	−2.5 / −3.3 V for LVNECL and 0 V for LVPECL
V_{CS}	Internally Generated Voltage (V_{EE} + 0.915 V ± 50 mV)
IN	True (+) Input to BUFFER
$\overline{IN}$	Inverted (−) Input to BUFFER
Q	True (+) Output of BUFFER
$\overline{Q}$	Inverted (−) Output of BUFFER
INT	Internal True (+) Input to Output Buffer
$\overline{INT}$	Internal Invert (−) Input to Output Buffer

The subcircuit models, such as input or output buffers, ESD and package simulate only device input or output paths. When used with interconnect models, a complete signal path may be modeled as shown in Figure 1.

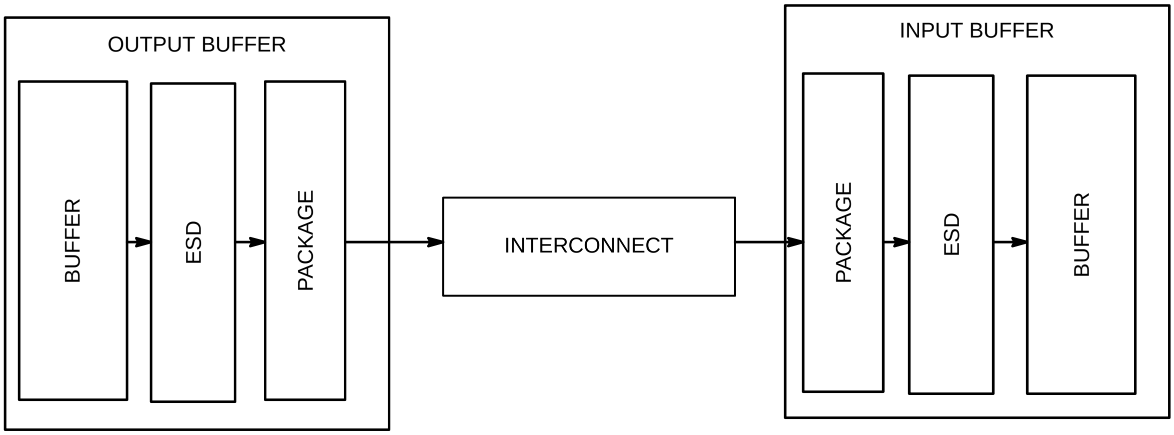

Figure 1. Interconnect Model Template

For device modeling, the behavioral LOGIC or gate functionality is not modeled (see Figure 2. DEVICE Model Template)

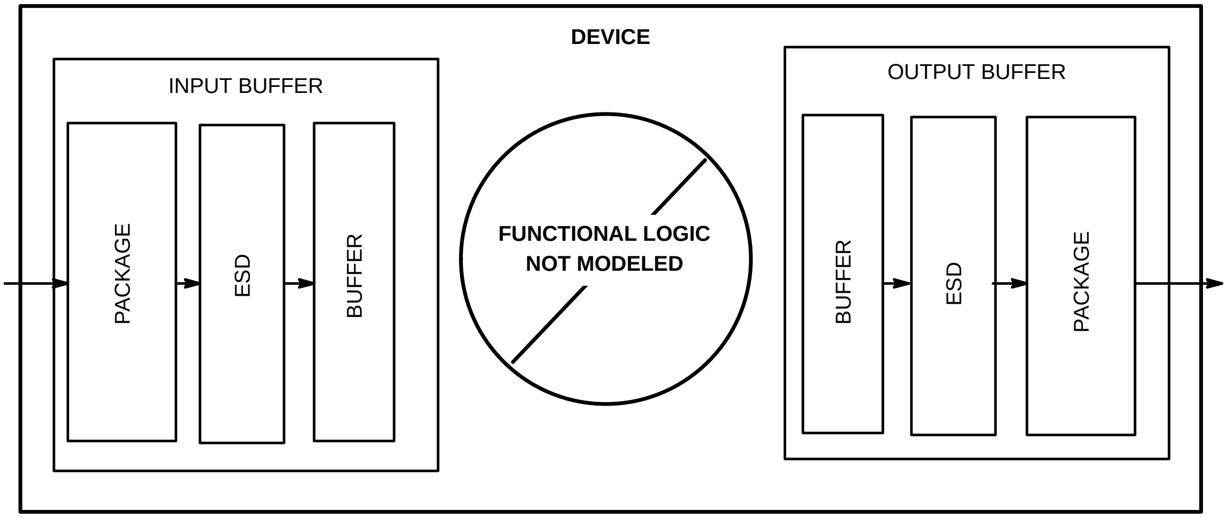

Figure 2. DEVICE Model Template

Package

Models for various package types have been included to improve the accuracy of the system interconnect model (Table 2).

Table 2. Available Package Models

Package	Model
SOIC−8	Appendix B (Figure 11 and Table 4)
TSSOP−8	Appendix B (Figure 12 and Table 5)
QFN−16	Figure 9

The package model represents the parasitics as they are measured at a significant distance from an AC ground pin. The package models should be placed on all external inputs of an input model, all external outputs of an output model and the V_{CC} line. Since the current in the V_{EE} pin is a constant, a package model for V_{EE} pin is not necessary. Note an internal V_{CS} voltage does not require a package model. To speed up the simulation process, simplified package models have been used.

Input Buffer

The input buffer schematics and netlists present the various input structures for ECLinPS MAX family devices. The schematics and netlists include ESD and package model parasitics for accuracy.

Output Buffer

Output buffer schematics and netlists models are provided. The package model parasitics has been added for accuracy. The output buffer models typically show internal differential inputs driven by INT and $\overline{\text{INT}}$. Outputs should always be simulated with both output lines properly terminated, even when only one line or single ended use is intended. This will balance the output buffer’s load.

For correlation, a typical output waveform seen at the input of the receiver, is shown in Figure 10.

SPICE Netlist

The netlists are organized as a subcircuit. In each subcircuit model netlist, the model name should be followed by a list of external node interconnects. When copying a “SUBCKT” netlist files to your text editor, use Adobe® Acrobat® Reader 4.0 or higher to ensure proper character conversion.

SPICE Parameter Information

In addition to the schematics and netlists there is a listing of the SPICE parameters for the transistors and diodes referenced in the schematics and netlists found provided in APPENDIX A. These parameters represent a typical case device of the transistor or diode. Varying the typical parameters will affect the DC and AC performance of the structures and is not recommended. Modeling of device actual delay time is not the intention of this document.

The performance levels may be varied by methods and discussed in the next section. The resistors referenced in the schematics are polysilicon and have negligible parasitic capacitance in the real circuit. The schematics display only devices needed in the SPICE netlists.

Modeling Information

The bias drivers for the devices are not included as they are unnecessary for interconnect simulations and their use results in a large increase in model complexity and simulation time. The internal reference voltages (V_{BB}, V_{CS}, etc.) should be modeled with ideal constant voltage sources. Output and input levels of ECLinPS MAX devices generally vary in a one to one ratio with the power supply; and remain relatively constant over temperature. Note the V_{CS} supply is always relative to V_{EE}, the most negative supply. The output schematics and SPICE parameters include a typical waveform, for simulation correlation. Inclusion of ESD and package models typically will add about 5.0 ps − 7.0 ps to the output waveform rise and fall time. Simple adjustments made to the models may permit output characteristics to emulate conditions at or near the performance corners of the data sheet specifications. Consistent, repeatable cross–point voltages of 50% should be maintained.

To Adjust Rise and Fall Times, t_r and t_f

Produce the desired variant rise and fall times output slew rates by adjusting collector load resistors. This V_{CS} voltage determines the tail current in the output differential affecting the t_r and t_f of the output.

To Adjust the V_{OH}

Adjust the V_{OH} and V_{OL} level together by varying V_{CC}. The output levels will follow changes in V_{CC} at a 1:1 ratio.

To Adjust the V_{OL}

Adjust the V_{OL} level independently of the V_{OH} level by adjusting increasing the collector load resistance. Note the V_{OH} level will also by affected due to an I_{BASE} * R drop across the collector load resistor. The V_{OL} can be changed by varying the V_{CS} supply which will also affect gate current through the current source resistor.

Device Specifics

6L239

An exception to the general rule of "levels are relative to V_{CC}" is found in the internal input node of **$\overline{\text{EN}}$, SELx**, and **$\overline{\text{MR}}$ INPUT BUFFERS** at the voltage divider BIAS feeding one side of the differential. This remains at $V_{CC}/2$ forcing the detect threshold to ratiometrically change with V_{CC}.

When left floating open, the $\overline{\text{EN}}$ and SELx inputs will be forced to a default state of LOW by the internal 75 kΩ pulldown resistor to V_{EE}, relative to the $V_{CC}/2$ BIAS voltage on the other side of the differential. The $\overline{\text{MR}}$ input, when left floating open, will be forced to a default state of HIGH by the internal 75 kΩ pullup resistor to V_{CC}.

6L11 and 6L16

Inputs, when left floating open, will not be forced to a determined default state. Precautionary considerations may be needed to prevent spontaneous self oscillation of the device.

Summary

The information included in this kit provides adequate information to run a SPICE level system interconnect simulation. The block diagram in Figure 2 illustrates a typical situation, which can be modeled using the information in this kit.

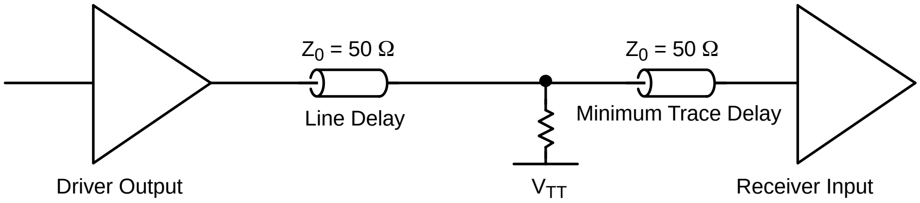

Figure 3. Typical Application for I/O SPICE Modeling Kit

Device input or output models are presented in Table 3.

Table 3. ECLinPS MAX Input/Output Buffer Selector Guide

Device	Function	Pin	Description	Model
NB6L11	2.5 V / 3.3 V Multilevel Input to Differential LVNECL/LVPECL 1:2 Clock or Data Fan-out Buffer/Translator	6, 7	INPUT	INBUF_01
		1, 2, 3,4	OUTPUT	OBUF_01
NB6L16	2.5 V / 3.3 V Multilevel Input to Differential LVNECL/LVPECL Clock or Data Receiver/Buffer/Translator	2, 3	INPUT	INBUF_01
		6, 7	OUTPUT	OBUF_01
NB6L239	2.5 V / 3.3 V Any Differential Clock IN to Differential LVPECL OUT DIV by 1/2/4/8/16 Clock Divider	5, 6, 7, 14, 15	$\overline{\text{EN}}$ and SELx INPUT	$\overline{\text{EN}}$_SEL
		16	$\overline{\text{MR}}$ INPUT	$\overline{\text{MR}}$
		1, 2, 3	CLKs and VDT INPUT	CLK_IN
		9, 10, 11, 12	OUTPUT	OBUF_01
NB6N239S	3.3 V, 3.0 GHz Any Differential Clock IN to LVDS OUT DIV by 1/2/4/8, DIV by 2/4/8/16 Clock Divider	5, 6, 7, 14, 15	Single Ended Inputs	INBUF_01
		16	$\overline{\text{MR}}$ INPUT	$\overline{\text{MR}}$
		2, 3	CLKs and VDT INPUT	INBUF_01
		9, 10, 11, 12	LVDS OUTPUT	OBUF_02

INBUF_01 INPUT BUFFER

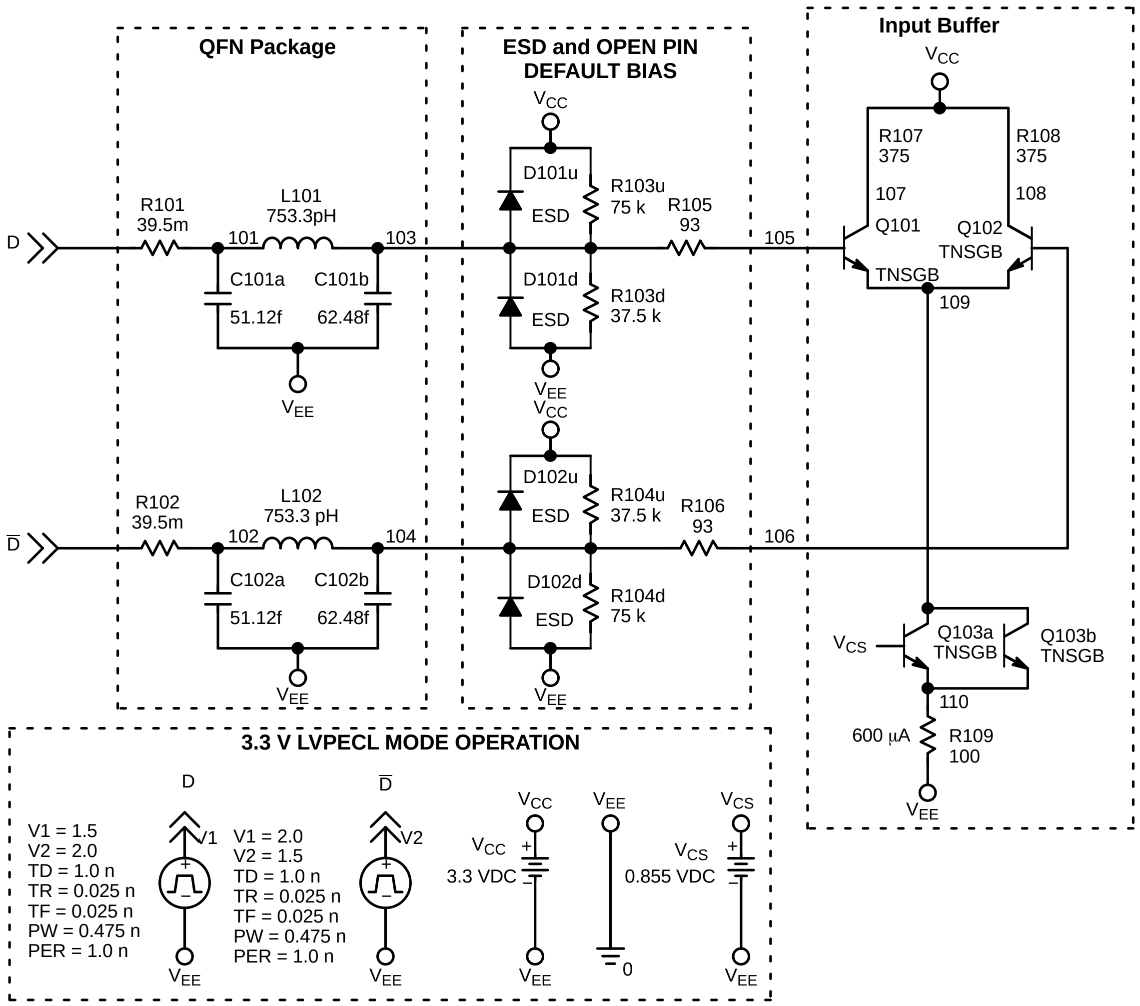

Figure 4. INBUF_01 Input Buffer

```
V_V1     D 0
V_V2     DB 0
V_VCC     VCC 0 3.3Vdc
V_VCS     VCS 0 .855Vdc
+PULSE 1.5 2.0 1n 0.025n 0.025n 0.475n 1n
+PULSE 2.0 1.5 1n 0.025n 0.025n 0.475n 1n
.SUBCKT INBUF_01
C_C101a     0 101 51.12f
C_C101b     0 103 62.48f
C_C102a     0 102 51.12f
C_C102b     0 104 62.48f
D_D101d     0 103 ESD
D_D101u     103 VCC ESD
D_D102d     0 104 ESD
D_D102u     104 VCC ESD
L_L101     101 103 753.3pH
L_L102     102 104 753.3pH
Q_Q101     107 105 109 TNSGB
Q_Q102     108 106 109 TNSGB
Q_Q103a     109 VCS 110 TNSGB
Q_Q103b     109 VCS 110 TNSGB
R_R101     101 D 39.5m
R_R102     102 DB 39.5m
```

```
R_R103d     103 0 37.5K
R_R103u     VCC 103 75K
R_R104d     104 0 75K
R_R104u     VCC 104 37.5K
R_R105     103 105 93
R_R106     104 106 93
R_R107     107 VCC 375
R_R108     108 VCC 375
R_R109     0 110 100
.END INBUF_01
```

$\overline{\text{EN}}$ AND SELx INPUT BUFFER

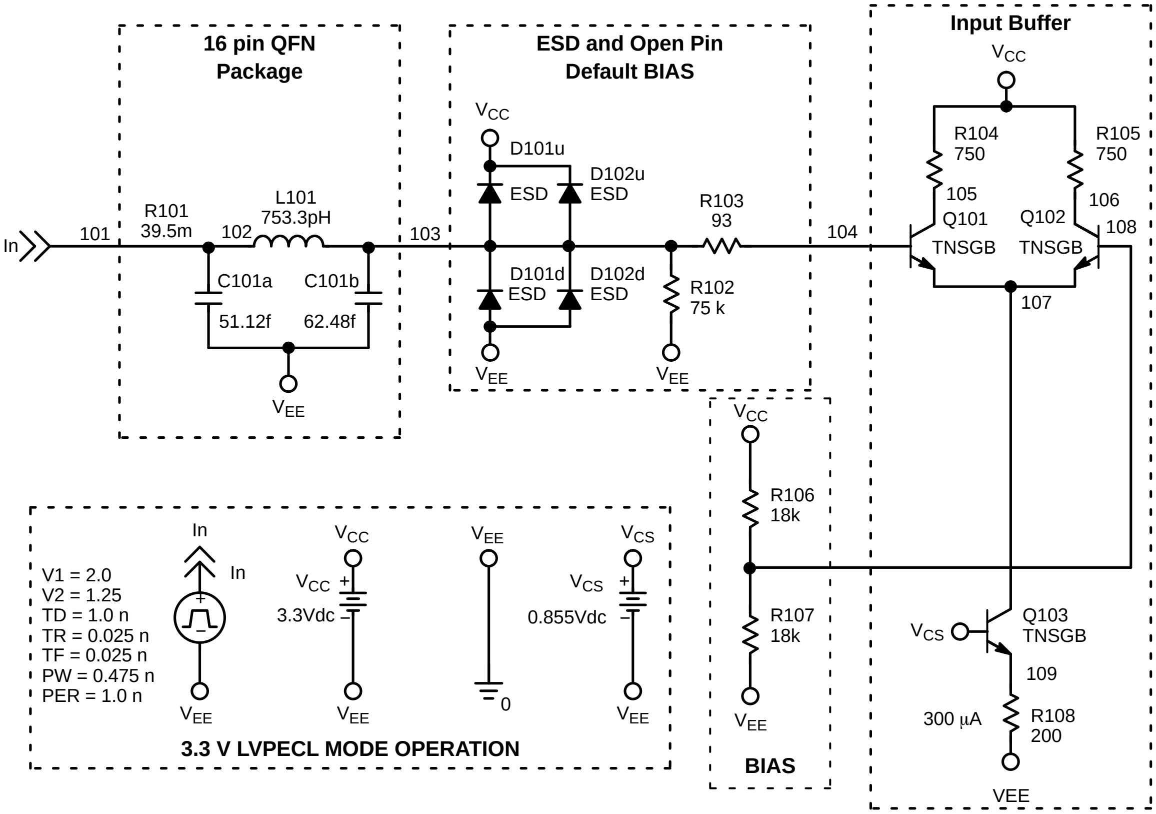

Figure 5. $\overline{\text{EN}}$ and SELx Input Buffer

```
V_In     IN 0
V_VCC     VCC 0 3.3Vdc
V_VCS     VCS 0 0.855Vdc
+PULSE 2.0 1.25 1n 0.025n 0.025n 0.475n 1n
.SUBCKT ENb_SEL
C_C101a     0 102 51.12f
C_C101b     0 103 62.48f
D_D101d     0 103 ESD
D_D101u     103 VCC ESD
D_D102d     0 103 ESD
D_D102u     103 VCC ESD
L_L101     102 103 753.3pH
Q_Q101     105 104 107 TNSGB
Q_Q102     106 108 107 TNSGB
Q_Q103     107 VCS 109 TNSGB
R_R101     102 IN 39.5m
R_R102     103 0 75K
R_R103     103 104 93
R_R104     105 VCC 750
R_R105     106 VCC 750
R_R106     VCC 108 18K
R_R107     108 0 18K
R_R108     0 108 200
.END ENb_SEL
```

$\overline{\text{MR}}$ INPUT BUFFER

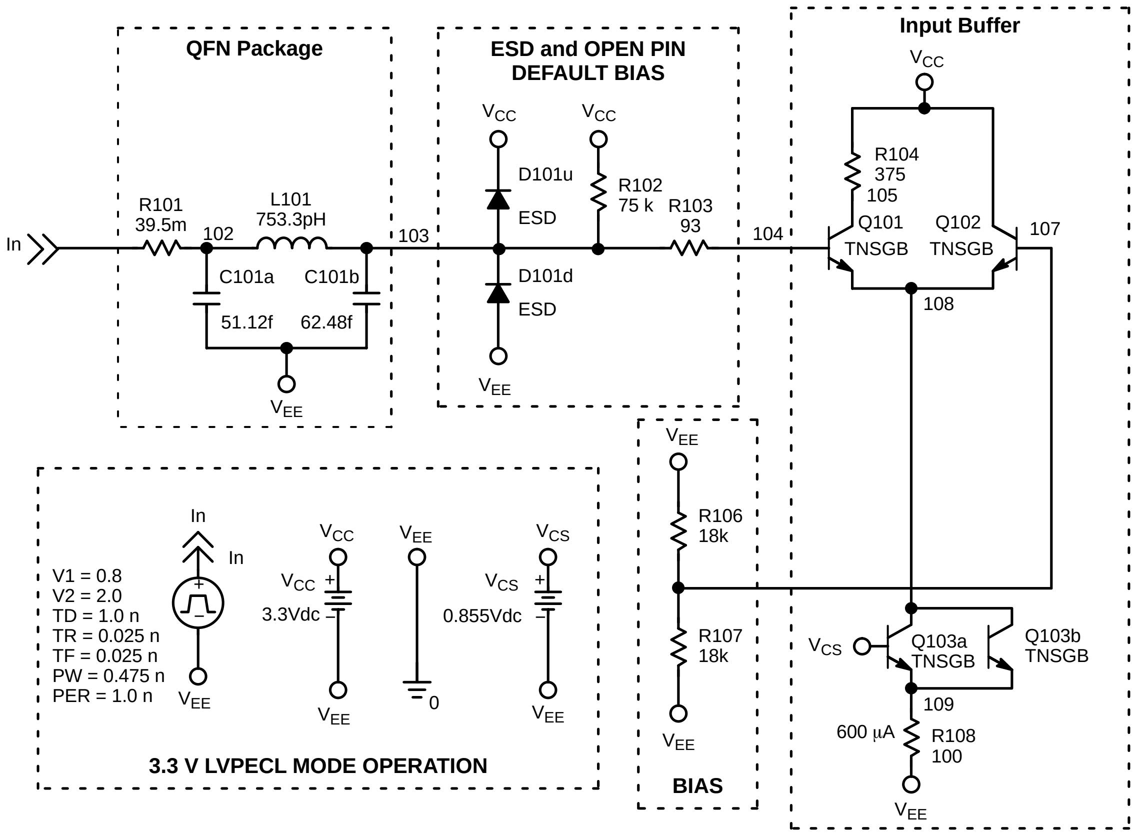

Figure 6. $\overline{\text{MR}}$ Input Buffer

```
+PULSE 0.8 2.0 1n 0.025n 0.025n 0.475n 1n
V_V1     IN 0
V_VCC     VCC 0 3.3Vdc
V_VCS     VCS 0 .855Vdc
.SUBCKT MRb
C_C101a     0 102 51.12f
C_C101b     0 103 62.48f
D_D101d     0 103 ESD
D_D101u     103 VCC ESD
L_L101     102 103 753.3pH
Q_Q101     105 104 108 TNSGB
Q_Q102     VCC 107 108 TNSGB
Q_Q103a     108 VCS 109 TNSGB
Q_Q103b     108 VCS 109 TNSGB
R_R101     102 IN 39.5m
R_R102     VCC 103 75K
R_R103     103 104 93
R_R104     105 VCC 375
R_R106     VCC 107 18K
R_R107     107 0 18K
R_R108     0 109 100
.END .MRb
```

CLKS AND VTD INPUT BUFFER

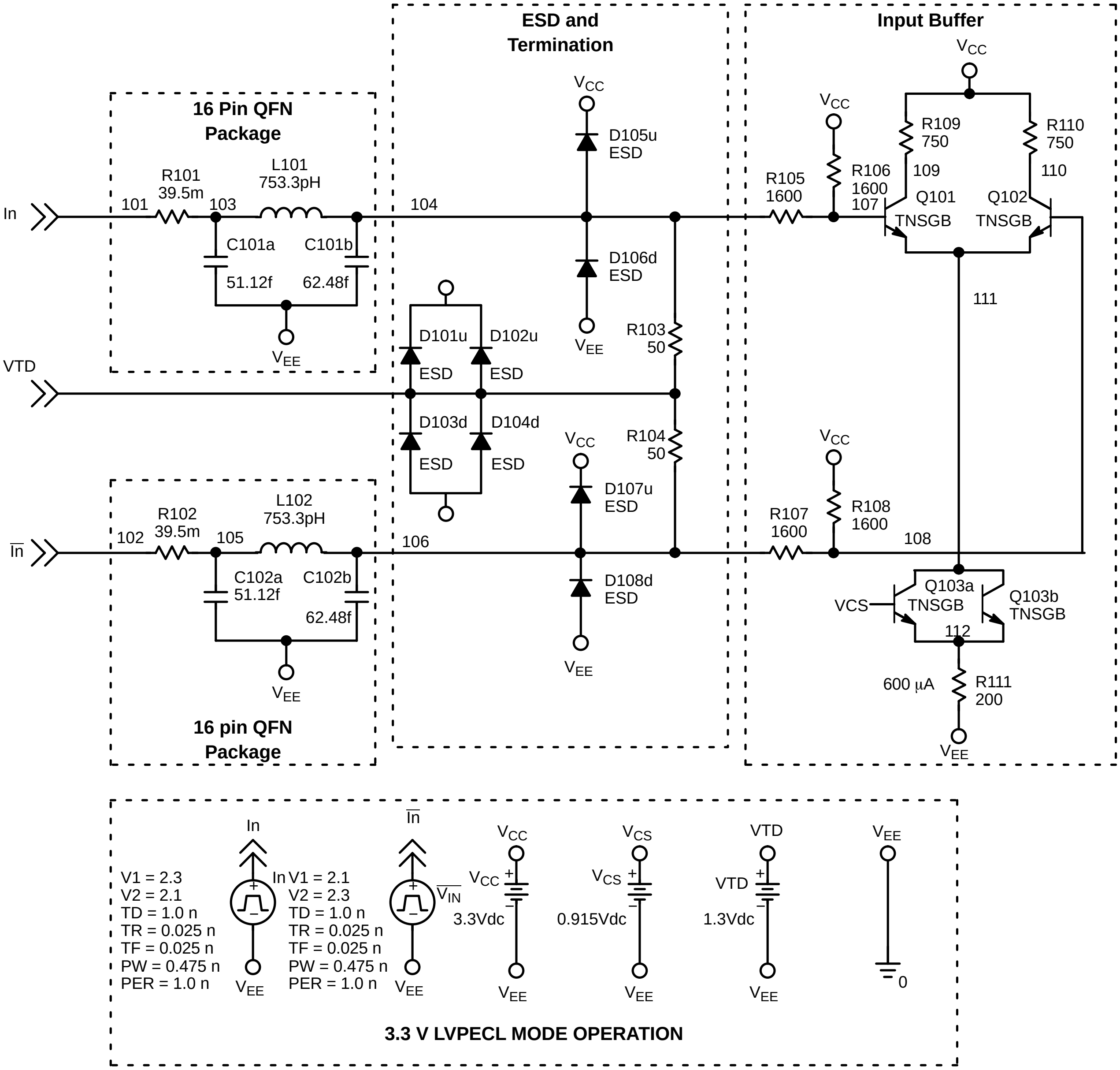

Figure 7. CLKs and VTD Input Buffer

```
+PULSE 2.1 2.3 1n 0.025n 0.025n 0.475n 1n
+PULSE 2.3 2.1 1n 0.025n 0.025n 0.475n 1n
V_TD     TD 0 1.3Vdc
V_VCC     VCC 0 3.3Vdc
V_VCS     VCS 0 0.915Vdc
V_VIN     IN 0
V_VINb     INB 0
.SUBCKT CLK_IN
C_C101a     0 103 51.12f
C_C101b     0 104 62.48f
C_C102a     0 105 51.12f
C_C102b     0 106 62.48f
D_D101u     TD VCC ESD
D_D102u     TD VCC ESD
D_D103d     0 TD ESD
```

```
D_D104d     0 TD ESD
D_D105u     104 VCC ESD
D_D106d     0 104 ESD
D_D107u     106 VCC ESD
D_D108d     0 106 ESD
L_L101     103 104 753.3pH
L_L102     105 106 753.3pH
Q_Q101     109 107 111 TNSGB
Q_Q102     110 108 111 TNSGB
Q_Q103a     111 VCS 112 TNSGB
Q_Q103b     111 VCS 112 TNSGB
R_R101     103 IN 39.5m
R_R102     105 INB 39.5m
R_R103     104 TD 50
R_R104     TD 106 50
R_R105     104 107 1600
R_R106     VCC 107 1600
R_R107     106 108 1600
R_R108     VCC 108 1600
R_R109     109 VCC 750
R_R110     110 VCC 750
R_R111     0 112 200
.END CLK_IN
```

INBUF_01 INPUT BUFFER

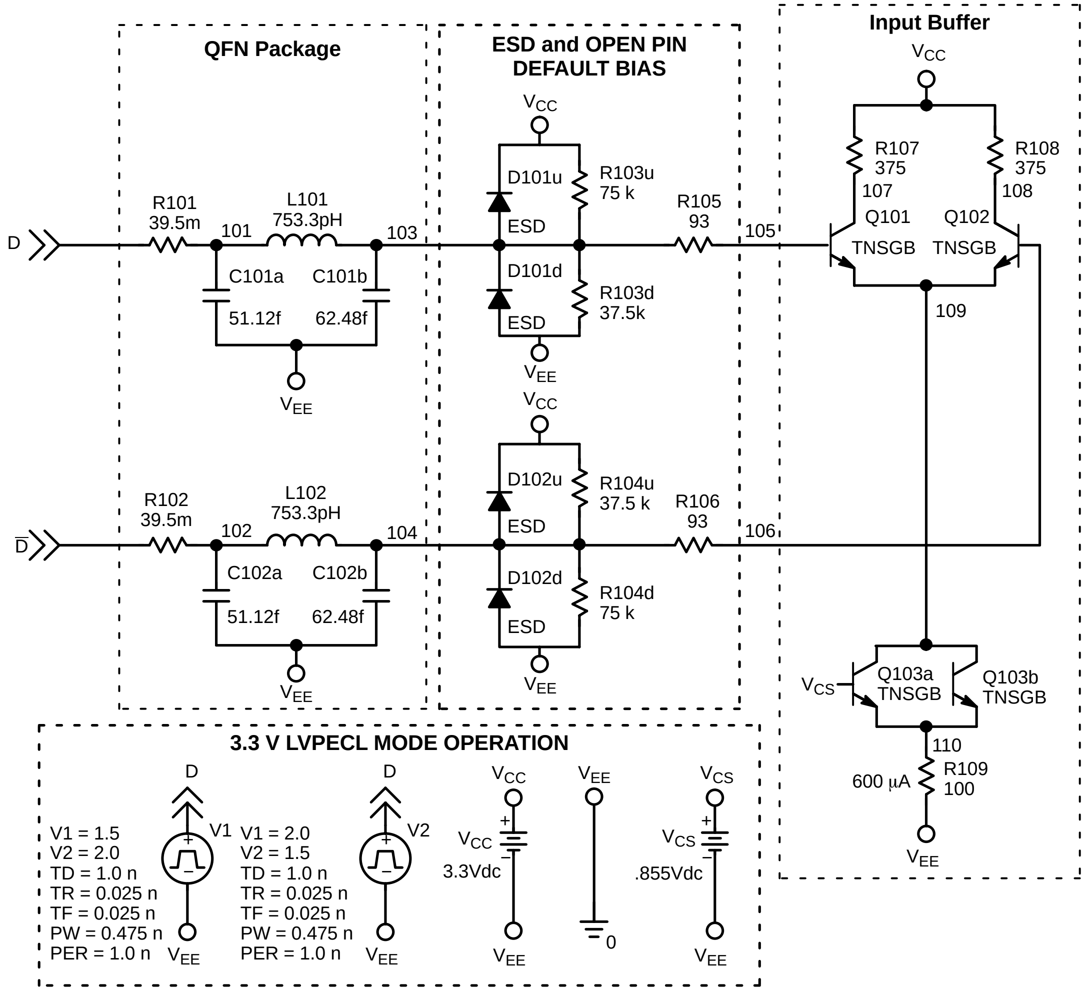

Figure 8. INBUF01 Input Buffer

```
V_V1     D 0
V_V2     DB 0
V_VCC     VCC 0 3.3Vdc
V_VCS     VCS 0 .855Vdc
+PULSE 1.5 2.0 1n 0.025n 0.025n 0.475n 1n
+PULSE 2.0 1.5 1n 0.025n 0.025n 0.475n 1n
.SUBCKT INBUF_01
C_C101a     0 101 51.12f
C_C101b     0 103 62.48f
C_C102a     0 102 51.12f
C_C102b     0 104 62.48f
D_D101d     0 103 ESD
D_D101u     103 VCC ESD
D_D102d     0 104 ESD
D_D102u     104 VCC ESD
L_L101     101 103 753.3pH
L_L102     102 104 753.3pH
Q_Q101     107 105 109 TNSGB
Q_Q102     108 106 109 TNSGB
Q_Q103a     109 VCS 110 TNSGB
Q_Q103b     109 VCS 110 TNSGB
R_R101     101 D 39.5m
R_R102     102 DB 39.5m
```

```
R_R103d     103 0 37.5K
R_R103u     VCC 103 75K
R_R104d     104 0 75K
R_R104u     VCC 104 37.5K
R_R105     103 105 93
R_R106     104 106 93
R_R107     107 VCC 375
R_R108     108 VCC 375
R_R109     0 110 100
.END INBUF_01
```

OBUF_01 OUTPUT BUFFER DRIVING 6L239 CLKS AND VTD INPUT BUFFER

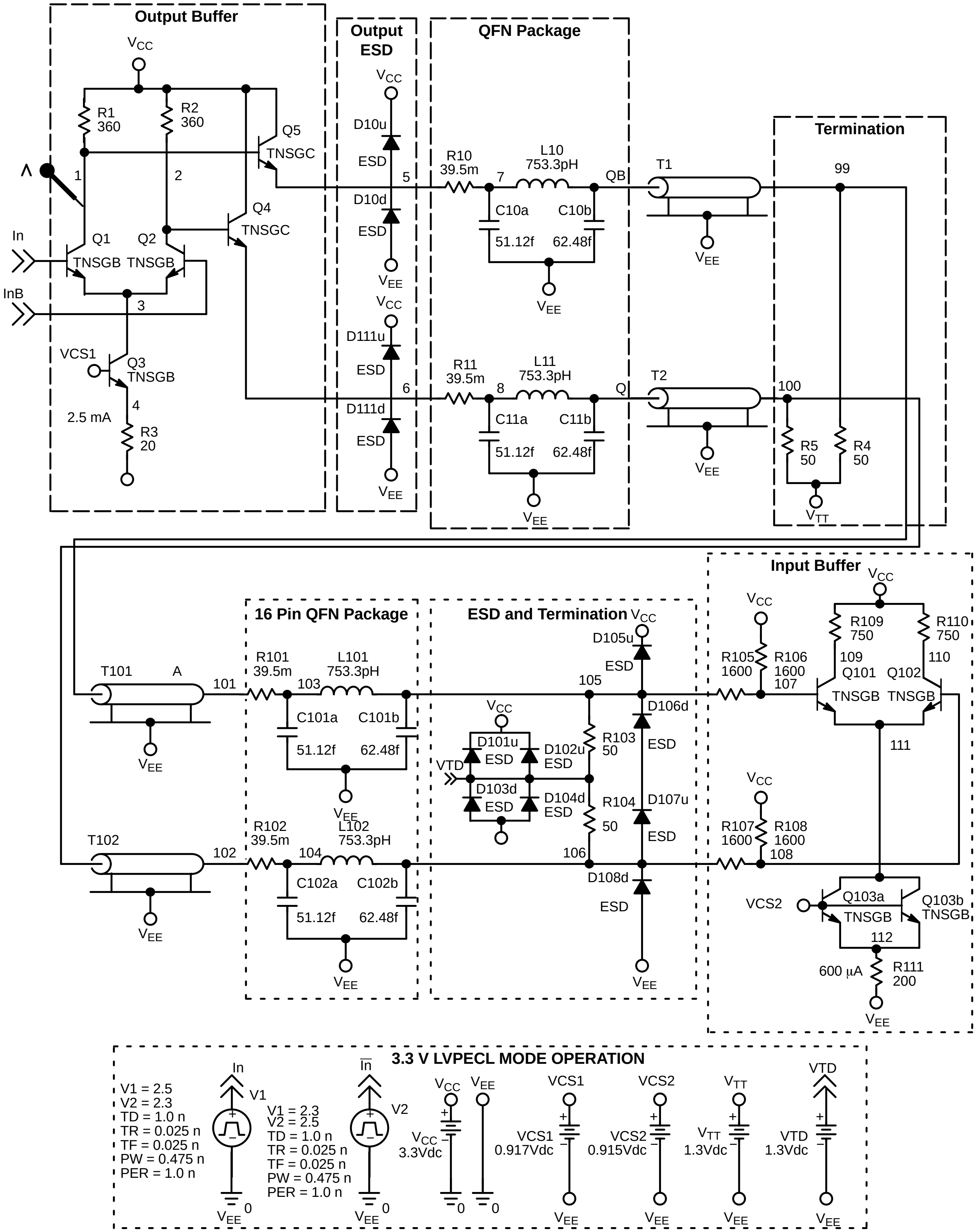

Figure 9. OBUF_01 Output Buffer driving 6L239 CLKs and VTD Input Buffer

```
V_V1     IN 0
V_V2     INB 0
V_VCC     VCC 0 3.3Vdc
V_VCS1     VCS1 0 0.917Vdc
V_VCS2     VCS2 0 0.915Vdc
V_VTD     VTD 0 1.3Vdc
V_VTT     VTT 0 1.3Vdc
+PULSE 2.3 2.5 1n 0.025n 0.025n 0.475n 1n
+PULSE 2.5 2.3 1n 0.025n 0.025n 0.475n 1n
.SUBCKT OBUF_01
C_C10a     0 7 51.12f
C_C10b     0 QB 62.48f
C_C11a     0 8 51.12f
C_C11b     0 Q 62.48f
D_D10d     0 5 ESD
D_D10u     5 VCC ESD
L_L10     7 QB 753.3pH
L_L11     8 Q 753.3pH
Q_Q1     1 IN 3 TNSGB
Q_Q2     2 INB 3 TNSGB
Q_Q3     3 VCS1 4 TNSGB
Q_Q4     VCC 2 6 TNSGC
Q_Q5     VCC 1 5 TNSGC
R_R1     1 VCC 360
R_R10     5 7 39.5m
R_R11     6 8 39.5m
R_R2     2 VCC 360
R_R3     0 4 20
R_R4     99 VTT 50
R_R5     100 VTT 50
T_T1     QB 0 99 0 Z0=50 TD=80ps
T_T2     Q 0 100 0 Z0=50 TD=80ps
.END OBUF_01
.SUBCKT CLK_INBUF
C_C101a     0 103 51.12f
C_C101b     0 105 62.48f
C_C102a     0 104 51.12f
C_C102b     0 106 62.48f
D_D101u     VTD VCC ESD
D_D102u     VTD VCC ESD
D_D103d     0 VTD ESD
D_D104d     0 VTD ESD
D_D105u     105 VCC ESD
D_D106d     0 105 ESD
D_D107u     106 VCC ESD
D_D108d     0 106 ESD
D_D111d     0 6 ESD
D_D111u     6 VCC ESD
L_L101     103 105 753.3pH
L_L102     104 106 753.3pH
Q_Q101     109 107 111 TNSGB
Q_Q102     110 108 111 TNSGB
Q_Q103a     111 VCS2 112 TNSGB
Q_Q103b     111 VCS2 112 TNSGB
R_R101     103 101 39.5m
R_R102     104 102 39.5m
R_R103     105 VTD 50
R_R104     VTD 106 50
R_R105     105 107 1600
R_R106     VCC 107 1600
R_R107     106 108 1600
```

```
R_R108     VCC 108 1600
R_R109     109 VCC 750
R_R110     110 VCC 750
R_R111     0 112 200
T_T101     99 0 101 0 Z0=50 TD=80ps
T_T102     100 0 102 0 Z0=50 TD=80ps
.END CLK_INBUF
```

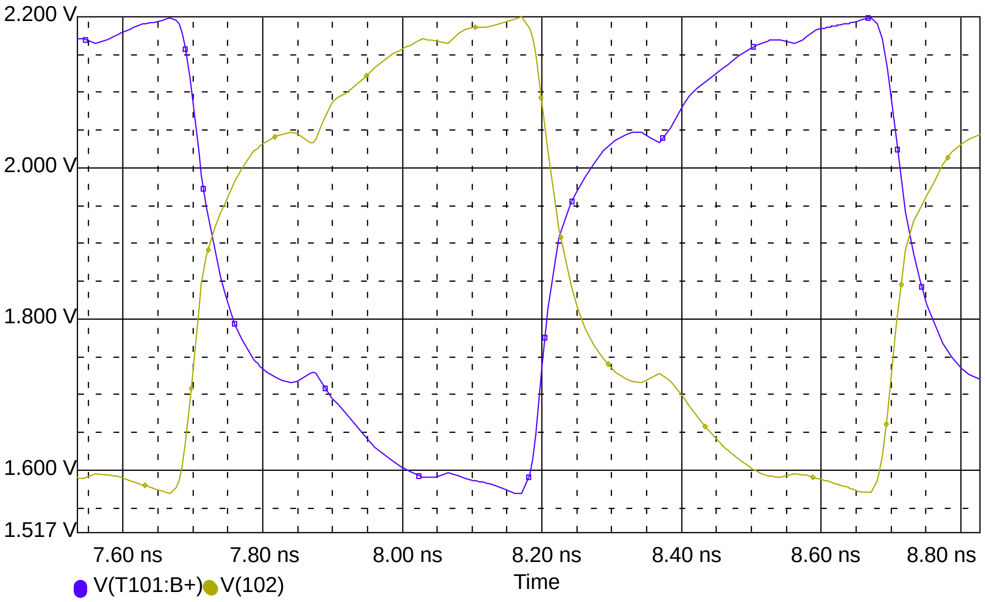

Figure 10. Typical OBUF_01 OUTPUT Waveform driving 6L239 CLK/$\overline{\text{CLK}}$ INPUT BUFFER

OBUF_02 OUTPUT BUFFER DRIVING STANDARD LVDS TERMINATION

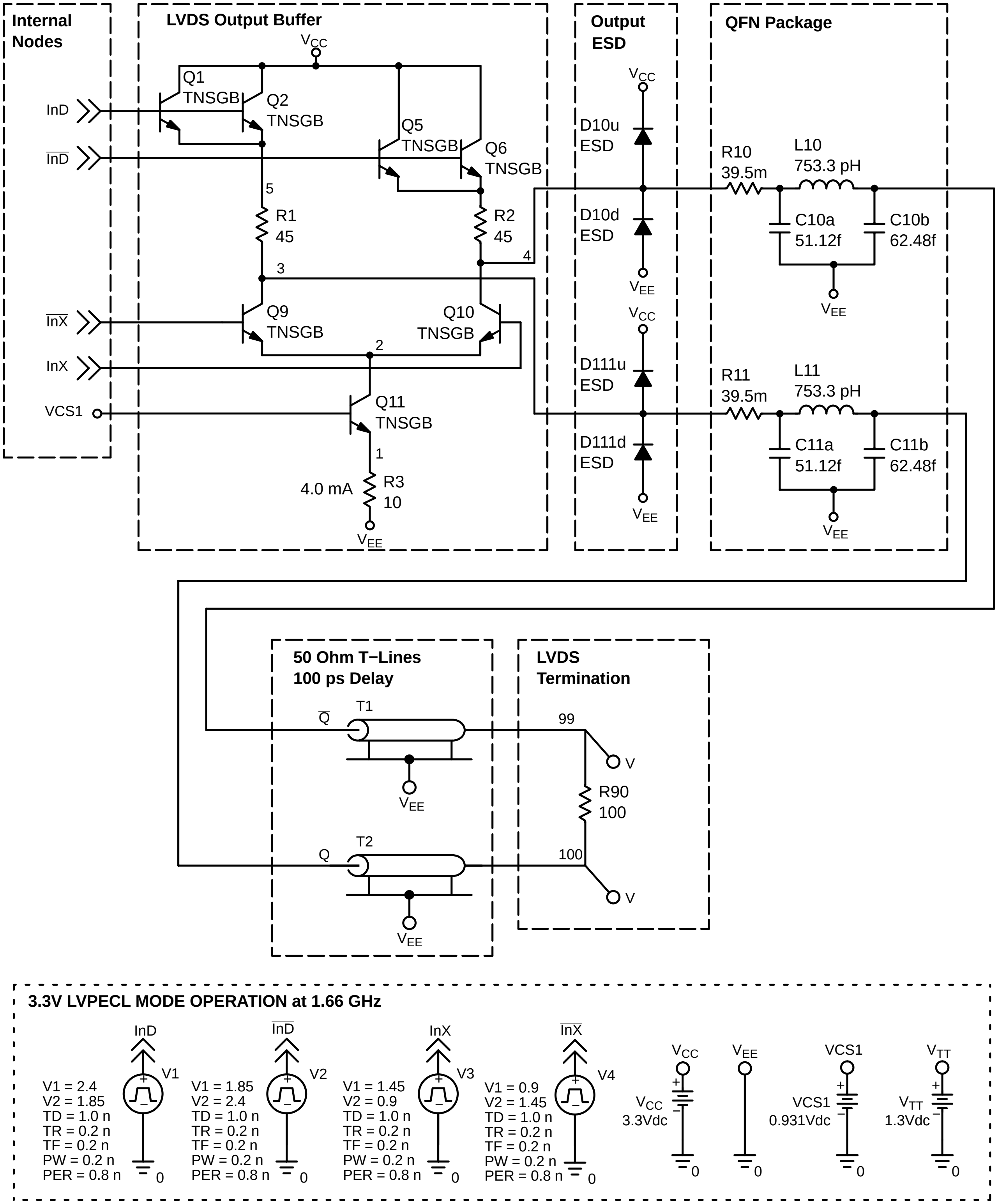

Figure 11. OBUF_02 Output Buffer driving standard LVDS termination

```
V_V1         IND 0
V_V2         INDB 0
V_V3         INX 0
V_V4         INXB 0
V_VCC         VCC 0 3.3Vdc
V_VCS1         VCS1 0 .931Vdc
V_VTT         VTT 0 1.3Vdc
+PULSE 0.9 1.45 1n 0.2n 0.2n 0.2n .8n
+PULSE 1.45 0.9 1n 0.2n 0.2n 0.2n .8n
+PULSE 1.85 2.4 1n 0.2n 0.2n 0.2n .8n
+PULSE 2.4 1.85 1n 0.2n 0.2n 0.2n .8n
```

```
.SUBCKT OBUF_02
C_C10a         0 N66098  51.12f
C_C10b         0 QB  62.48f
C_C11a         0 N09146  51.12f
C_C11b         0 Q  62.48f
D_D10d         0 4 ESD
D_D10u         4 VCC ESD
D_D111d         0 3 ESD
D_D111u         3 VCC ESD
L_L10         N66098 QB  753.3pH
L_L11         N09146 Q  753.3pH
Q_Q1         VCC IND 5 TNSGB
Q_Q10         4 INX 2 TNSGB
Q_Q11         2 VCS1 1 TNSGB
Q_Q2         VCC IND 5 TNSGB
Q_Q5         VCC INDB N293875 TNSGB
Q_Q6         VCC INDB N293875 TNSGB
Q_Q9         3 INXB 2 TNSGB
R_R1         3 5  45
R_R10         4 N66098  39.5m
R_R11         3 N09146  39.5m
R_R2         4 N293875  45
R_R3         0 1  10
R_R90         100 99  100
T_T1         QB 0 99 0 Z0=50 TD=100ps
T_T2         Q 0 100 0 Z0=50 TD=100ps
.END OBUF_02
```

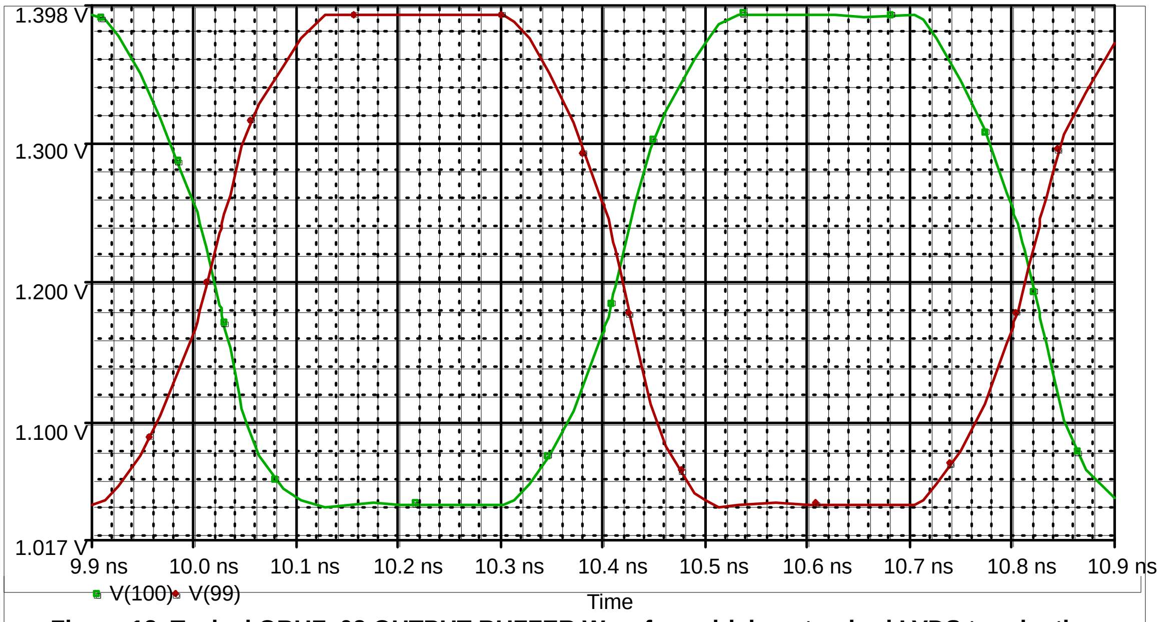

Figure 12. Typical OBUF_02 OUTPUT BUFFER Waveform driving standard LVDS termination

APPENDIX A

```
************* Transistor and Diode Models for ECLinPS MAX **************
.MODEL TNSGB NPN (IS=2.18e−17 BF=179 NF=1 VAF=96.5 IKF=2.42e−02
+ ISE=3.83e−16 NE=2.5 BR=20.4 VAR=2.76 IKR=1.98e−03 ISC=2.91e−17
+ NC=1.426 RB=55 IRB=1.12e−04 RBM=48 RE=6 RC=11 CJE=7.98e−15
+ VJE=.8867 MJE=.2868 TF=2.00e−12 ITF=0.4e−02 XTF=0.7 VTF=0.6 PTF=20 TR=0.5e−9
+ CJC=4.55e−15 VJC=0.632 MJC=0.301 XCJC=0.3 CJS=4.71e−15 VJS=.4193 MJS=0.256
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
******************************************************************************
.MODEL TNSGC NPN (IS=1.47e−16 BF=180 NF=1 VAF=96.3 IKF=1.62e−01
+ ISE=2.96e−15 NE=2.5 BR=20.2 VAR=2.76 IKR=1.34e−02 ISC=2.14e−16
+ NC=1.426 RB=25 IRB=1.50e−03 RBM=4 RE=1 RC=7 CJE=6.34e−14
+ VJE=.8867 MJE=.2868 TF=2.00e−12 ITF=0.25e−01 XTF=0.7 VTF=0.35 PTF=20 TR=0.5e−9
+ CJC=4.08e−14 VJC=0.632 MJC=0.301 XCJC=.3 CJS=11.12e−15 VJS=.4193 MJS=0.256
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
******************************************************************************
.MODEL ESD D (IS=9.99E−21 CJO=6.52E−14 RS=50.1 VJ=.82 M=.25 BV=35)
******************************************************************************
```

APPENDIX B

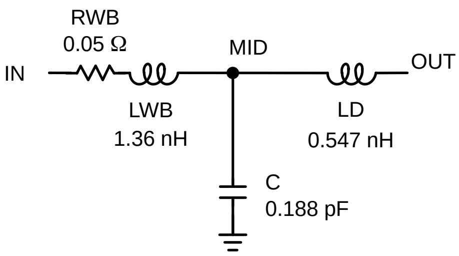

Figure 13. Schematic Model of 8 ld SOIC Packge

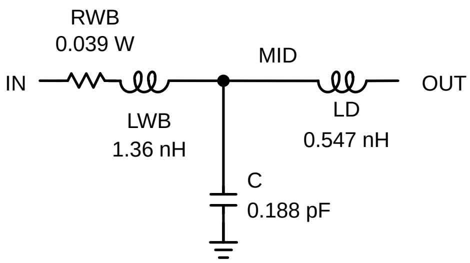

Figure 14. Schematic Model of 8 ld TSSOP Packge

Table 4.

Package: 8−Lead SOIC (D)	
Component	**Value**
RWB	0.05 Ω
LWB	1.36 nH
LD	.547 nH
C	0.188 pF

Table 5.

Package: 8−Lead TSSOP (DT)	
Component	**Value**
RWB	.039 Ω
LWB	1.36 nH
LD	.547 nH
C	.188 pF

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