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ADC Offset Calibration for BELASIGNA® 300

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APPLICATION NOTE

Introduction

This application note describes the procedure for calibrating the analog−to−digital converters (ADCs) on BelaSigna 300, and discusses when and why this calibration is recommended.

The intended audience is customers who are building high−fidelity audio applications using BelaSigna 300.

BACKGROUND

Analog to Digital Conversion on BelaSigna 300

The operational amplifiers (op−amps) used in the input stage of BelaSigna 300 produce DC offsets that are accumulated in the closed loop of the sigma−delta ADC. This accumulation creates ADC output oscillation that is periodic in nature, which may result in tones and/or bumps in the noise floor. The frequency of these bumps in the noise floor is directly correlated to the frequency of the ADC output oscillation and can be managed by adjusting the DC offset within the ADC itself. A DC offset can be selected to place the bump in the noise floor out of the sampling or audible frequency range. For more detail on how this DC offset accumulation manifests itself as a bump in the noise floor, refer to Appendix A.

The value of the DC offset is configurable for each ADC through a dedicated register. To determine the ideal DC offset value (which can be unique to each BelaSigna 300 device) and achieve the best performance, an ADC calibration procedure may be performed. Typically this would be performed at the production line, with calibration values stored in an SPI EEPROM attached to BelaSigna 300. These values would then be loaded at each boot time.

BelaSigna 300 provides 4 independent, 16−bit, 8x over−sampled analog−to−digital converters. Each of these channels has 8 possible gain settings (0, 12, 15, 18, 21, 24, 27, and 30 dB), and each gain setting for each channel may have a unique calibration value. Thus, a total of 32 possible calibration values are required for a complete system calibration. Depending on the application, however, it may be more efficient to calibrate the ADCs for only those pre−amplifier gain settings used.

When Is ADC Calibration Necessary?

The severity of the tones in the noise floor depends on the rate of DC offset accumulation, and the sampling rate at which the system is configured. The absolute worst case occurs when the fundamental frequency of oscillation is lower than the one−half of the sampling rate of the system (Fs/2). This can produce tonal spikes in the frequency spectrum as high as −70 dBFS. While this is quite rare for typical audio sampling rates, tones of this magnitude may be audible when low preamplifier gain values are used and for this reason calibration is recommended.

In general, calibration is recommended for most audio applications; however it may be beneficial to ignore the calibration procedure if your product is using a microphone as a signal source, as any ADC tones may be masked by the self−noise of the microphones.

THE CALIBRATION PROCEDURE

DC Offset Registers and Calibration

Each channel of the input stage has its own DC offset register. The ideal value for the DC offset depends on a number of factors including:

- The analog gain that is applied by each channel's preamplifier
- The maximum ADC current setting
- The rate at which the ADCs are running (clock divisor settings and corresponding sampling rate)

How the Calibration Works

The goal of the calibration procedure is to find a DC offset register setting that results in a specific DC offset at the output of the ADC. In particular, this target DC offset at the output of the ADC will ensure that any periodic oscillations due to accumulation are at a frequency outside the audio passband, minimizing the impact on the audio performance of the system. These DC offset register calibration values must be determined for each preamplifier gain setting on each ADC.

The relationship between the DC offset register setting and actual measured DC offset at the output of the input

stage is modeled to be linear, and for the purposes of the calibration procedure this is a very good practical approximation. The slope and intercepts of this linear relationship are unique to each device, and this is why calibration on a per−part basis is required. Once this linear relationship has been characterized, it gives the relationship between an appropriate DC offset register setting and a specific target DC offset.

To characterize the system it is necessary to measure the actual DC offset at the output of the input stage. To measure this DC offset, the onboard DC removal filter is disabled and a simple, two−stage finite impulse response (FIR) decimation is employed.

To find which DC offset register value produces the desired target DC level, a minimum of three measurements are performed. The first two measurements allow for a linear interpolation to be done, and the third measurement verifies the accuracy of the interpolation. Since not all devices will produce a perfectly linear relationship between the DC calibration register setting and the measured DC offset, the calibration routine uses an iterative technique to ensure the best calibration value is found. If a solution cannot be found within a maximum number of iterations, then calibration failure is indicated in a status flag. The calibration application provided by ON Semiconductor checks this flag and if the calibration procedure failed to converge nothing is written to EEPROM and an error is reported to the user. If you are integrating the calibration library routines into your own application, your code must check the status flag and take appropriate action should the calibration procedure fail.

Hardware Setup

The calibration procedure requires that a single analog input be left floating or, ideally, AC grounded (shorted to ground through a capacitor) for the duration of the calibration procedure. Grounding the input through a capacitor will result in a more consistent calibration. The value of the capacitor is not important, and can be the same type and value as the usual DC blocking capacitor (10 nF).

Only analog input pins AI1, AI2, and AI3 can be used for the calibration procedure as these are the only three pins internally multiplexed to all four ADCs. AI3 is not available on the WLCSP and cannot be used for reliable calibration on this package.

Running the Calibration

To calibrate the ADCs you will need to download the calibration script from the MyON customer portal at http://www.onsemi.com/. Once you have logged in to MyON, select “File Share Documents” from the Services menu on the left−hand side, and choose “BelaSigna 300”, then “Software” to access the folder containing the script. Download the archive file named belasigna300_adc_calibration.zip.

After inflating this archive you will find the source code for the calibration program, as well as a helper application written in Python that is used to perform the calibration procedure from the command line. Also included in the archive is a text file documenting the calibration program and helper application, describing in detail how to prepare your system and potentially rebuild the code to suit your specific settings. It is important that you change the clocking and sampling rate values in the calibration code to match your final product configuration and recompile the calibration routine as described in the documentation included in the archive.

To reconfigure and rebuild the code, you will need the SIGNAKLARA® Development Tools IDE. To download and execute the calibration application, you will also require a Communications Accelerator Adaptor (CAA) or some other communications device supported by the Communications Toolkit (CTK).

If you have any questions or require assistance, contact your local ON Semiconductor technical support.

FIRMWARE SUPPORT

The EEPROM File System

The BelaSigna 300 EEPROM file system contains a Manufacturing Area that holds device−specific calibration values, including the ADC calibration values. The 32 ADC calibration values are stored in EEPROM at byte addresses 0x0030 to 0x004F inclusive; with an additional status byte stored at EEPROM address 0x0050 (the calibration table is considered valid if bit 7 of the status byte is set). Additional details on the structure of the EEPROM file system can be found in the Firmware Reference Manual for BelaSigna 300.

The bootloader (also stored in EEPROM) performs the task of loading the user application as well as any calibration values from EEPROM to RAM. As part of the bootloading process, the bootloader copies the 32 calibration values plus the status byte from EEPROM to the base of Y memory at address 0x0000 for use by the system firmware.

Bootloading Over I2C

If your product does not include an EEPROM, but rather bootloads BelaSigna 300 over I^2C you will need to either:

- Calibrate the device every time after bootloading
- Include the calibrated ADC offsets as part of your application binary image

Either solution has its complications. It may be impractical hardware−wise to dedicate an analog input to calibrate the device every time it is bootloaded, or the time required to perform the calibration may be undesirable. Alternatively, including the calibration values as part of your application binary image may be difficult as these values must be determined on a per−part basis at production time.

It is up to you to determine the best approach when an EEPROM is not available. For your convenience, the calibration script will output a header file containing the

calibration values in a separate Y memory segment. Refer to the script documentation for more information.

Firmware Macros

Once the ADC calibration table is resident in Y memory, it is available for use by the system firmware. There is a single macro called Sys_CalibrateADCs that reads the calibration table status byte, and if it is valid, copies the appropriate calibration values based on the current preamplifer gains into the bit fields of the 32−bit control register at address 0xE14F in P memory. This macro is simply invoked with no arguments, and is expected to be called after the preamp gains have been configured. In fact, the system macro Sys_Set_IN_GAIN_CTRL automatically calls Sys_CalibrateADCs after configuring the preamplifier gains. Assuming there is a valid ADC calibration table in Y memory, the ADCs are in a calibrated state immediately after the call to Sys_CalibrateADCs.

THE CALIBRATION LIBRARY

The calibration library used by the calibration script can also be integrated into your own applications and scripts. All that is required is to include the header file (dcOffsetCal.cfi) in your project, instruct the linker to link with the library file (sk3_dcOffsetCal.lib), and insert the appropriate calls to the library routines in your application code.

For details on usage, refer to the documentation included with the DC offset calibration library.

APPENDIX A

Relationship Between Audio Quality and DC Offset

This appendix is provided for those who wish to understand the background behind the ADC calibration procedure. It is not critical to read or understand this section to perform the calibration.

The operational amplifiers (op−amps) used in the input stage of BelaSigna 300 produce DC offsets that are accumulated in the closed loop of the sigma−delta ADC. This accumulation creates ADC output oscillation that is periodic in nature.

There is a relationship between the DC offset magnitude, and the ADC output oscillation. A small amount of DC offset corresponds to a slow ADC output oscillation (large period between 2's complement wrap around), and a large amount of DC offset corresponds to a fast ADC output oscillation (small period between 2's complement wrap around). This is illustrated in Figure 1.

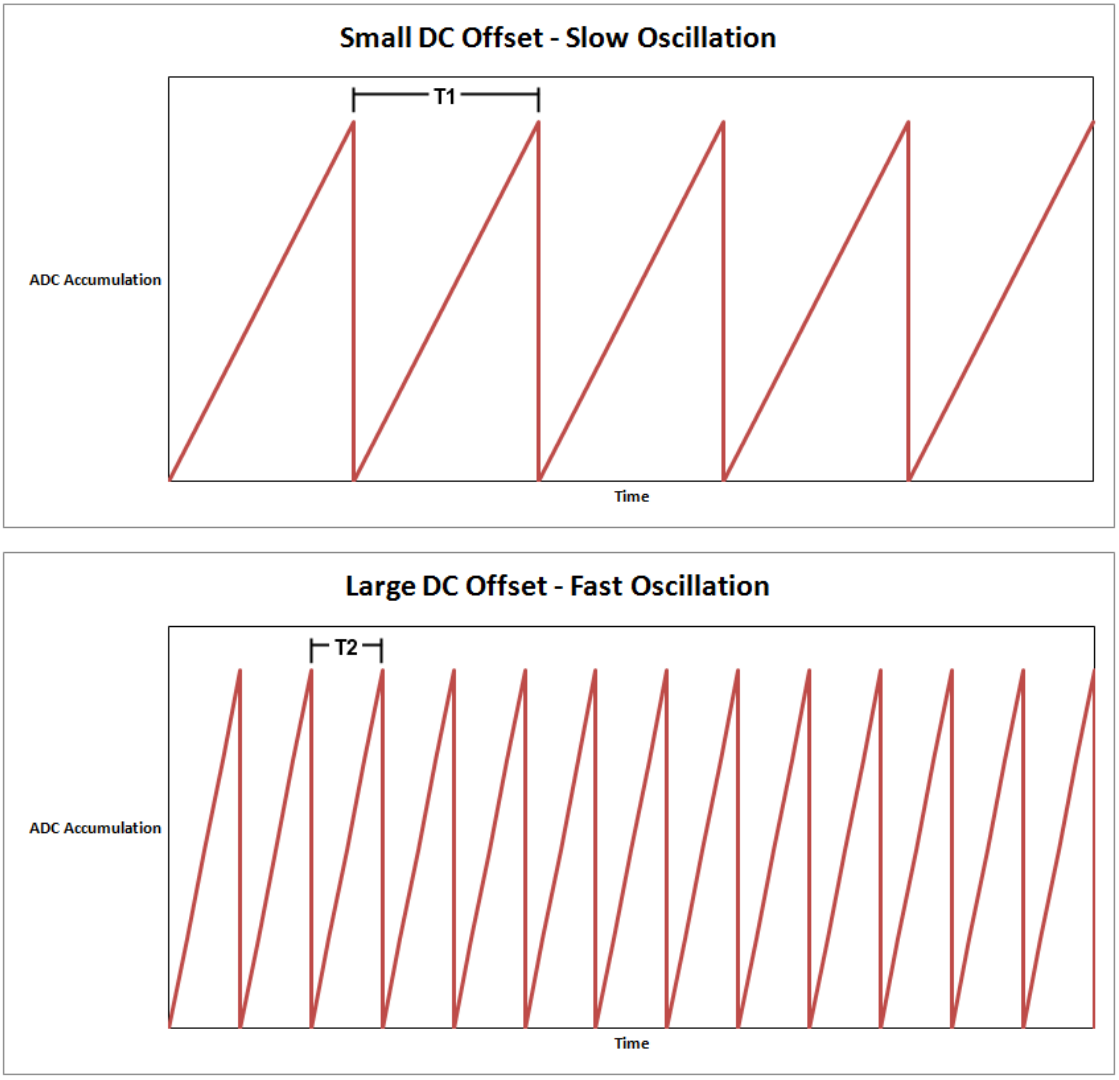

Figure 1. Period of ADC Output Oscillation

Depending on the period of this oscillation, a hump may be visible in the noise floor at the frequency of the ADC output oscillation. A small DC offset (slow ADC output oscillation) may result in an oscillation frequency that is less than the Nyquist Frequency ($F_s/2$), and hence will become visible in the baseband, as illustrated in Figure 2.

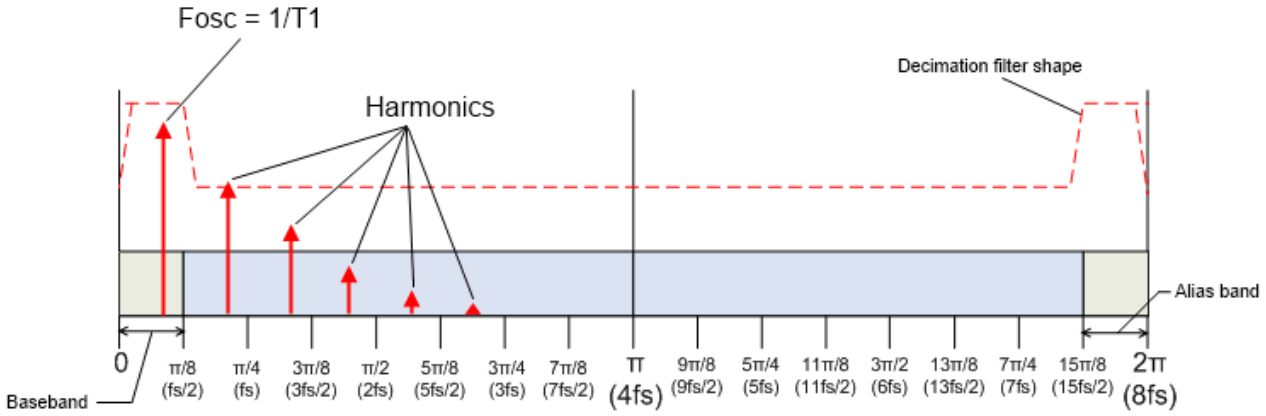

Figure 2. Slow ADC Output Oscillation

A large DC offset (fast ADC output oscillation) may result in an oscillation frequency with lower−order harmonics (2nd or 3rd) visible in the alias band (and thus visible in the baseband as well), as shown in Figure 3.

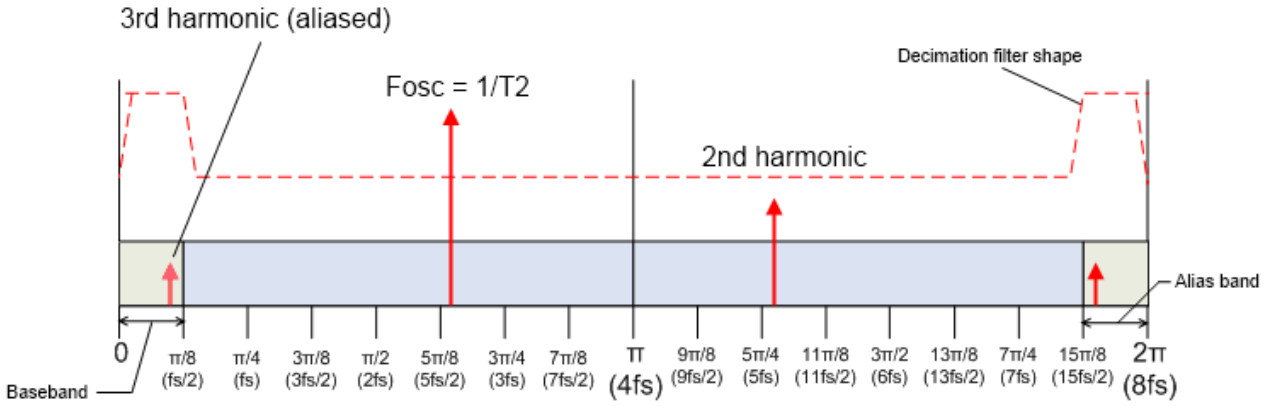

Figure 3. Fast ADC Output Oscillation

In both of these cases, there will be a noticeable hump in the noise floor, which results in audible tones. This can be an issue, depending on the application. The goal of the calibration is to prevent this hump from appearing in the baseband. To do this, the DC offset should be tuned so that the ADC oscillation frequency will be somewhere between $F_s/2$ and any alias band, but located such that any harmonics are either outside the alias band as well, or small enough that they are not detectable in the noise floor. Characterization has shown that calibrating the ADCs to place the ADC output oscillation at 1.333 * F_s results in a favorable situation where the 6th harmonic lands in the middle of the alias band. This harmonic is small enough to be undetectable in the noise floor, and has the added advantage that it will be removed by the DC removal filter on the input stage. This is illustrated in Figure 4.

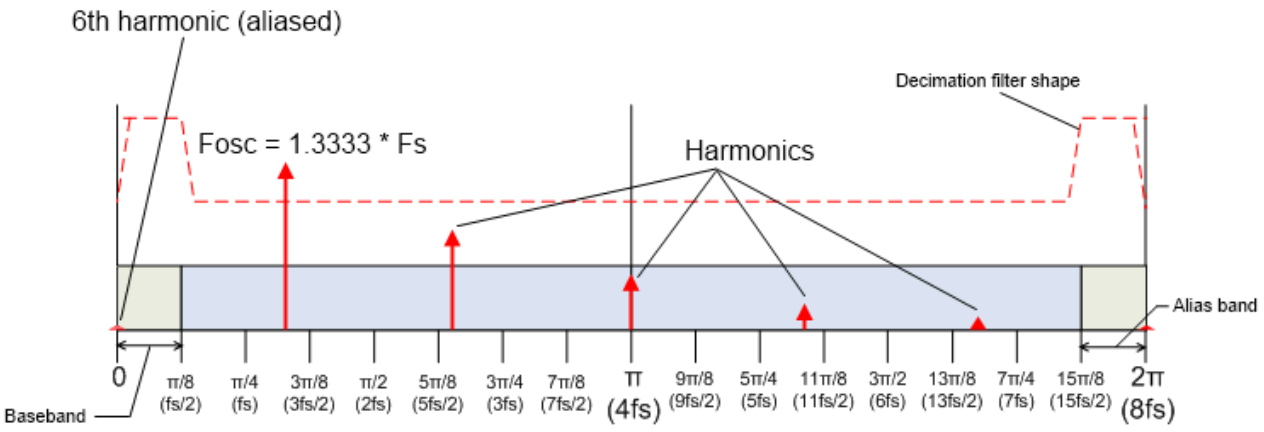

Figure 4. Ideal ADC Output Oscillation

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